DEVELOPMENT OF THE SIRIUS RF BPM ELECTRONICS

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Abstract

A Beam Position Monitor (BPM) system is being developed for the new low emmitance 3 GeV Brazilian synchrotron light source, Sirius. The Sirius BPM electronics is a modular system based on a PICMG® MicroTCA.4 platform using ADC mezzanine cards in ANSI/VITA 57.1 FMC form factor and standalone RF front-end boards. It has been designed under the CERN Open Hardware License (OHL) by the Brazilian Synchrotron Light Laboratory (LNLS) in collaboration with the Warsaw University of Technology (WUT). This paper presents the overall architecture of the Sirius BPM electronics system and performance evaluation of its first prototype, comprehending beam current, filling pattern and temperature dependences, and position measurement resolution as a function of the beam current.

INTRODUCTION

Sirius is a new 3 GeV synchrotron light source under construction in Brazil [1], targeting a 0.28 nm.rad natural emittance. The commissioning of the storage ring should start in the first quarter of 2016.

In total there will be more than 320 RF BPM pick-ups on Sirius, from which 240 are button BPMs distributed along 518 meters of the storage ring circumference (12 per super period), 50 BPMs on the booster and more than 30 BPMs on the LINAC and transfer lines.

The development of an RF BPM electronics for Sirius [2] started in the second semester of 2010, following two main directives: i) design a modular and reconfigurable system (hardware and software) to be used in accelerator applications other than BPMs; ii) adopt a collaborative approach for the development in order to strengthen its performance and usability on the scientific instrumentation community.

SYSTEM REQUIREMENTS

The Sirius BPM system short-term and long-term requirements are summarized in Table 1. They consider a minimum vertical beam size of 1.4 µm at the center of the longer straight section of the storage ring.

Table 1: General Requirements for Sirius's Storage Ring Electron Beam Stability

Parameter	Value
Resolution (RMS) @ 0.1 to 1000 Hz	< 0.14 µm
Resolution (RMS) @ turn-by-turn full bandwidth	< 3 µm
1 hour position stability (RMS)	< 0.14 µm
1 week stability (RMS)	< 5 µm
Beam current dependence (w/o top-up)	< 1 µm
Beam current dependence (w/ top-up)	< 0.14 µm
Filling pattern dependence	< 5 µm
First-turn resolution (RMS)	< 0.5 mm
Horizontal/Vertical plane coupling	< 1%

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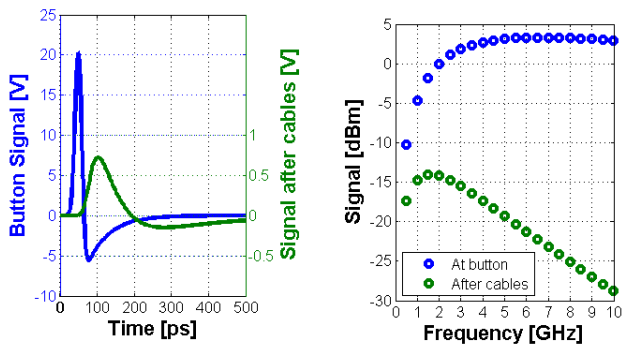
BPM Pick-up and RF Signal

The Sirius storage ring's RF BPM pick-ups are of button type, with 45° rotated horizontal and vertical axis in a circular vacuum chamber with 12 mm radius, resulting in a geometry factor of 8.5 mm for both planes [3]. The characteristics of the pulsed RF signal are summarized in Table 2.

Table 2: Beam Signal Characteristics

Parameter	Value
RF accelerating frequency	500 MHz
Revolution frequency (harmonic number = 864)	578.7 kHz
Bunch length	8.8 ps
Amplitude fluctuation due to top-up	~ 1%

The RF signals exiting the pick-ups are brought to the BPM electronics by 25 meters of LMR195 coaxial cables, resulting in a significant attenuation of high harmonics of the pulsed RF signals. Figure 1 shows the time- and frequency-domain simulations of the beam signal considering a 6 mm diameter button.



(a) (b)

Figure 1: Simulation of the RF voltage signal at button pick-ups and after LMR195 cables of a 500 mA multi-bunch beam with ideal 100% filling: (a) Time-domain; (b) Frequency-domain (RF frequency harmonics).

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The simulation shows that for a 500 mA multi-bunch beam there is -17 dBm of 500 MHz signal available to be processed by the BPM electronics. For lower beam currents, factors of -2 dB (400 mA), -4.5 (300 mA) dB, -8 dB (200 mA), -14 dB (100 mA) and -28 dB (20 mA) must be applied to scale the frequency-domain simulation to the correct signal levels.

An RF Front-End (RFFE) [4] has been designed to filter out all RF harmonics other than the 500 MHz component with more than 80 dB attenuation at stopband and 45 MHz passband. It provides up to ~48 dB of gain.

SYSTEM ARCHITECTURE

The Sirius RF BPM electronics uses the so-called under-sampling technique to bring the first harmonic of the beam RF signal at 500 MHz to an intermediate frequency (IF) and digital down-conversion plus decimation to provide beam position measurements in baseband at different and configurable data rates/bandwidths (e.g. turn-by-turn, orbit feedback and slow monitoring rate).

The system is built in a modular fashion, based on proven industrial standards. In that sense, the Sirius RFFE is a standalone analog electronics controlled by Ethernet and additional synchronization input. The ADC electronics is a 4-channel 16-bit mezzanine card in FMC form factor providing sampling rates above 100 MS/s and flexible clocking resources [5]. The digital signal processing electronics are FPGA boards in double-width AMC cards featuring large SDRAM memory (512 MB or 2 GB), 2 FMC mezzanine slots for hosting up to two BPMs and provision to communicate with up to 8 instruments (e.g. orbit corrector power supplies, X-ray BPMs, insertion device encoders) via multigigabit links (SFP+ interface) in a MicroTCA Rear Transition Module (μRTM) [5]. The FPGA boards are used in MicroTCA.4 crates providing common infrastructure for power, cooling, reference clock distribution, shared trigger lines, PCI Express x4 connectivity to a crate CPU module and 1 Gigabit Ethernet or point-to-point connectivity from all FPGA boards to the fast orbit feedback (FOFB) and general accelerator's distributed control system networks.

The FPGA board is made completely generic to allow its use in several accelerator applications. It can be used integrated in a MicroTCA system or as standalone board. It has full hardware support for the White Rabbit timing system.

WORK IN PROGRESS

The BPM electronics development work is in its first prototyping phase. The first version of all main boards (RFFE, ADC and FPGA) were already produced and delivered to LNLS.

The RFFE has been designed by LNLS. It features diagonal antenna signals swapping and board temperature digital control to assure adequate long-term stability.

The ADC board has been designed in two variants (LTC2208 and ISLA216P25 ADC ICs) in a collaboration between LNLS and the Warsaw University of Technology (WUT).

The FPGA board was specified by LNLS and designed by WUT. First versions of FPGA firmware for basic digital signal processing (digital down-conversion, filtering and decimation, channels switching) and ADC board control and monitoring were developed for allowing the first tests.

The RFFE control board is currently implemented using an "mbed LPC1768" development board plus dedicated discrete logic for implementing the precise triggering of the RF channels switching scheme. It is used for general command and monitoring of the RFFE controllable devices. Both EPICS and Labview TCP/IP high-level interfaces have been implemented, following the control protocol currently under design for the Sirius Control System [6]. Digital control of board's temperature was also implemented in Labview and tested successfully [4].

LABORATORY TESTS

For the first performance evaluation of the Sirius BPM electronics, the experimental setup described in Fig. 2 has been set.

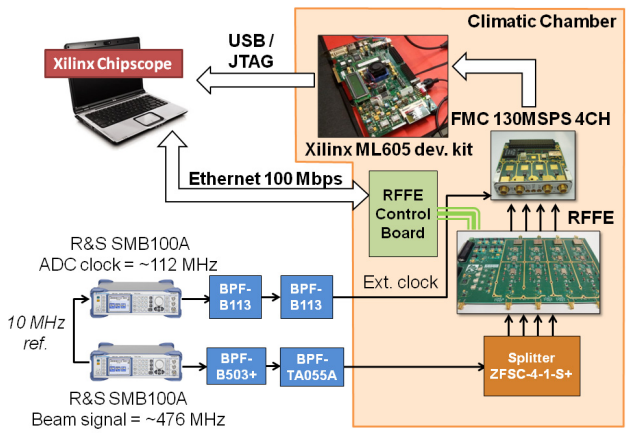

Figure 2: Experimental setup for the Sirius BPM electronics prototype evaluation.

Development kits were used for the RFFE control ("mbed LPC1768") and FPGA processing board (Xilinx ML605 kit). The RFFE and ADC boards (130 MS/s version) are the first version prototypes. All the signal generators are synchronized with a common 10 MHz source. The Sirius BPM electronics was placed inside a temperature controlled climatic chamber.

Libera Brilliance+ is used as benchmark for resolution experiments. Libera RF&Clock generator is used for generating the gated signal for the Filling Pattern Depedence (FPD) tests. The Libera unit was placed outside the climatic chamber.

During all the tests a geometry factor of 10 mm has been used in both planes in order to allow easy comparison among other electronics. The RF signal frequency was 476 MHz (LNLS UVX's frequency) instead of 500 MHz (Sirius's frequency) to allow

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comparison with tests with beam at LNLS existing storage ring, therefore the RFFE electronics uses a slightly modified design with bandpass filters centered at 476 MHz. For the Sirius BPM, the ADC clock is fed directly from an RF generator; for Libera, the same generator was used to generate the revolution frequency reference clock.

Resolution vs. Input Power

In order to evaluate the measurement resolution as a function of the beam current, a power sweep of the RF signal (single tone) was done for different configurations of gain using two attenuators of the RFFE processing chain. 65536 points were collected in each run, at the FOFB data rate (100 kS/s for Sirius BPM and 10 kS/s for Libera). The tests were performed with the switching scheme turned off in both electronics for easiness of comparison, since at date the switching scheme is not implemented for the Sirius BPM at the FOFB data rate. The results are shown in Fig. 3, where a measurement bandwidth with an upper bound (2 kHz) higher than the specification (1 kHz) is considered.

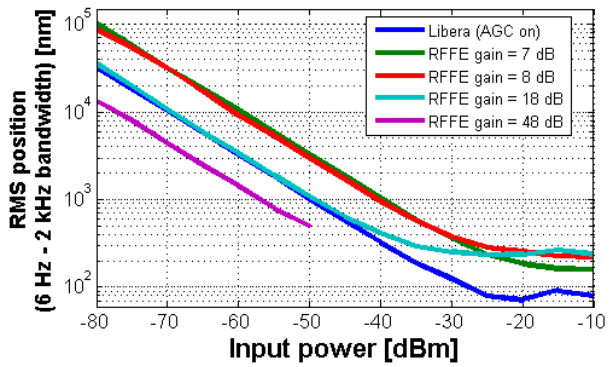

Figure 3: RMS resolution (6 Hz to 2 kHz bandwidth) vs. input power.

It can be noted that for the Sirius BPM RFFE gains of 8 and 18 dB the position resolution for higher power inputs (above -30 dBm) cannot reach values lower than ~230 nm, while Libera Brilliance+'s lower limit for very similar test conditions is below 100 nm.

When some specific configurations of attenuators on the RFFE are done by increasing the overall attenuation, the signal level at the ADC inputs is decreased without great impact to the overall noise figure. For instance, the best result (160 nm) was obtained for power levels higher than -20 dBm, equivalent to a 350 mA beam current.

For very low input powers (below -50 dBm, or 10 mA beam current), it is possible to set no attenuation on the RFFE to improve the resolution.

Short-range Beam Current Dependence

In order to evaluate the beam current dependence (BCD) during top-up operation, a short-range power sweep (± 0.1 dB) was done in the RF signal simulating the beam current variation (centered beam). Each data value is taken from the mean value of 10 seconds of stable 10 Hz beam position data. The results are summarized in Fig. 4. During the test the diagonal channels (A-C, B-D) were swapped at ~13 kHz, with manual amplitude gain unbalance compensation at the beginning of the test.

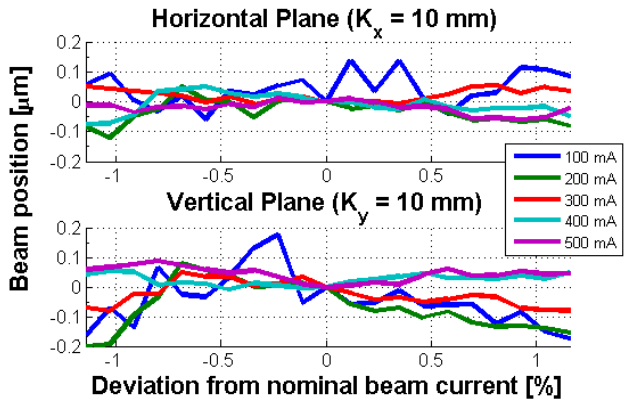

Figure 4: Short-range beam current dependence for centered beam in different beam current scenarios.

The results show that within the 1% range of top-up variation, beam current values greater than 300 mA allow reaching the specification of 140 nm of BCD, while 100 and 200 mA beam currents may lead to regions where the specifications are met and others where it is missed for up to a factor of 2.

Filling Pattern Dependence

The filling pattern dependence test was performed in a similar condition as the BPD tests. The same data rate (10 Hz) and sample window at each point (10 s) were used, as well as the use of RF channels switching and its initial calibration. The test was done simulating a 100 mA beam current and 20-100% filling pattern sweep. Figure 5 shows the result.

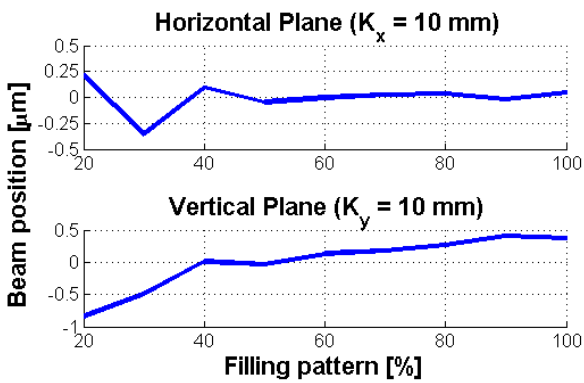

Figure 5: Filling pattern dependence for a 100 mA centered beam.

The results show that a FPD of 5 µm is a very relaxed requirement that can be already met with the current version of the electronics prototype.

Temperature Dependence

Figure 6 shows a long-term test performed during nearly 2 days of temperature set-point sweeping (from

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25°C to 33 °C) inside the climatic chamber. The input power was set compatible with a 500 mA beam current. During the test the RF channel switching was turned on and amplitude compensation was done manually at the beginning of the test. The RFFE temperature control was turned off during the entire test.

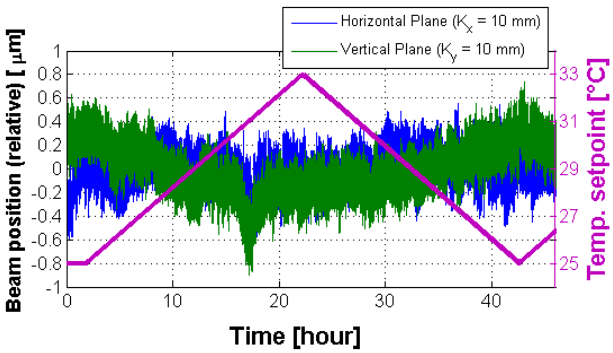

Figure 6: Temperature dependence for a 500 mA centered beam (10 Hz data rate).

The temperature dependence was kept below 140 nm for the long term run under a temperature variation (8 °C) much larger than expected for the real setup at Sirius (< 1 °C). The requirement of long-term stability and temperature dependence is not a limiting factor of performance for the BPM electronics under consideration.

COLLABORATION

The Sirius BPM electronics project unfolds in an open collaborative manner. LNLS's strategy to develop the project with a reduced manpower was to interact with similar institutes worldwide and ask for input from key similar BPM and data acquisition developers about the general architecture of the system. Several technical visits and discussions by the BPM project's mailing list have lead to improvements on the final system specification, remarkably the modular approach inspired on the Paul Scherrer Institut's (PSI) digital BPM design for SLS [7] and the adoption of proven and largely supported industrial standards on most of the Sirius BPM subsystems. The project follows an entirely open-source approach, with all related designs made publicly available at the CERN Open Hardware Repository [8]. It aims at evolving the final product towards the state-of-the-art with easy integration with other accelerator systems, avoiding duplication of efforts and vendor lock-in.

The WUT contributes with projects of hardware, FPGA firmware and low-level software and has found interest on parts of the system from GSI's Cryring and CBM experiments and CERN's NA61 experiment and CMS.

CONCLUSION

The first bench tests results show that the BCD, FPD and long-term stability figures of the Sirius BPM electronics for centered beams are partially or entirely in accordance with the specifications. However major improvements in the resolution for high input powers must be done by exploring the several possibilities of attenuation in the RFFE and clocking schemes on the ADC board. Systematic studies must also be carried out for off-centered beams.

The development of the second version of all hardware is underway. Small impedance matching issues were found on the ADC boards and will be investigated. The RFFE can still be improved by simplifying the calibration schemes, removing the power supply from the board and simplifying the onboard temperature control.

Several FPGA firmware and software functionalities are still to be implemented, for example the final port of the digital signal processing chain to the AMC FPGA board, amplitude and phase compensation of antenna signals as well as the de-spike mechanism for switching operation mode, automatic gain control, distribution of the revolution frequency clock, triggered acquisition support, integration with the distributed control system and implementation of mis-steered beam interlock mechanism.

LNLS is in the process of ordering a 12-BPM prototype rack with complete infrastructure, with delivery expected to December 2013. Entirely automated test suits will be developed to allow systematic evaluation of a large number of electronics.

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