Paul Scherrer Institut

A Generic BPM Electronics Platform For European XFEL, SwissFEL and SLS

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Paul Scherrer Institut

Contents

Introduction

PSI Electron BPM Systems & Design Activities

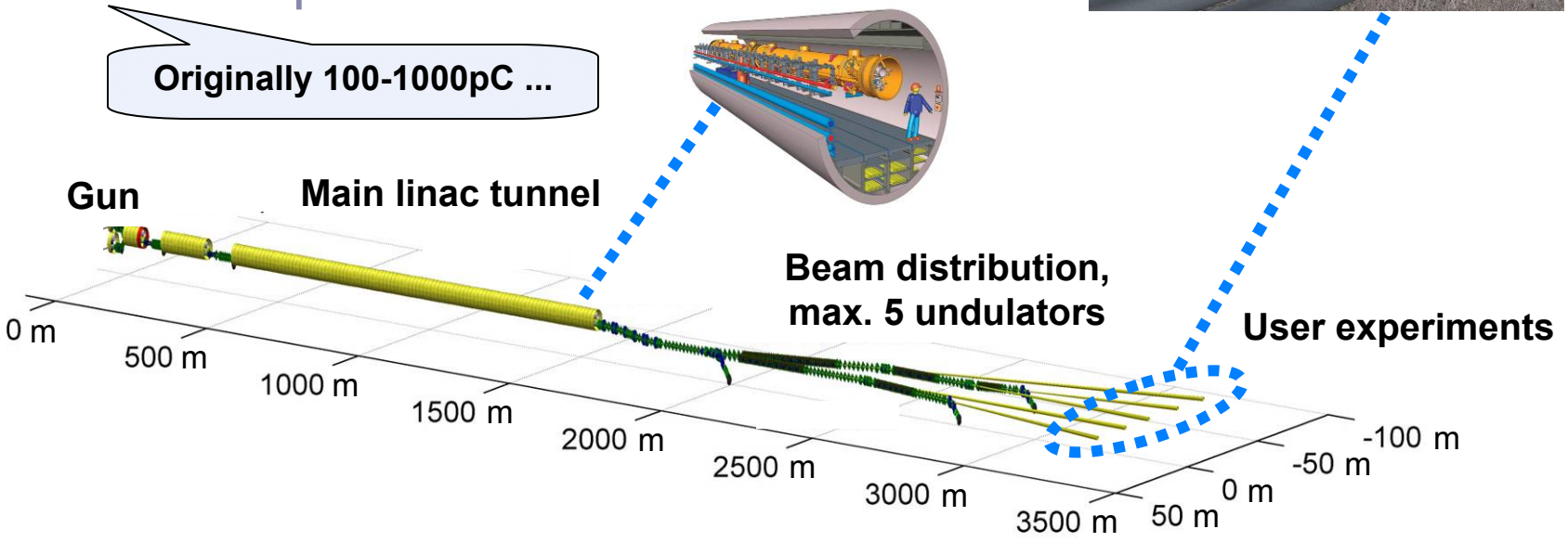
Accelerator	***1st Beam***	***# BPMs***	***Status / Activity***
SLS	2000	~140 (button, reson. stripline)	Digital BPM system since 2000. 2011: Start design of new BPM electronics. SLS Linac: FEL BPM test area.
SwissFEL Test Injector	2010	~25 (reson. stripline, …)	19 resonant stripline BPMs in operation. Test area for cavity & button BPMs.
FLASH-II	2013	~20 (cavity)	PSI provides BPM electronics (E-XFEL pre-series) for ~20 E-XFEL type cavities.
E-XFEL	2014/15	~410 (button, cavity)	PSI provides BPM electronics for ~290 buttons & ~120 dual-resonator cavities.
SwissFEL	2016	~150 (cavity)	Adaptation of E-XFEL cavity pickups & electronics to lower charge & shorter bunch spacing.

All BPM electronics PSI in–house designs, except ~30 re-entrant cavity BPM RFFE in E-XFEL (C. Simon, CEA/Saclay).

Introduction

European XFEL

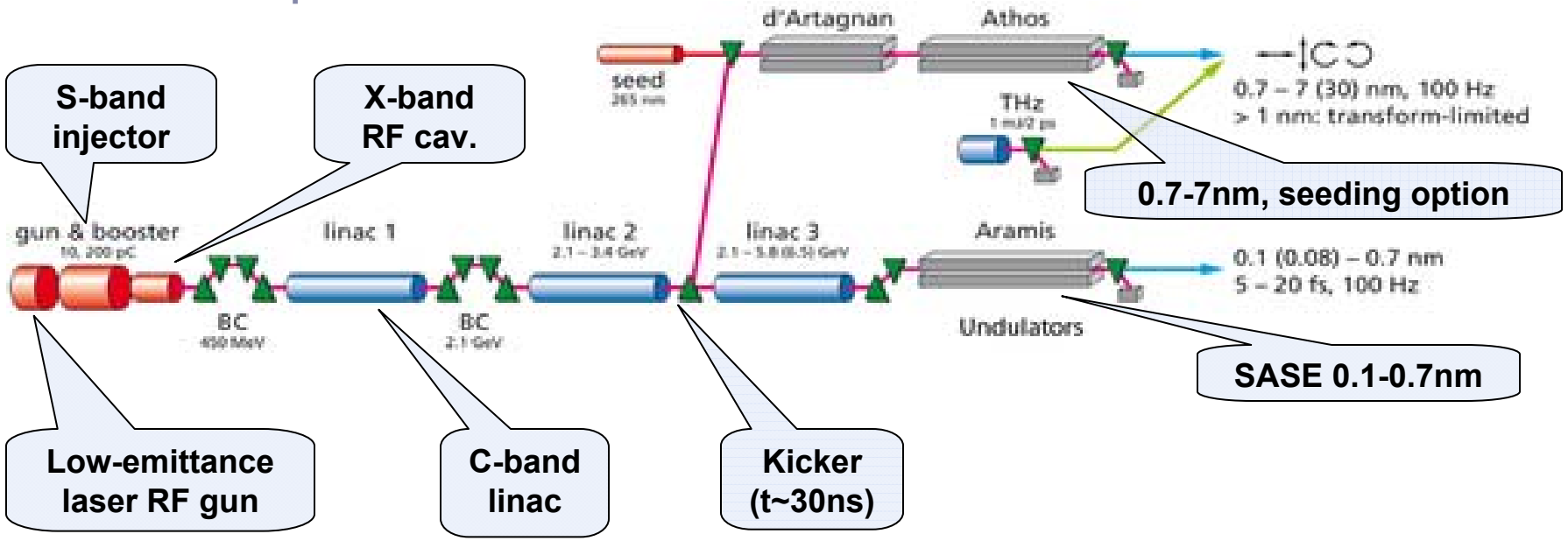
- L ~ 3400m. 17.5GeV. SASE <0.1nm.
- Trains of ~2800 bunches @ 10Hz.
- ~222ns min. bunch spacing.
- 20-1000pC / bunch.



Introduction

SwissFEL

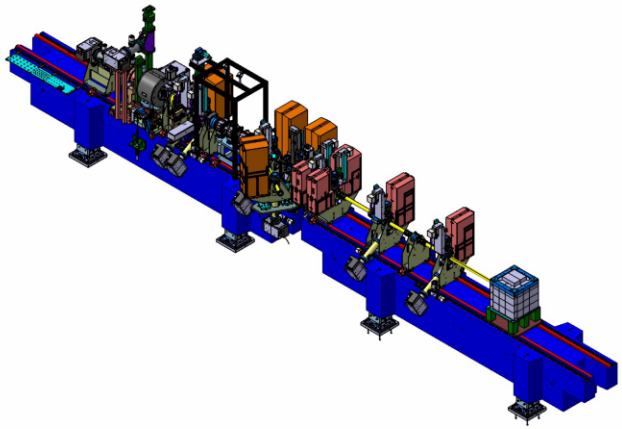
- L~700m. 5.8GeV. SASE, λ_{min}=0.1nm.
- Trains of 2 bunches (1 per undulator).
- ~28ns bunch spacing, 100Hz.
- 10-200pC.

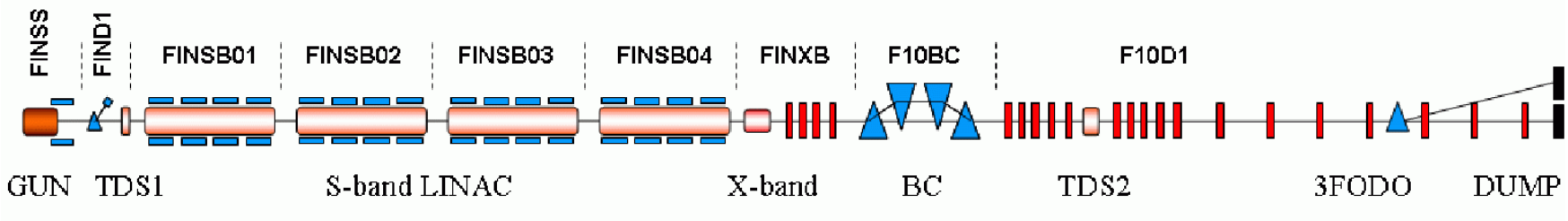


Introduction

SwissFEL Test Injector

- Goal: R&D for SwissFEL.
- Beam since 2010.
- E_{max}~250MeV, 1 bunch, 10Hz.
- 10-500pC.

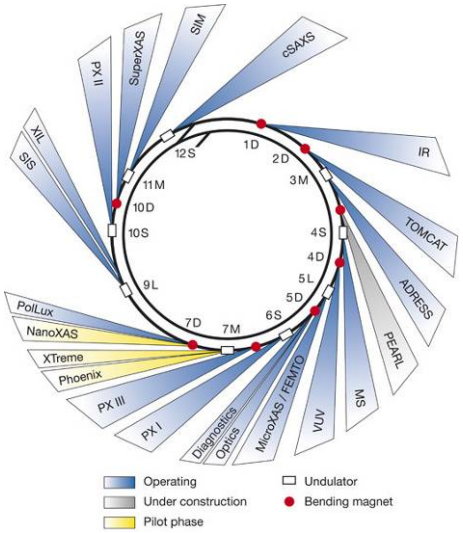




Introduction

SLS

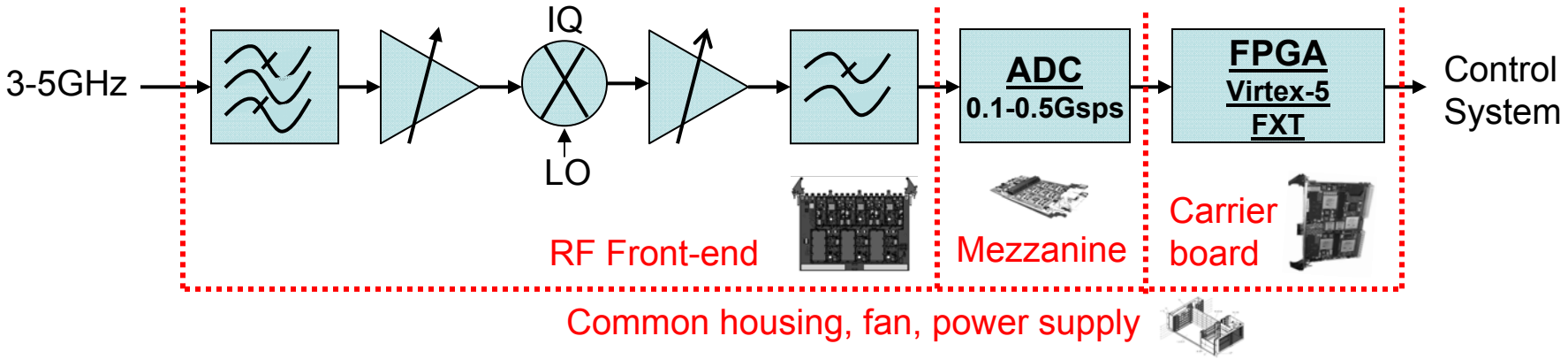
- 2000: 1st Beam.
- 2001: User Operation.
- 400mA top-up, 2.4GeV, 500MHz.
- Ring: L=288m, f_{rev} ~ 1MHz.



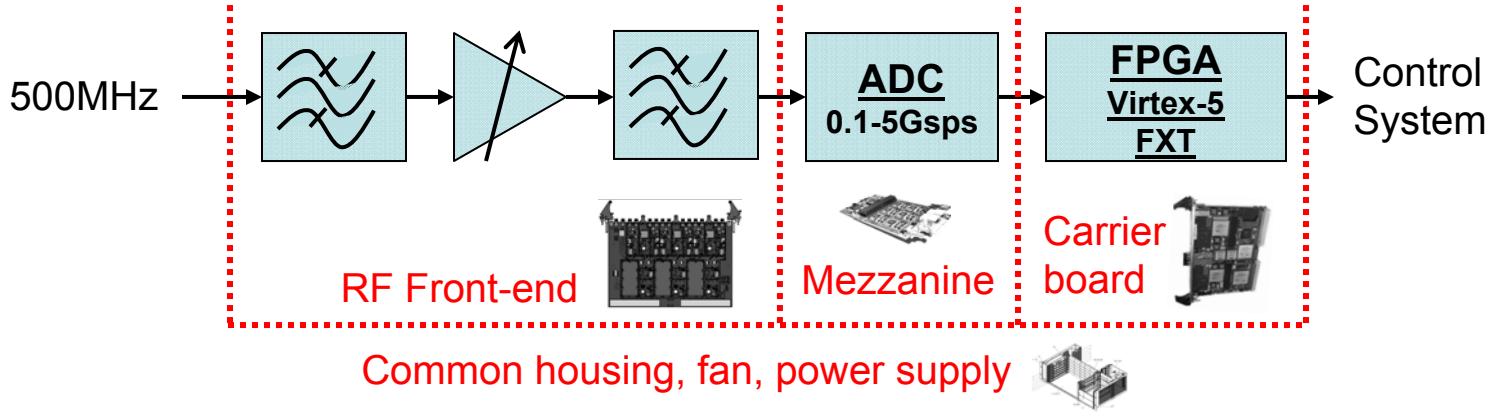
Introduction

Modular BPM/Diagnostics Platform Architecture

- E-XFEL / SwissFEL Cavity BPM Electronics (Simplified)



- New SLS BPM Electronics (Simplified)



Introduction

SLS & FEL BPMs: Electronics Platform Strategy

- Modular design: RF front-end, ADC mezzanine, FPGA carrier board. Standardized interfaces.
- SLS BPMs can use same FPGA carrier board as E-XFEL & SwissFEL.
- ADC mezzanine: Requirements for SLS BPMs & FEL undulator BPMs also very similar (16-bit, >100MSPS, …). Synergies save development time.
- Need new SLS-specific RF front-end.
- SLS Goal: Improve noise (>3x, ideally <100nm @ 2kHz), drift (active temperature stabilization, ...), latency, ...

Contents

PSI BPM Electronics Generations

PSI BPM Hardware Evolution: From Specific to Generic

Gene-ration	Final Application	Year	RFFE In/Out Fre-quency [GHz]	ADC Boards	Digital Back-End	ADC Data Deci-mation +Filter	Xilinx FPGA Type
0	SLS	2000	0.5/0.036	Specific	Specific	ASIC	-
1	Cyclotron	2005	0.1		Generic		Virtex 2Pro
1.1	SwissFEL TI	2010	0.5			FPGA	
2	FLASH-II	2013	3.3/0	Generic			Virtex5 FXT
	E-XFEL**	2015	.../...				
2.1*	SwissFEL	2016	3.3-4.8/0				Artix-7 & Kintex-7
	SLS	2016+	0.5				

Specific means: Has features (filters, ...) that prevent general-purpose ("generic") use

* Under development.

** Will use gen 2.1 when available: Interfaces backward-compatible.

PSI BPM Electronics Generations

BPM ADC Performance & Interface Evolution

per Digital Back-End Board

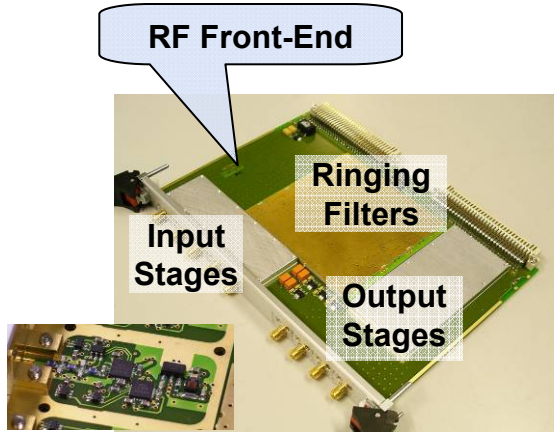
BPM Gene-ration	Final Application	Year	#Channels x ADCSampleRate [Samples/s]	Max. Sample Rate Supported by Back-End Interface (for parallel non-DDR data)
0	SLS	2000	4x40M (14-bit)	<100Mbps (Single Ended)
1	Cyclotron	2005	4x40M (14-bit)	<100Mbps (Single Ended)
1.1	SwissFEL TI	2010	4x5G (1024-Cell S&H) / 33M (S&H readout, 14 bit)	
2	E-XFEL Cavity	2013	12x160M (16-bit)	<1.25Gbps (LVDS)
	E-XFEL Button	2015	16x500M (12-bit)	
2.1*	SwissFEL	2016	12x160M (16-bit)	
	SLS	2016+	8x160M (16-bit)	

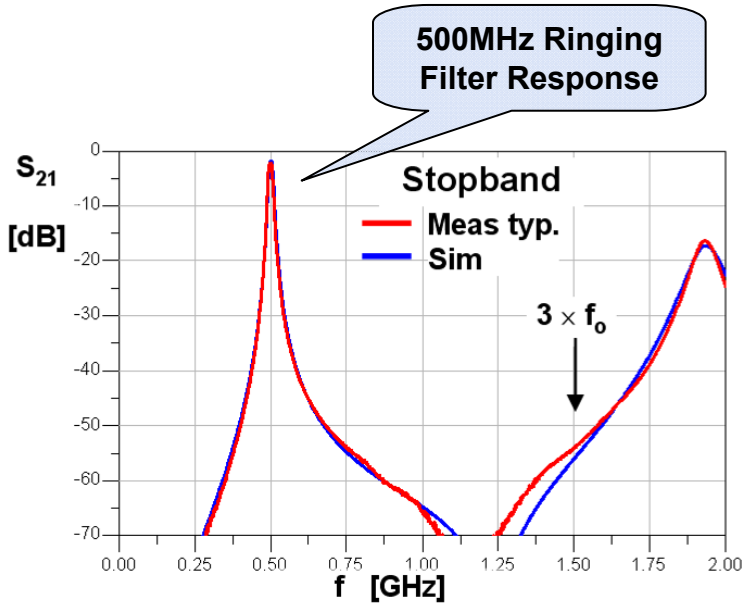
Contents

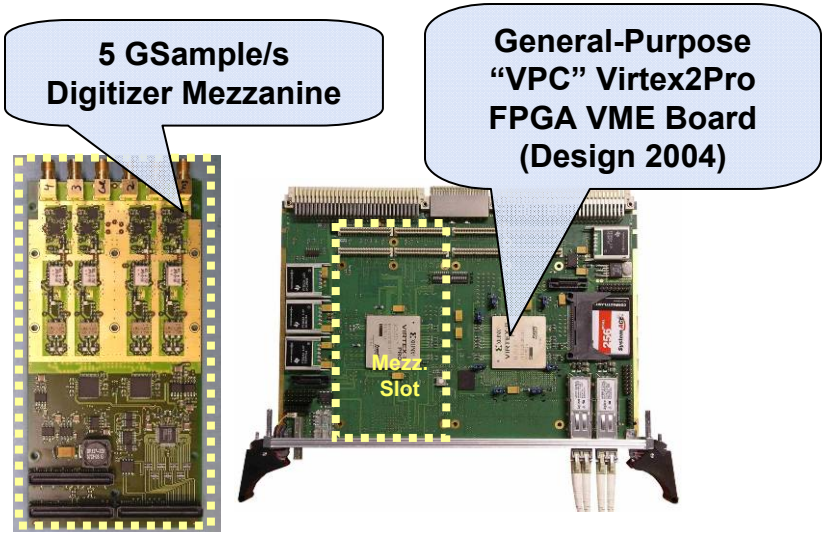
Examples & Status: SwissFEL Test Inj.

BPM Generation 1.1: 500MHz Resonant Stripline

- PSI in-house design, incl. 5GSPS analog waveform sampling chip (originally designed for low-cost 2000-channel muon detector digitizer).



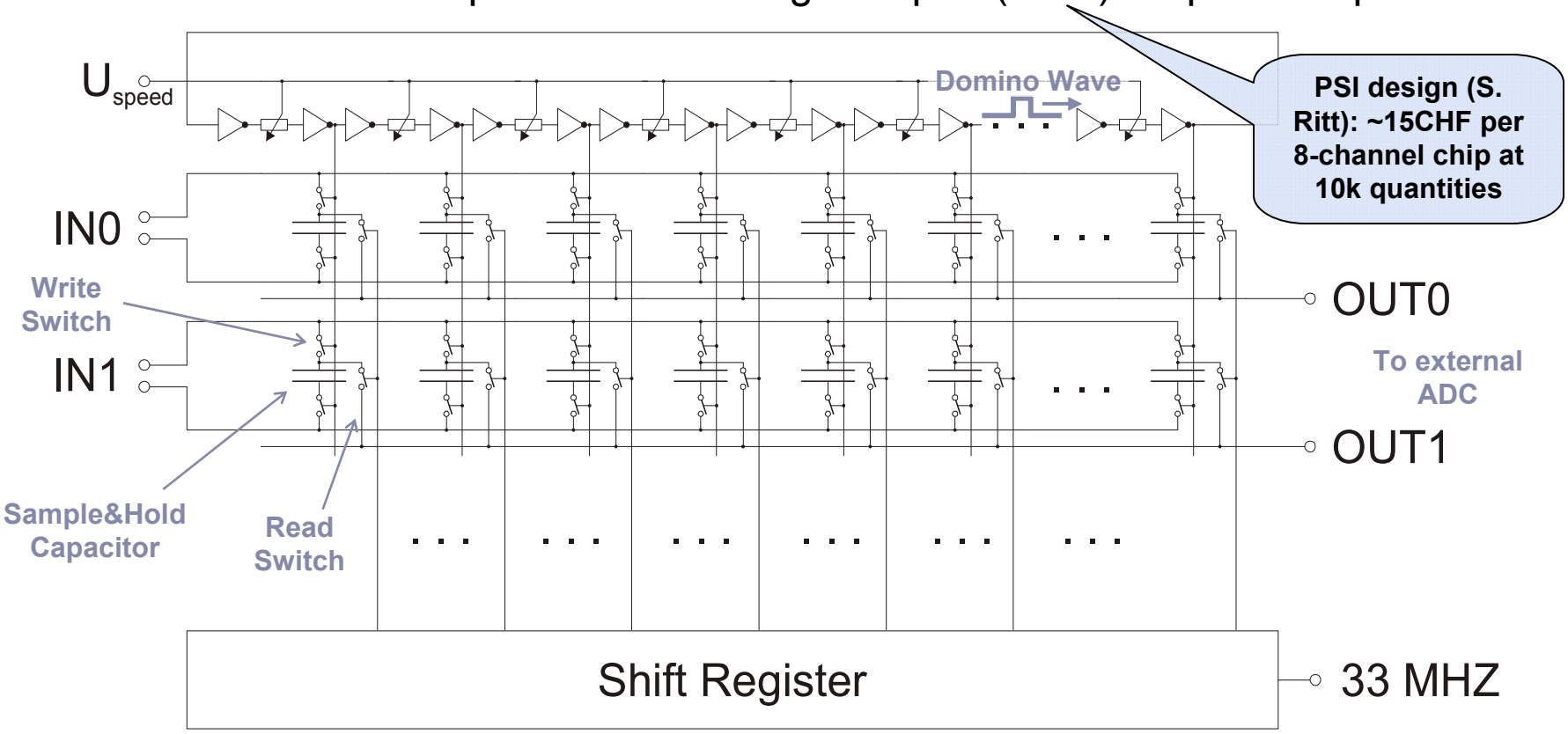




Examples & Status: SwissFEL Test Inj.

Analog Waveform Sampling Chip

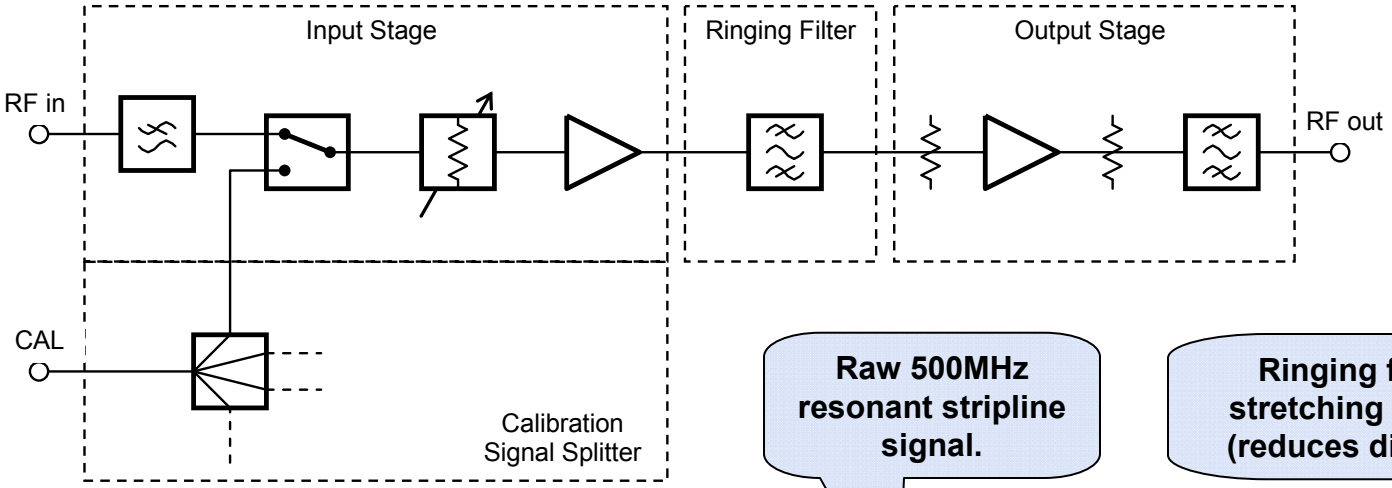
Low-cost 5 GSample/s Domino Ring Sampler (DRS) Chip - Principle



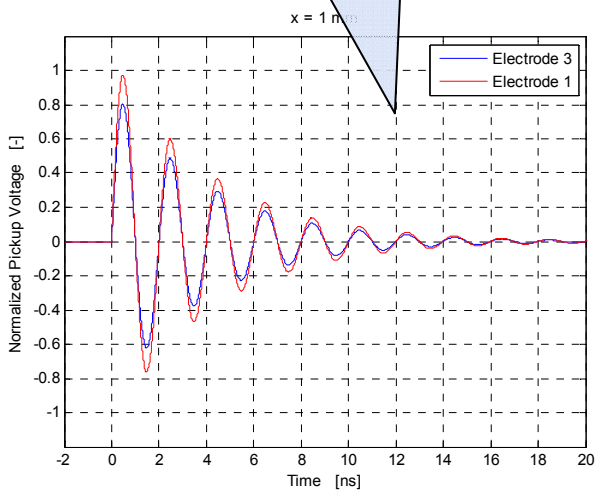
[S. Ritt, "Design and Performance of the 5 GHz Waveform Digitizing Chip DRS3", *IEEE Nucl. Sc. Symp. Conf.*, Honolulu, 26. Oct - 3. Nov. 2007]

Examples & Status: SwissFEL Test Inj.

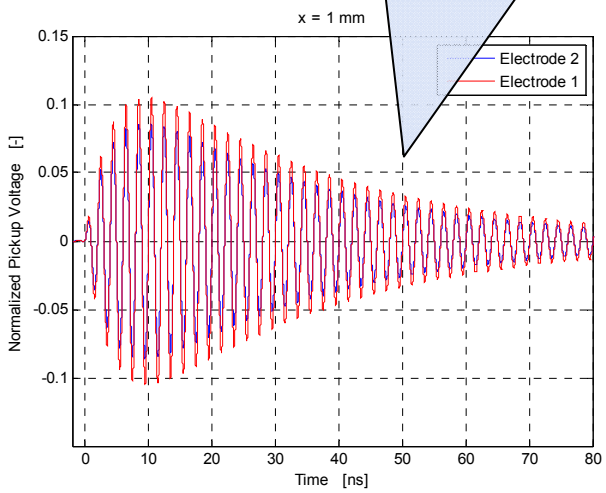
Resonant Stripline BPM: RFFE



Raw 500MHz resonant stripline signal.

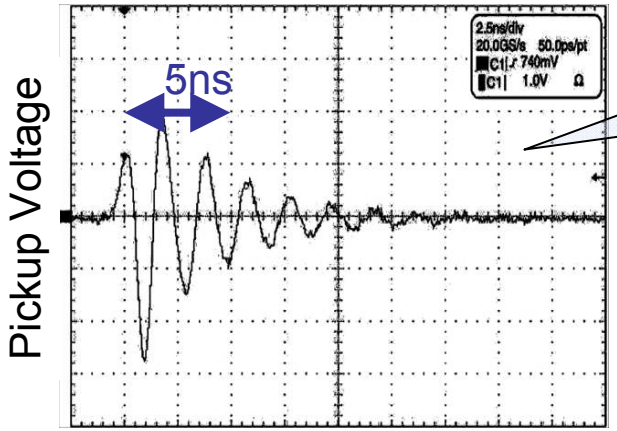


Ringing filter output: Pulse stretching improves resolution (reduces digitizer jitter impact).



Examples & Status: SwissFEL Test Inj.

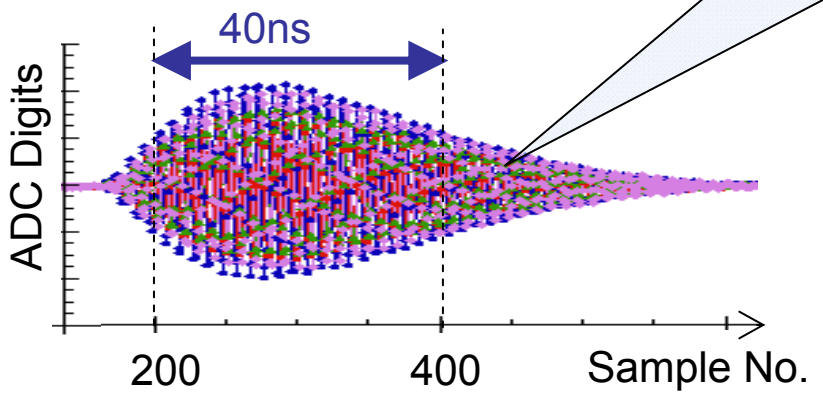
Signal Waveforms

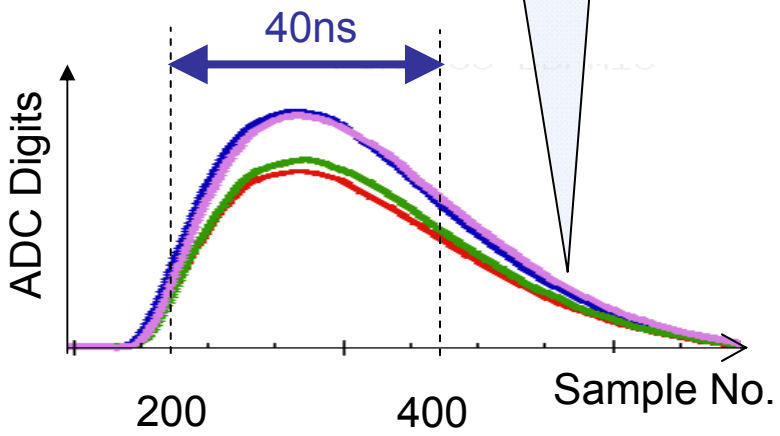


Low-passed pickup signal (scope image).

RFFE output, digitized by BPM electronics (5Gsps), after gain/offset/jitter correction & FIR filtering in FPGA.

FPGA calculates envelopes & then strip amplitudes via integrals. Auto peak search.

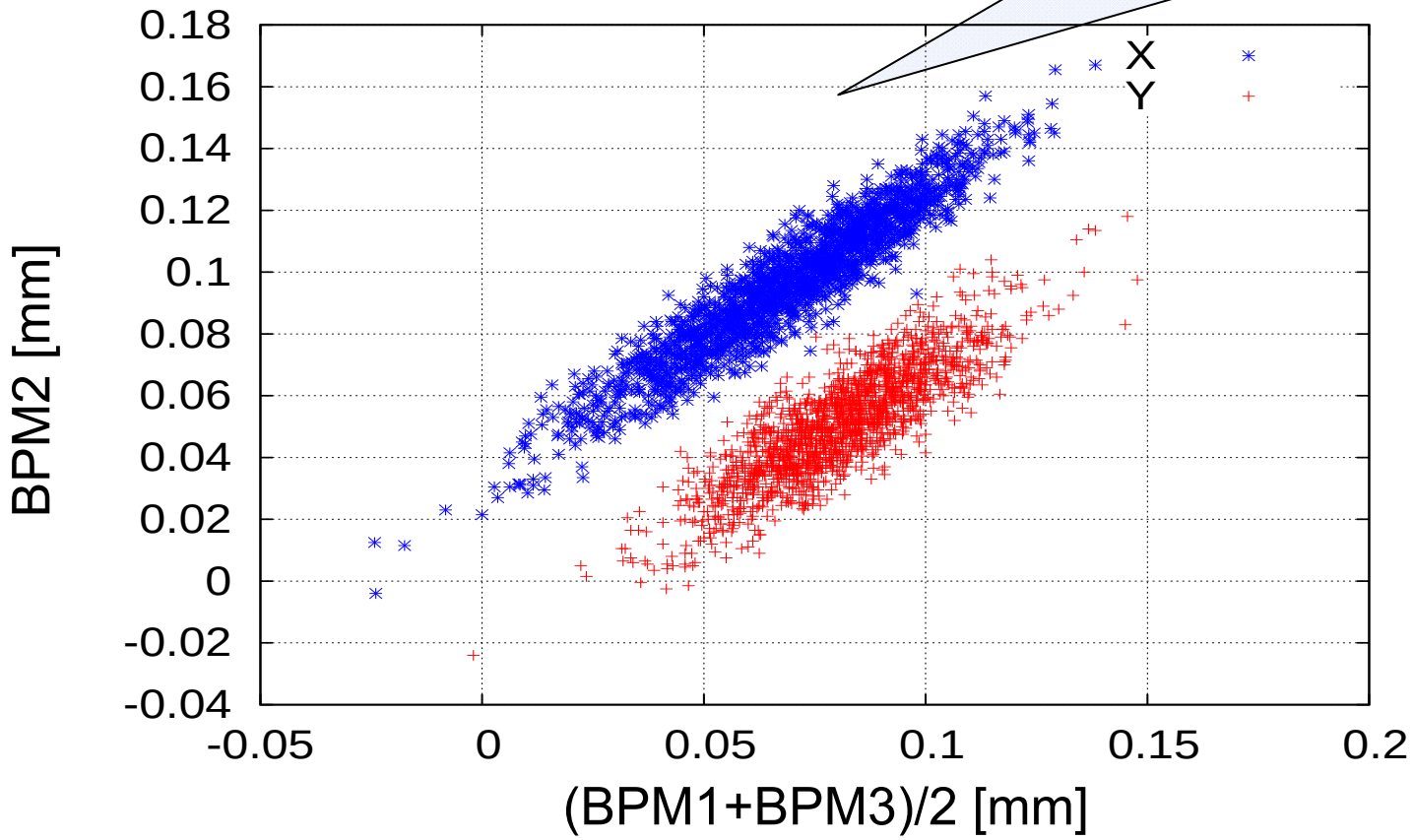




Examples & Status: SwissFEL Test Inj.

Position Resolution

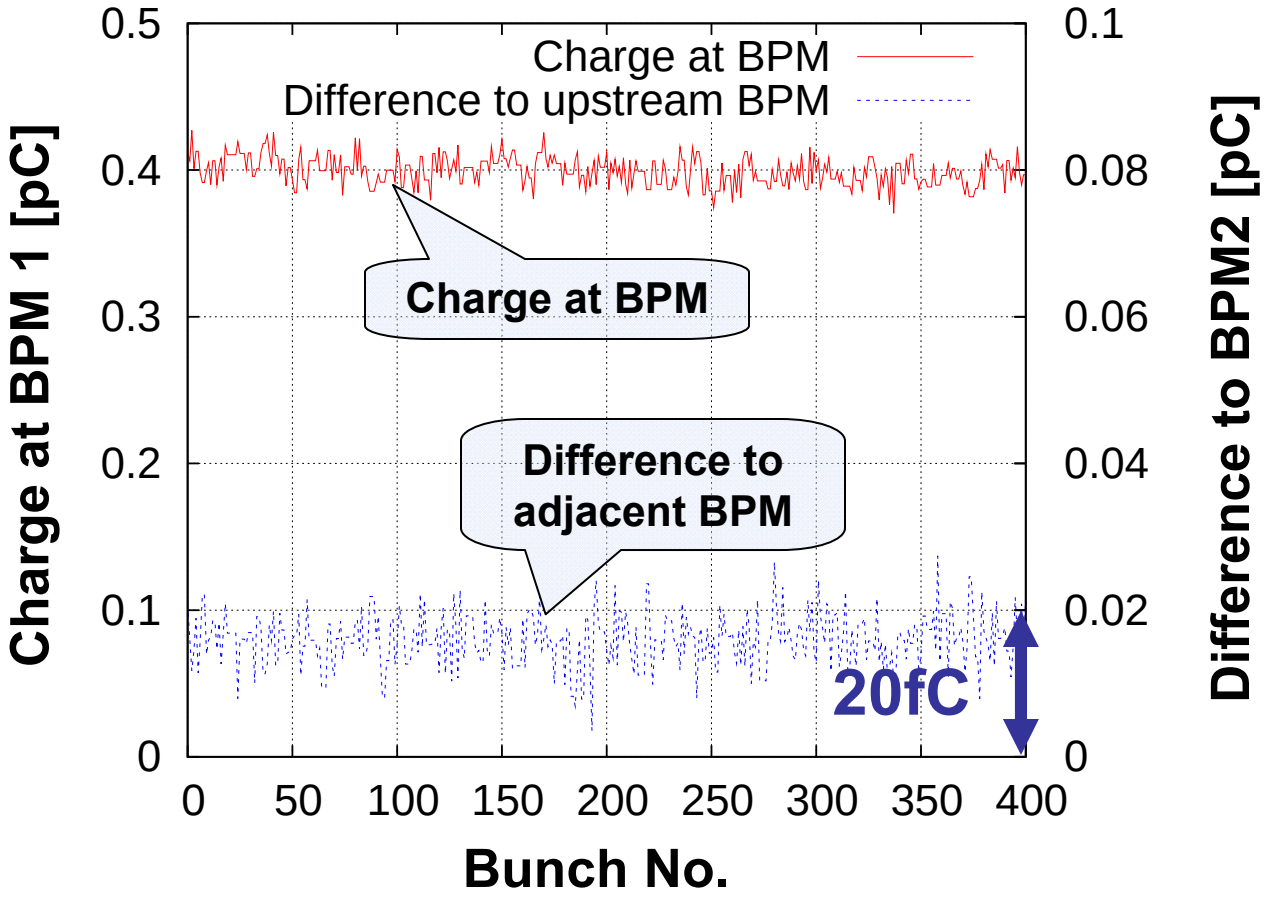
Correlation of 3 adjacent BPMs: 7µm RMS noise from 5-500pC (Required: 10µm). 16mm geometry factor.



Examples & Status: SwissFEL Test Inj.

Charge Resolution

~4fC RMS noise at 0.4pC bunch charge!

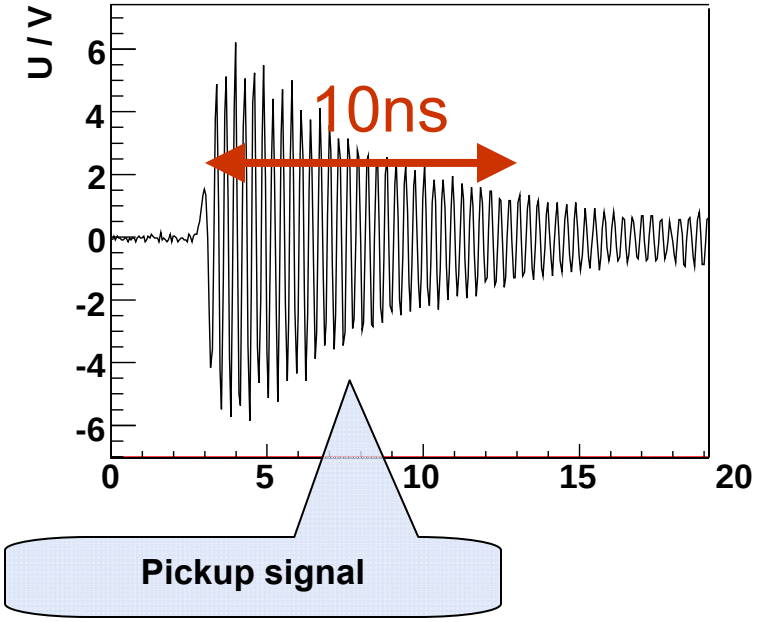


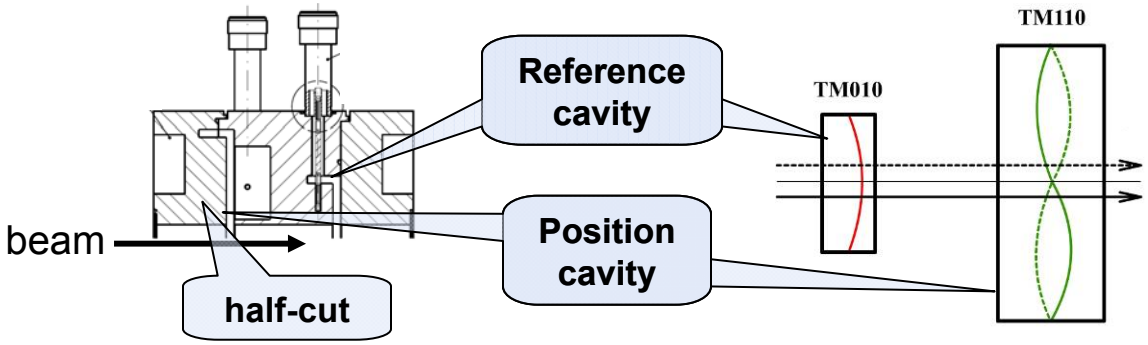
Contents

Examples & Status: E-XFEL Undulator

Undulator Cavity BPM Pickup

- Based on 4.8GHz SPring8/SCSS design.
- Adapted to E-XFEL (f=3.3GHz for both resonators, …).
- Q(loaded) = 70.



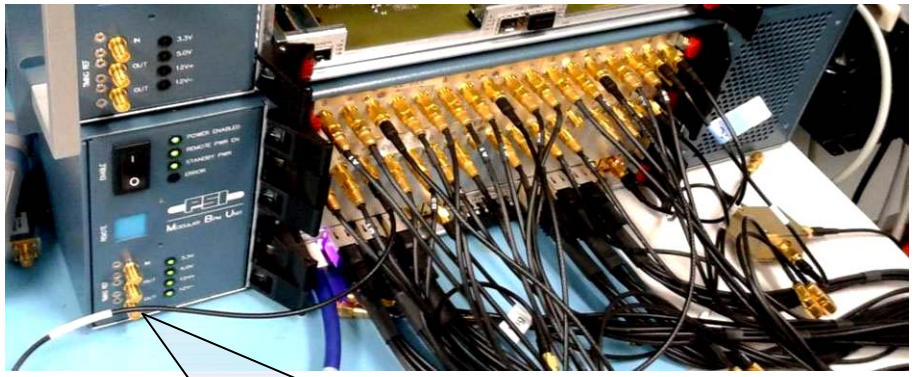


D. Lipka/DESY

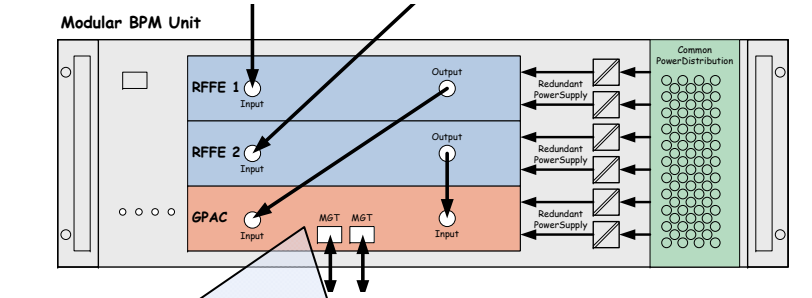
Examples & Status: E-XFEL Undulator

Modular BPM Unit ("MBU")

- Contains 4 button RF front-ends (RFFEs), or 2 cavity RFFEs, or combination.
- Common digital-back-end FPGA board (GPAC = Generic PSI ADC carrier) + two ADC mezzanines.
- No VMEbus. But: All boards also work in VME crates.

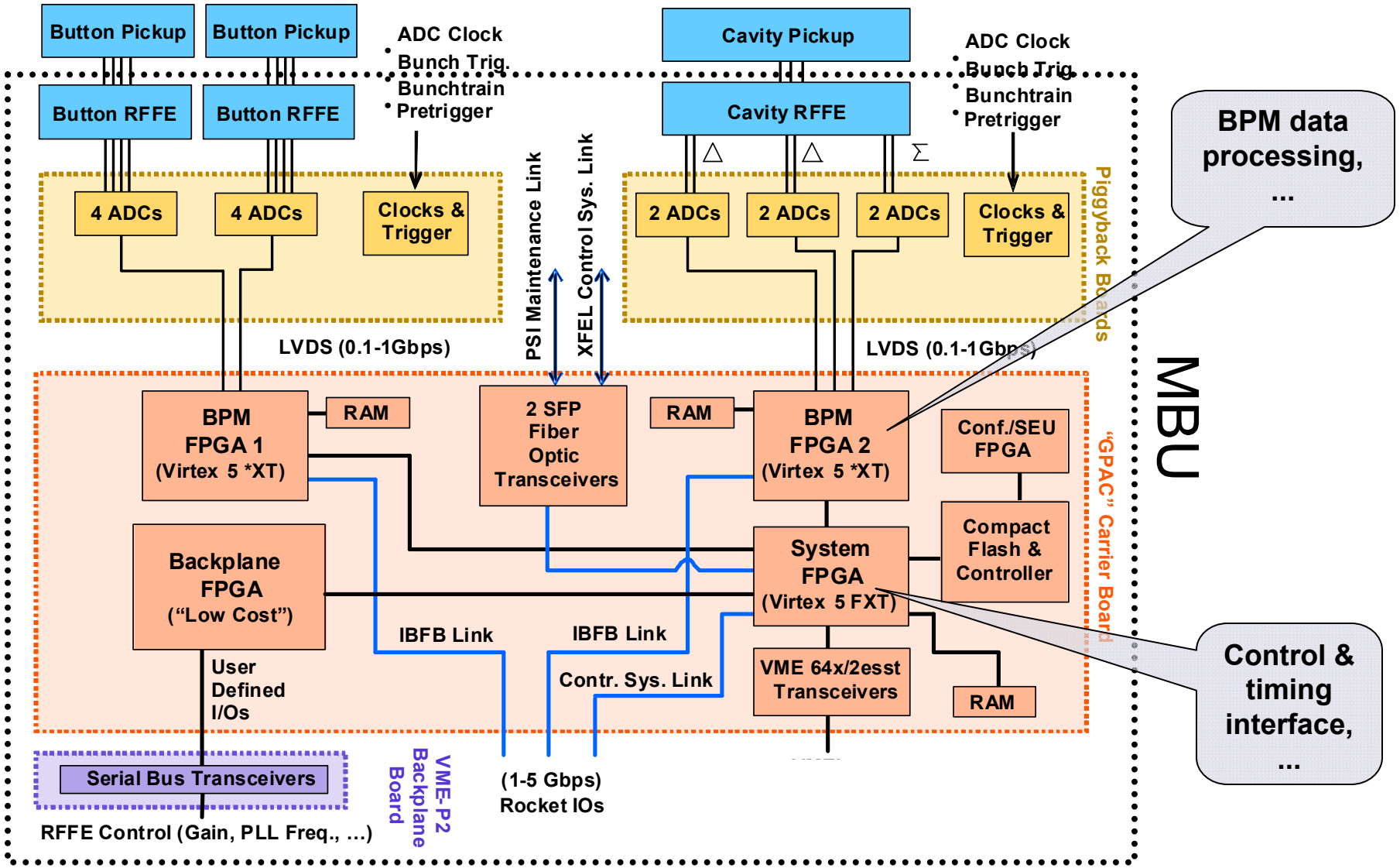


MBU for two undulator BPMs



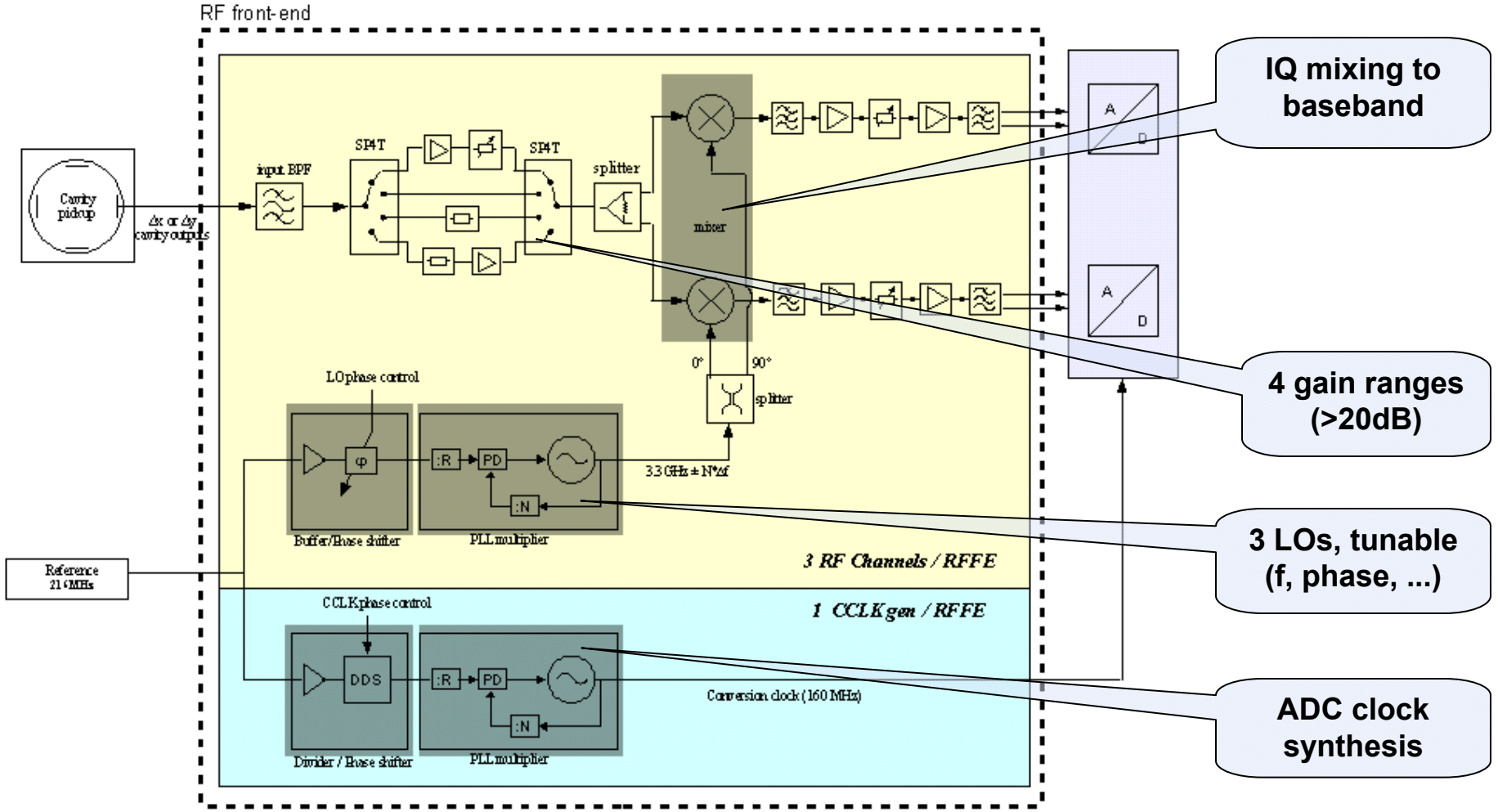
Control, timing & feedback interfaces: Multi-gigabit fiber optic links. Multi-protocol & baud rate support (PCI-e, Ethernet, …)

Examples & Status: E-XFEL Undulator



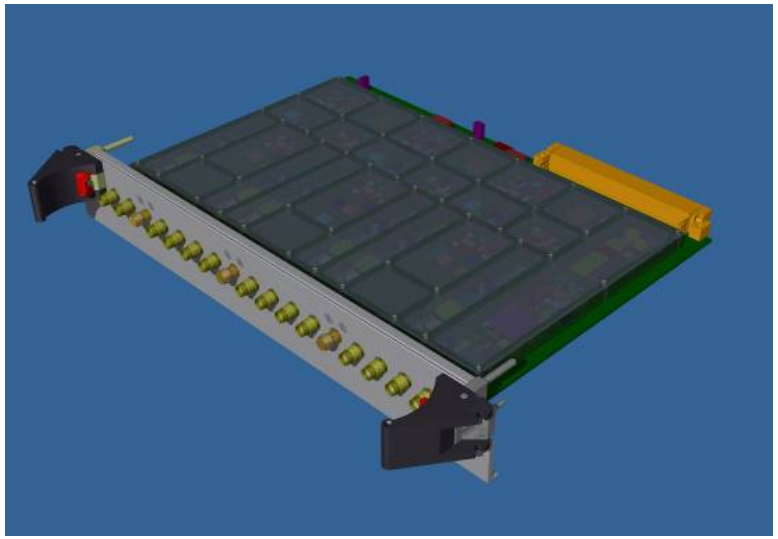
Examples & Status: E-XFEL Undulator

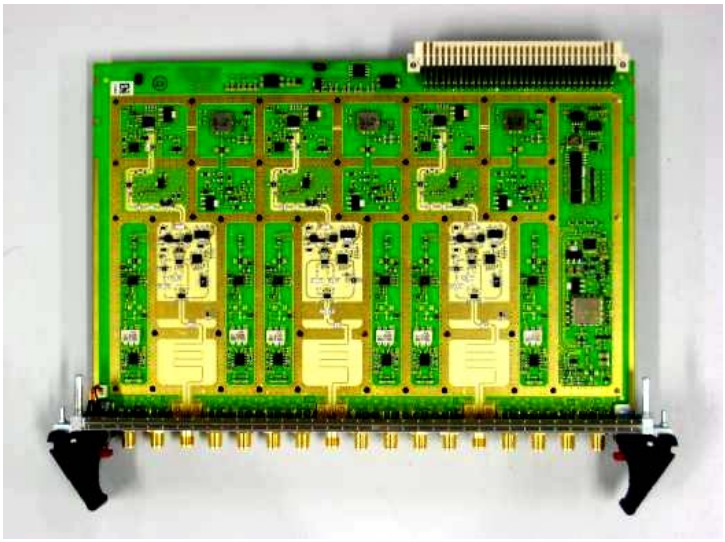
Undulator Cavity BPM RFFE



Examples & Status: E-XFEL Undulator

Undulator Cavity BPM RFFE



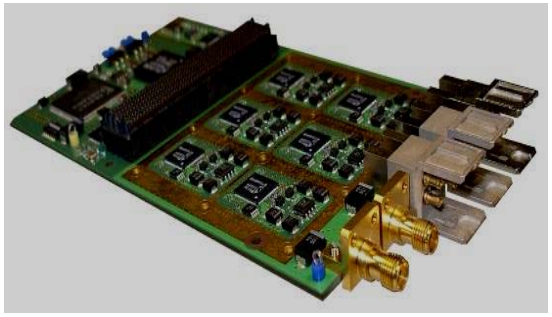
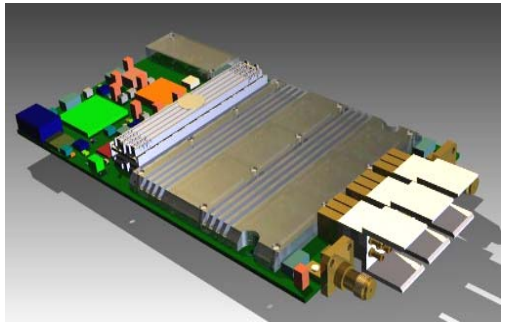
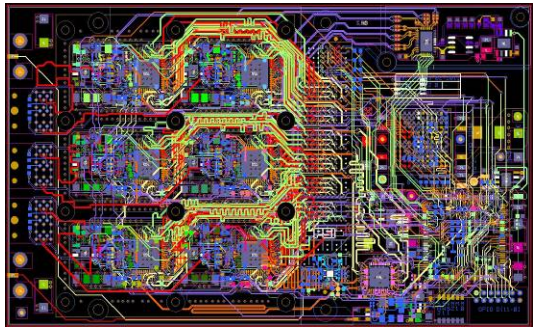


- Active temperature stabilization (several heaters & sensors) to minimize drift.
- Design of next version in progress (60dB gain range, 0.5dB steps, faster temperature regulation, ...)

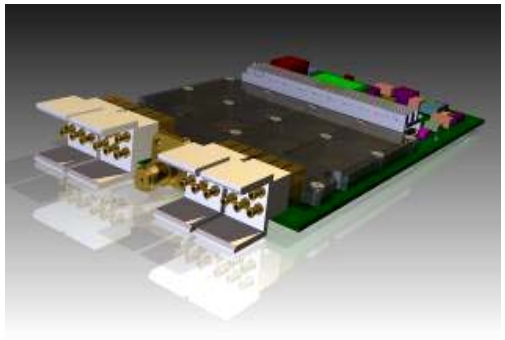
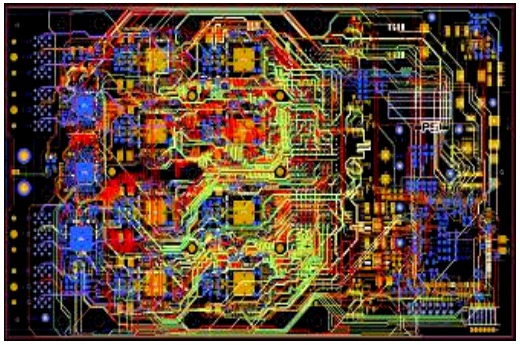
Examples & Status: E-XFEL Undulator

Undulator & Button BPM ADC Mezzanines

Cavity BPMs: 6-channel, 16-bit, 160MSamples/s.

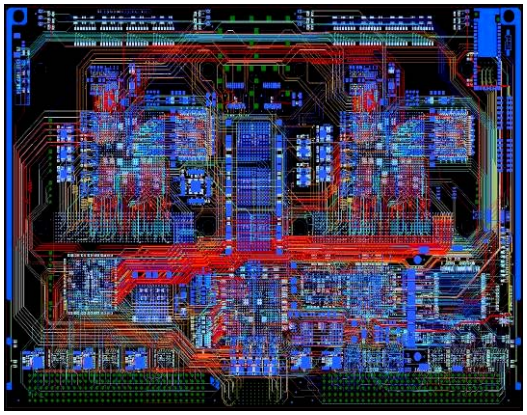
Button BPMs: 8-channel, 12-bit, 500MSamples/s.

Both types: Differential coax inputs, 150ps step clock phase adjust per ADC.

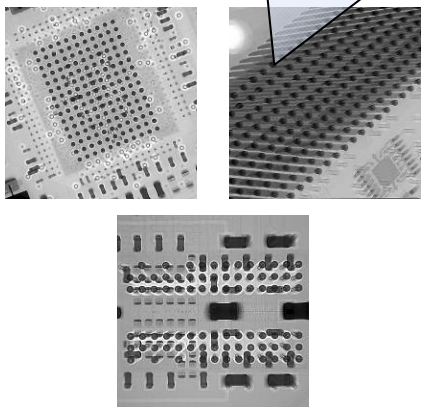
Examples & Status: E-XFEL Undulator

Digital Back-End (GPAC) FPGA Board: Hardware



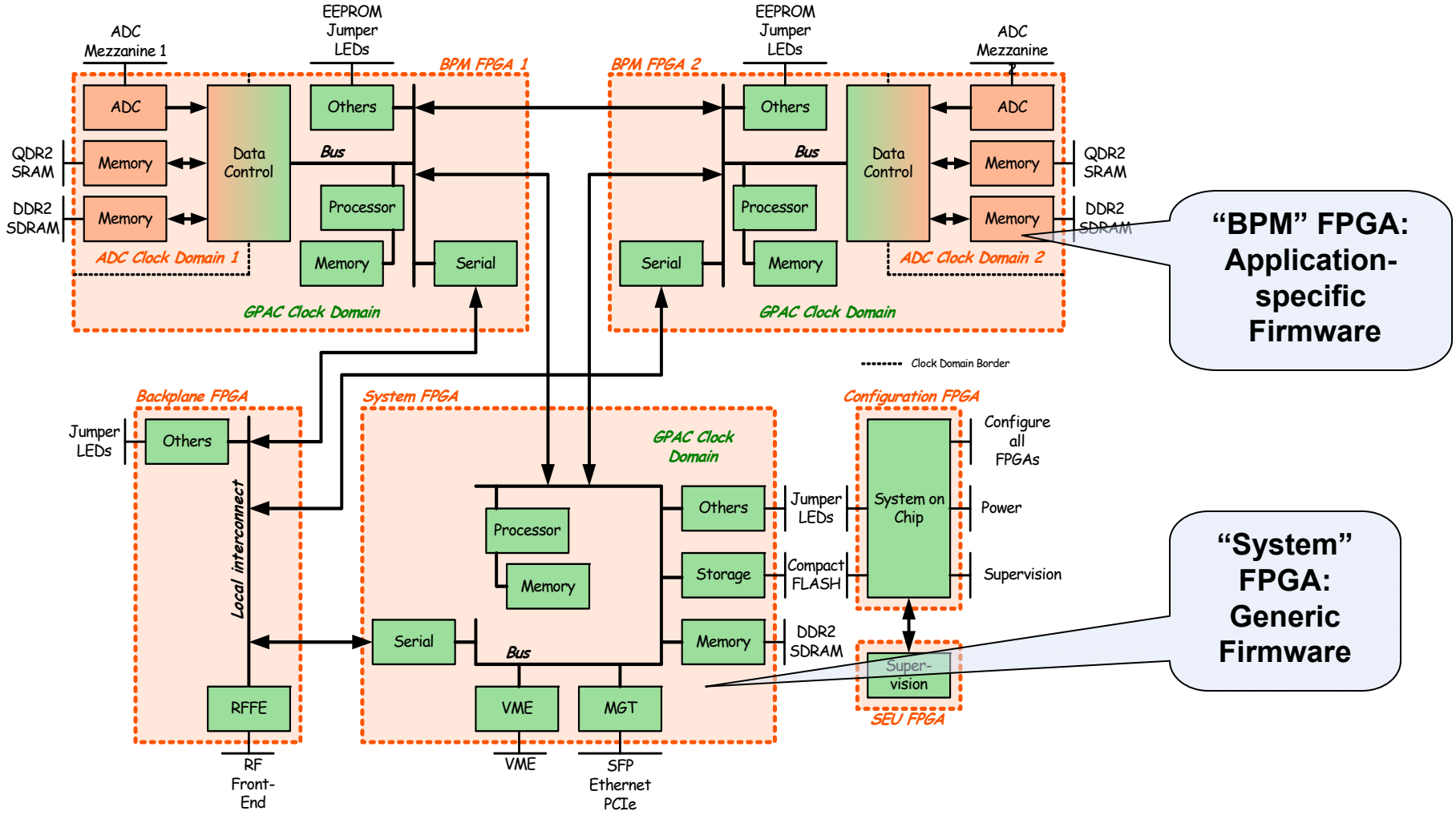
- Virtex-5 version: Ready for series production.
- But: New revision based on Artix-7 & Kintex-7 FPGAs under development. Motivation: FPGA costs (x1/3), maintenance, ...

X-ray quality control (RAMs, connector)



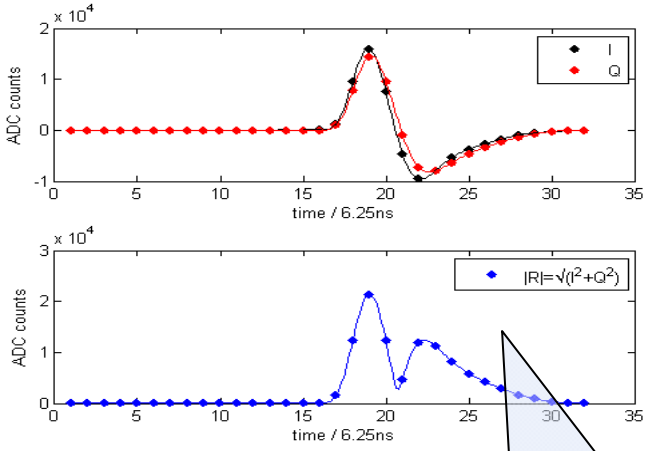
Examples & Status: E-XFEL Undulator

GPAC: FPGA Firmware/Software

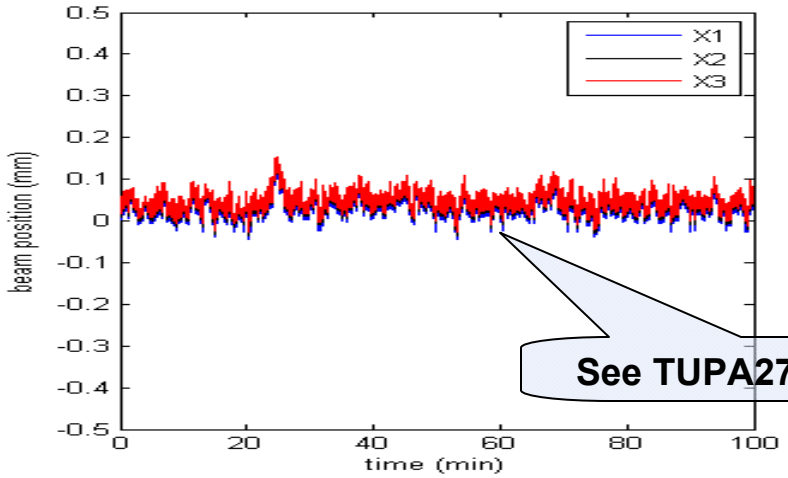


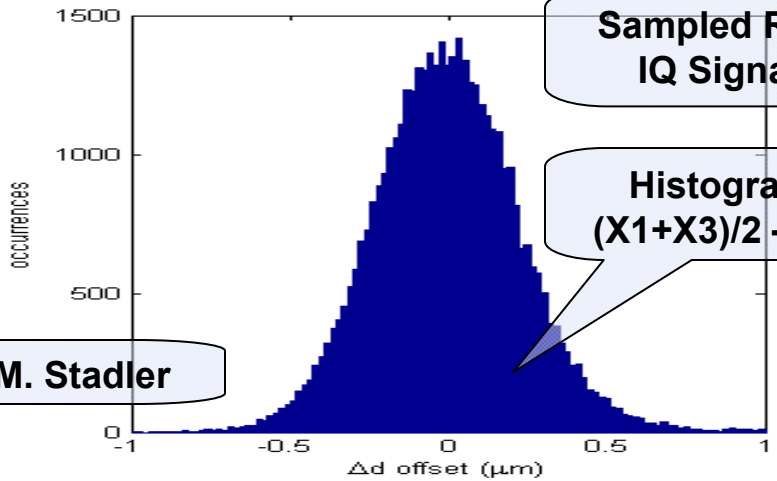
Examples & Status: E-XFEL Undulator

Correlation of 3 E-XFEL Undulator Cavity BPMs



Sampled RFFE IQ Signals





Histogram (X1+X3)/2 – X2

See TUPA27, M. Stadler

Examples & Status: E-XFEL Undulator

Correlation of 3 E-XFEL Undulator Cavity BPMs

Beam Offset (mm)	Beam Charge (pC)	Linear Meas. Range	Measured Resolution (μm RMS)
≈0.06	350	±250μm	0.12
0.1	285	±2mm	0.35
0.5	285	±2mm	0.40
1	285	±2mm	0.56
0.05	183	±500μm	0.18
0.2	2	±6.4mm	11.2

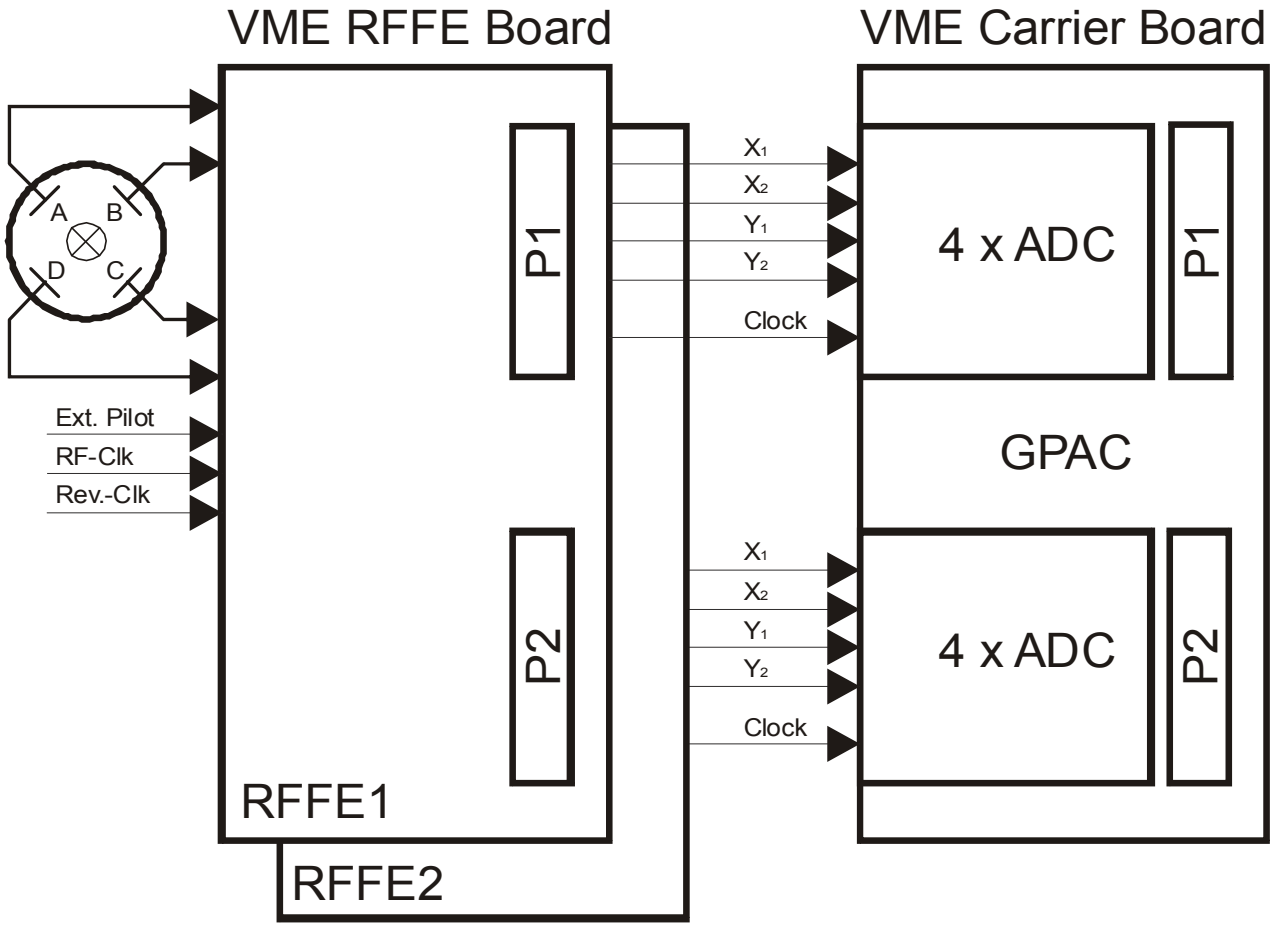
SwissFEL: Better low charge resolution with more sensitive pickup. See TUPA24 (F. Marcellini)

Meets E-XFEL resolution requirements (<1μm @ 0.1-1nC, ±0.5mm range). Long-term drift measurements to be done ...

Contents

Examples & Status: SLS Upgrade R&D

New SLS BPM Electronics: Prototype Block Schematics



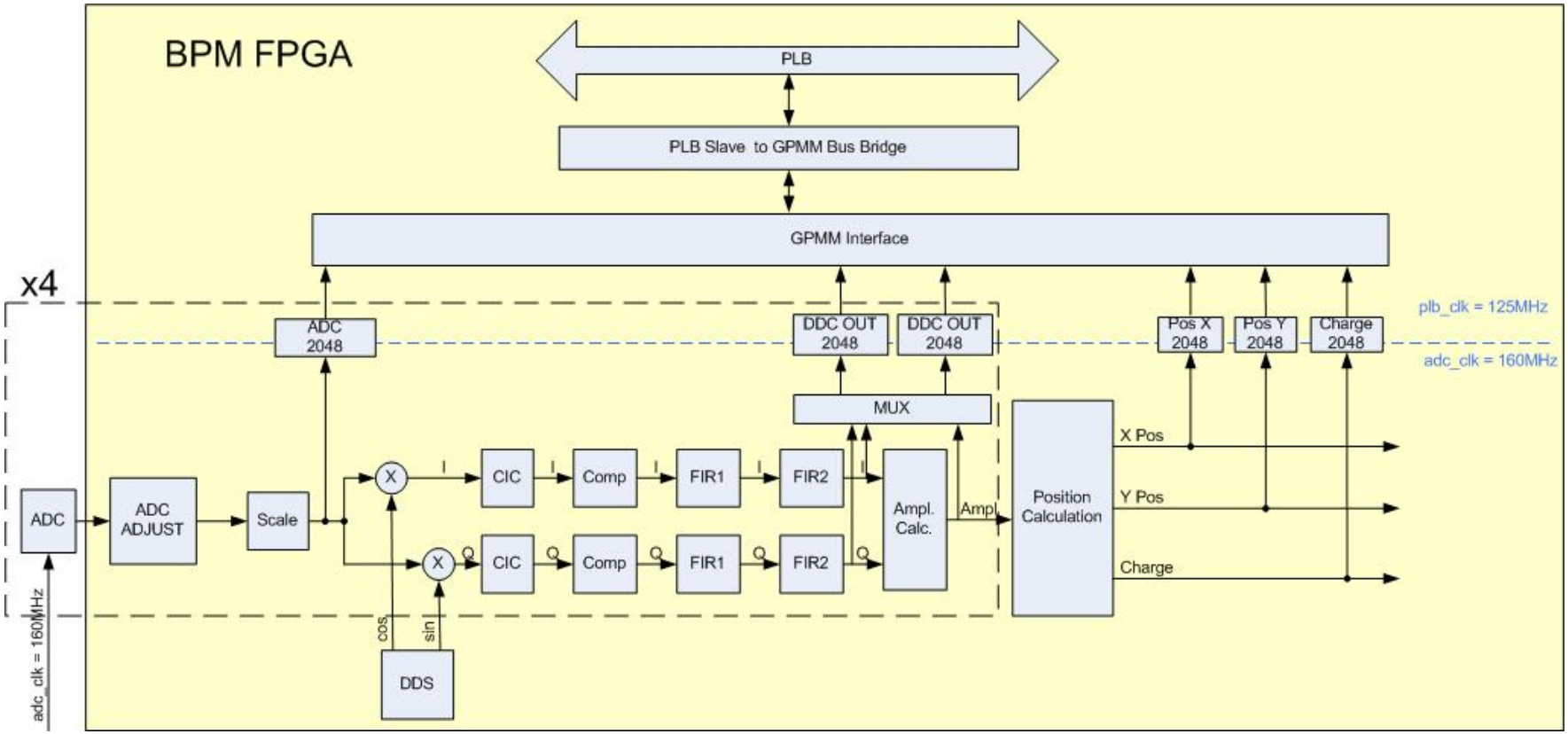
Examples & Status: SLS Upgrade R&D

Status of SLS BPM Upgrade Activities:

- FPGA Carrier Board: DDC + position calculation working. To be done: Automation (gain control, ...), feedback network interface, ...
- ADC mezzanine: Cavity BPM ADC performance seems OK for SLS. Motivation for SLS-specific ADC: Ideas to reduce jitter & simplify design, need just 4 channels, ...
- RF front-end: Tests of first dedicated RFFE in next months. So far: Used resonant stripline RFFE for test of DDC & ADC.

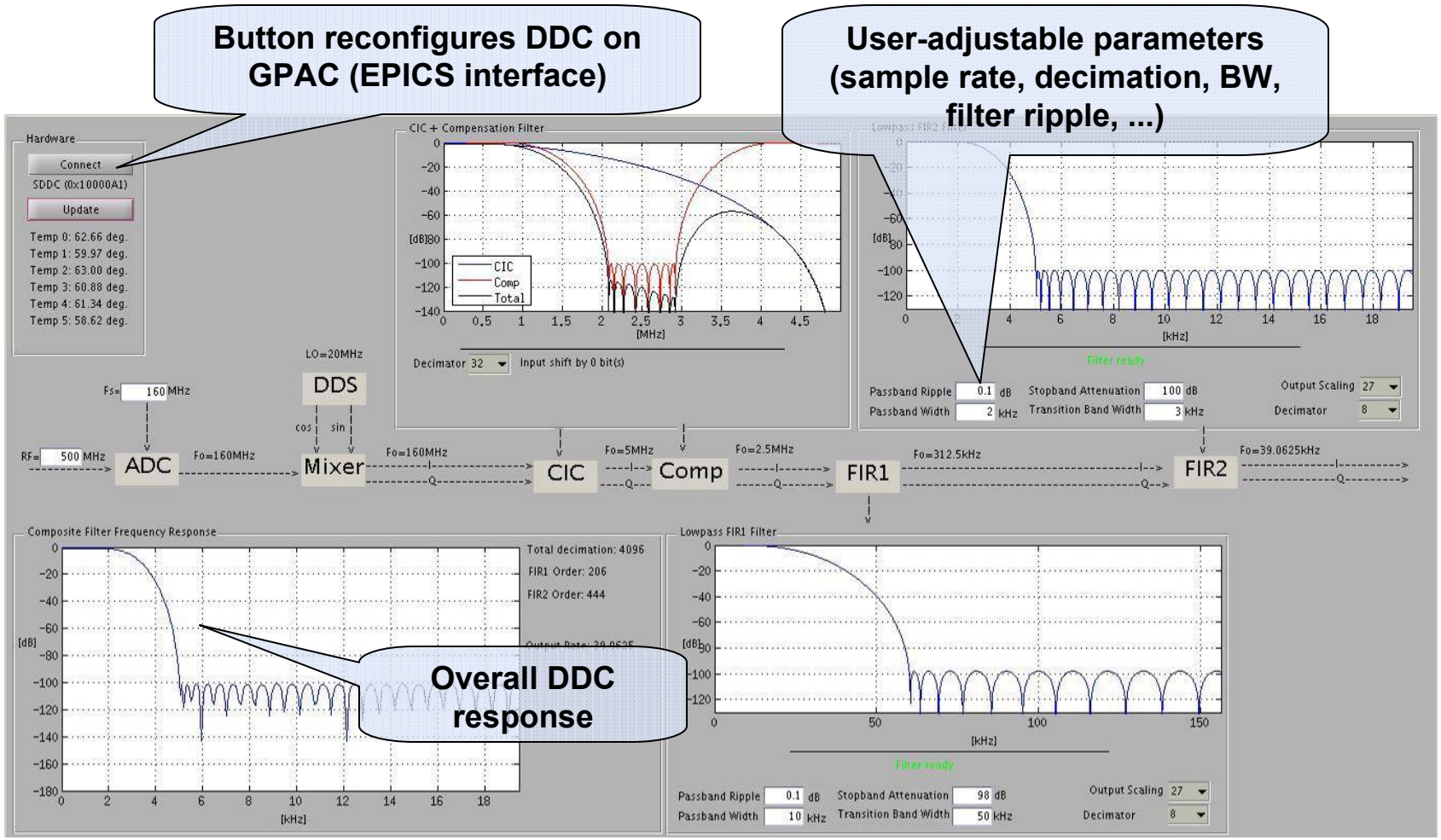
Examples & Status: SLS Upgrade R&D

New DDC: VHDL, Optimized for Speed & Space



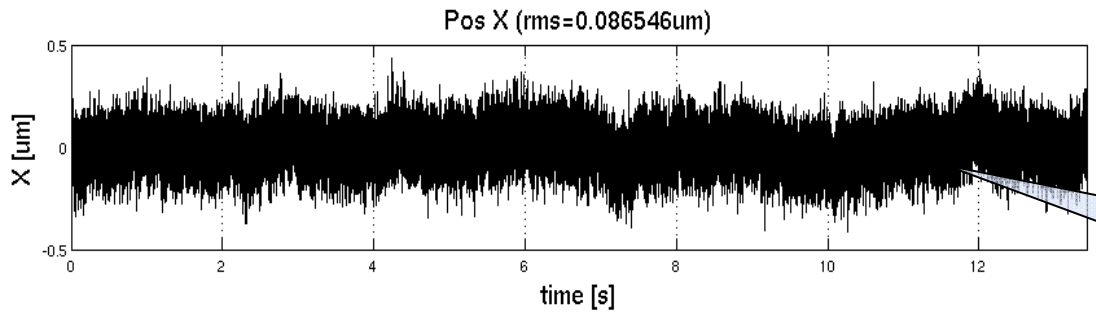
Examples & Status: SLS Upgrade R&D

GUI: Full DDC Reconfiguration During Operation



Examples & Status: SLS Upgrade R&D

DDC Test Results (Stripline RFFE + Cavity ADC + GPAC)



See TUPA26 (W. Koprek)

X: 87nm RMS (2kHz BW, 10kS/s, 10mm geometry factor, 12s)

Y: 76nm RMS (2kHz BW, 10kS/s, 10mm geometry factor, 12s)

- Results promising: RFFE + ADC were not made for SLS but FEL. But: Stripline RFFE not designed for low drift → want dedicated low-drift RFFE.

Contents

Summary & Outlook

- SwissFEL Test Injector: 10Hz single-bunch operation & analog 5Gsps waveform sampler allowed to re-use Gen1 FPGA board with slow interfaces (will not be used for SwissFEL ...).
- E-XFEL: 5MHz bunch rep. rate & submicron resolution needed new electronics, will also be used for SwissFEL (with few adaptations). Resolution for E-XFEL O.K., drift to be measured.
- SLS BPM Upgrade: Lower priority than FEL BPMs. So far mainly firmware development & resolution R&D. Want new RFFE & ADC. Time scale for upgrade depends on FEL work load ... So far MTBF of present SLS system still excellent, no complaints from users. Would like to do upgrade before that changes ...
- In-house design of SLS & FEL BPM systems: Many synergies, also with non-BPM systems.

Paul Scherrer Institut

PSI

Thank you for your attention!

PSI Team & Credits

E-XFEL/SwissFEL BPM Electronics:
Raphael Baldinger (Electronics Tech.)
Robin Ditter (Electronics Tech.)
Waldemar Koprek (Firmware/Software Engineer) →TUPA26
Reinhold Kramert (Electronics Eng., MBU)
Goran Marinkovic (Firmware/Software Engineer)
Markus Roggli (Electronics Eng., ADCs)
Markus Stadler (RF Engineer, Cavity Electronics) →TUPA27
Daniel Treyer (RF Engineer, Button & Stripline Electronics)

SwissFEL BPM Pickups:
Fabio Marcellini (RF Engineer, Cavity BPMs) →TUPA24
Martin Rohrer (Mech. Engineer)
Micha Dehler (RF Engineer, Resonant Stripline)
Alessandro Citterio (RF Group, Resonant Stripline)

And:
Thanks also to Volker Schlott & SER, support from other PSI/GFA groups, DESY E-XFEL diagnostics team (E-XFEL pickups) & Claire Simon/CEA (re-entrant E-XFEL BPM pickup & RFFE).

Supplementary Slides …

PSI BPM Electronics Generations

Motivation for Modular RFFE/ADC/Back-End Concept with Generic & Separated ADC & Back-End Boards

- Use FPGA back-end & ADCs for non-BPM applications. Examples:
  - SwissFEL Beam Arrival Time Monitor (Prototype Under Commiss.)
  - SwissFEL Bunching Monitor (Prototype Operational)
- Decoupling of developments (work, risk, bugs): Boards can be developed & tested independently.
- Long-term maintenance & upgrade: Boards can be upgraded independently.
- Saves work: Develop complex FPGA board once, then combine with different (simpler) ADC mezzanines & RFFEs (or vice versa).

PSI BPM Electronics Generations

Evolution of Digital Back-End: Interfaces & Processor

Gene-ration	Final Application	Ether-net / Pie Speed [Gaps]	Multi-Gigabit Serial Links to External Connectors & SFP(+)	PSI Timing Interface / Any Baud Rate Supported	On Board Pro-cessor / Linux
0	SLS	-	-	-	-
1	Cyclotron SwissFEL TI	- -	2x2.1Gbps	Y / -	Y / -
2	FLASH-II E-XFEL	1/2.5	26x5Gbps	Y / Y	Y / Y
2.1	SwissFEL SLS	1-10/5	22x5Gbps + 4x10Gbps		

10G Ethernet, PCI Express Gen2. Use of VME is optional, boards work also standalone ...

For timing, feedback, control system interface, ... Protocol determined by firmware.

PSI BPM Electronics Generations

Evolution of Digital Back-End: Memory

Back-End Gene-ration	Final Application	External FPGA RAM		Non-Volatile Configuration & Hard-Disk Memory
		Σ Size [Byte] (RAM Type)	Σ Bandwidth [Byte/s]	
0	SLS	<100k (FIFO)	...	EEPROM
1	Cyclotron SwissFEL TI	4M (ZBT)	1G	Compact FLASH
2	FLASH-II E-XFEL	16M & 256M (QDR2 & DDR2)	4+4G (R+W) & 4G	Compact FLASH
2.1	SwissFEL SLS	5G (DDR3)	20G	used Card

DRAM: Max. theoretical value. Real value application-dependent.

Examples & Status: SwissFEL Test Inj.

Choice of BPM & Electronics Type

Goal: Want "robust" standard BPM.

- Moderate resolution: ~10µm.
- Large position & charge range: ±10mm, 10-200pC.
- Needed ~20 BPM working 9/2010 (too early to use E-XFEL designs …).

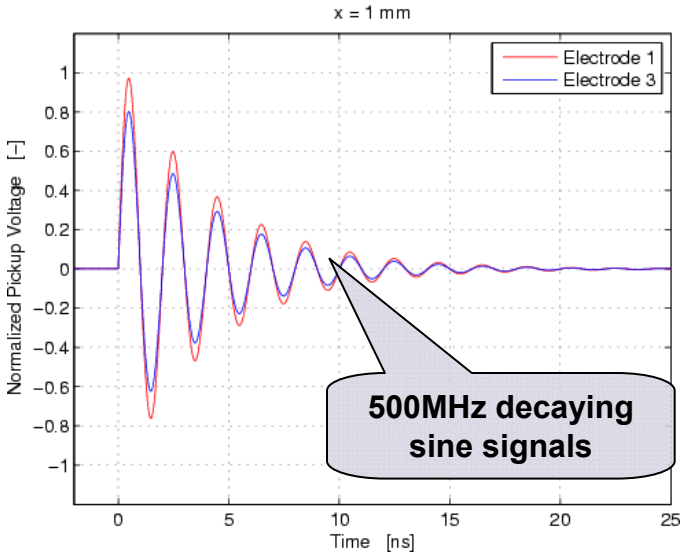
Solution: Re-use/modify existing PSI pickup & electronics

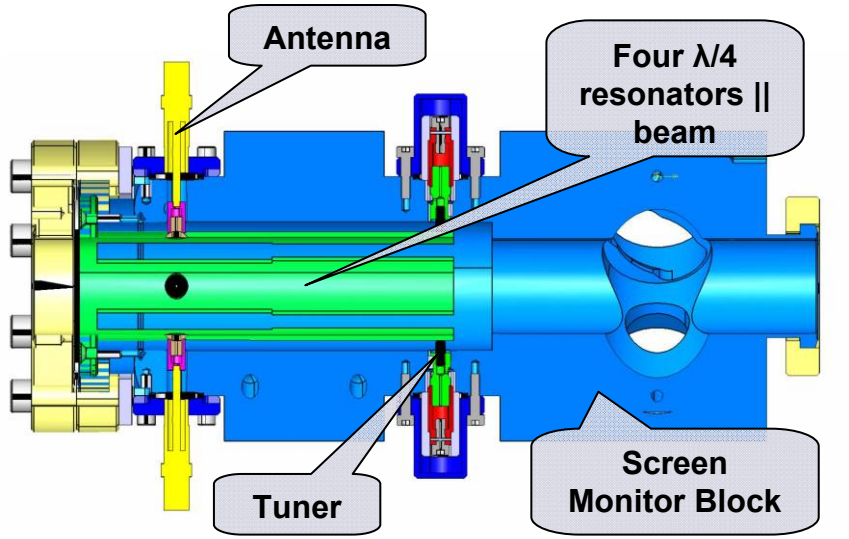
- Pickup = 500MHz resonant stripline (used in SLS linac).
- Electronics = 5GSPS digitizer mezzanine + generic "VPC" FPGA carrier board (modified PSI muon detector digitizer).

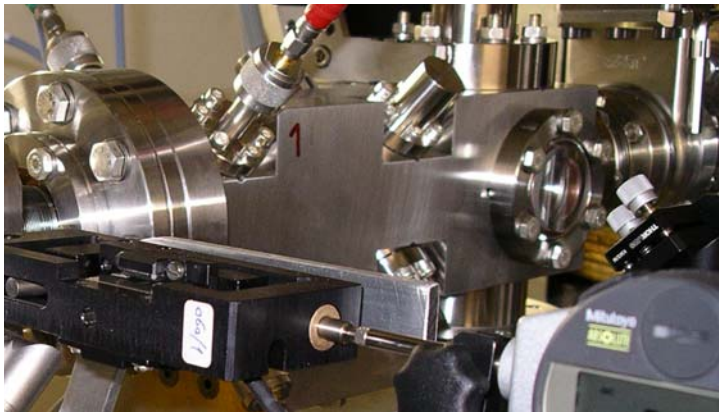
Examples & Status: SwissFEL Test Inj.

Resonant Stripline Pickup

- Already used in SLS linac & transfer lines.
- Optimized for SwissFEL test injector: frequencies, tuners, tolerances, ...







Examples & Status: E-XFEL Undulator

BPM Performance Requirements

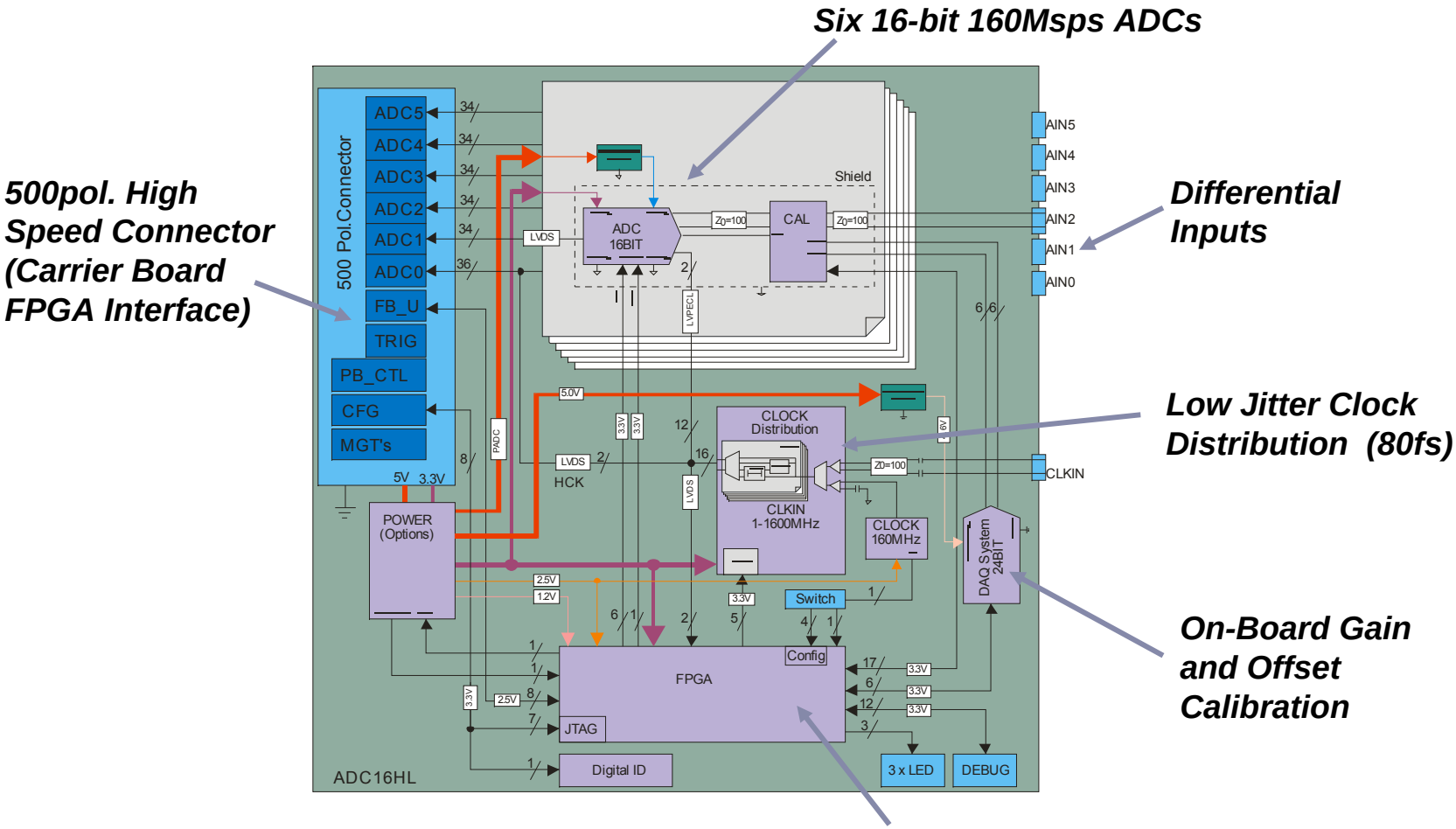
- Table from BPM CDR 2010. Preliminary (length, quantities, …).
- Most values from beam dynamics work package (Decking et al.).

	Type	Quantity	Beam Pipe Diameter	Vacuum length	Single Bunch RMS Resolution	Averaged RMS Resolution over 1000 bunches of identiccal trains	Drift per 1 deg C, min 0.1 µm	Operation range for maximum resolution	Operation range providing reasonable signal	Linearity	x/y Crosstalk	Charge Dependence (dQ=10%)	Bunch to Bunch Crosstalk	Transverse Alignment Tolerance (RMS)	Pipeline Latency
			mm	mm	µm	µm	µm	mm	mm	%	%	µm	µm	µm	ms
Cold BPM	Button/Re-entrant	102	78	170	50	10	10	± 3.0	± 10	10	1	50	10	300	10
Gun BPM	Button	3	40.5	100	100	10	10	± 3.0	± 10	5	1	100	10	200	10
Standard BPM	Button	219	40.5	200/ 100[1]	50	10	10	± 3.0	± 10	5	1	50	10	200	10
Standard BPM	Button	6	100	200	100	10	10	± 5.0	± 20	10	1	100	10	200	10
Cavity BPM Beam Transfer Line	Cavity	12	40.5	255	10	1	1	± 1.0	± 2	2	1	10	1	200	10
Cavity BPM Undulator	Cavity	117	10	100	1	0.1	1	± 0.5	± 2	2	1	1	0.1	50	10

[1] **Warm button: Flanged version & welded version (where flanged is too long)**

Examples & Status: E-XFEL Undulator

E-XFEL Cavity BPM ADC Mezzanine



Examples & Status: SLS Upgrade R&D

Motivation For SLS BPM In-House Design

- Estimate: Less expensive (incl. man power) compared to commercial solution.
- Synergies SLS ↔ E-XFEL / SwissFEL: Less man power for development & long-term maintenance.
- No “black box”. All documentation (source codes, board schematics, …) available. Reduces time & costs to integrate systems, fix problems, add new features. Ensures high SLS availability / uptime.
- Avoids dependence on companies.

Examples & Status: SLS Upgrade R&D

SLS Features Affecting BPM Requirements

- Global Fast orbit feedback (FOFB):
  → Any drift & noise of BPM electronics & pickups immediately modulated onto beam (if within FB bandwidth & if no X-ray BPM feedback).

- Top-up operation: I=400mA ± ~1%
  → Beam-current dependence of BPMs less critical.

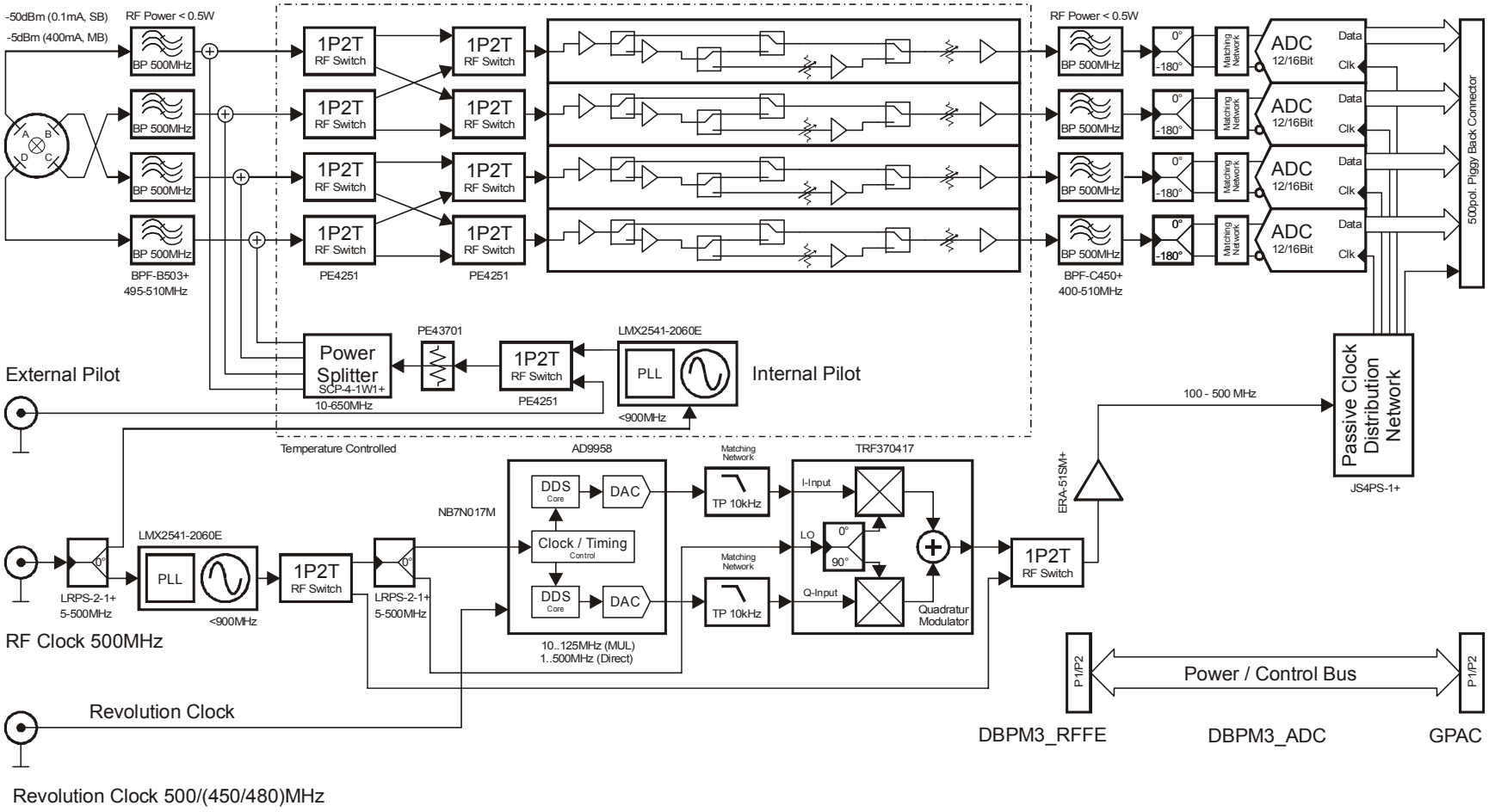
- Filling pattern feedback (keeps charge in bunches 0...N const.)
  → Filling pattern dependence of BPMs less critical.

- X-Ray BPM feedbacks (correction ~ Hz, move FOFB ref. orbit)
  → Position drift of RF BPMs less critical.

Accelerator design & features important for orbit stability, not only pure BPM system performance.

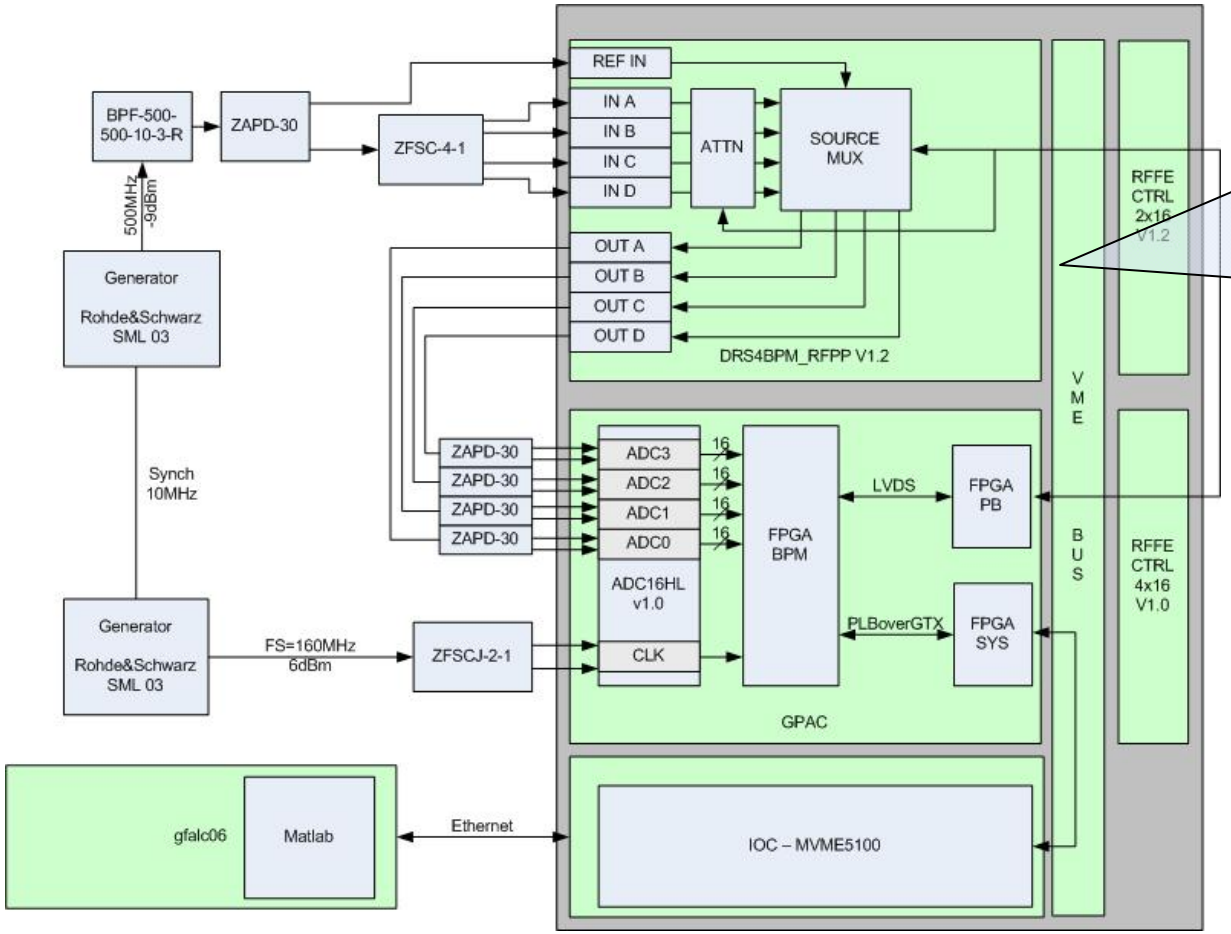
Examples & Status: SLS Upgrade R&D

New SLS BPM RF Front-End: Block Schematics



Examples & Status: SLS Upgrade R&D

Lab Test Setup For DDC Tests



PSI modular BPM electronics: Using SwissFEL test injector 500MHz resonant stripline RFFE & E-XFEL cavity BPM ADC for tests (DDC, ...), until dedicated new SLS ADC & RFFE are ready.