# DESIGN OF RF FRONT END FOR CAVITY BEAM POSITION MONITOR BASED ON ICS*

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*Abstract*

RF front end has the significant impact on the performance of cavity beam position monitor (CBPM) which is indispensable beam instrumentation component in free electron laser (FEL) or linear collider facility. With many new advances in data converter and radio technology, complex RF front end design has been greatly simplified. Now a based digital intermediate frequency (IF) receiver architecture RF front end for CBPM has been designed by using surface mount components on print circuit board (PCB). The front end contains analog-digital converter used to digitize the IF signals. The whole system would be integrated to a digital board developed by our lab to produce the dedicated signal processor for CBPM. There is a Xilinx Vertex-5 FPGA device on the digital board and relevant signal processing algorithm has been implemented on it using VHDL. The details about design would be introduced blow.

## INTRODUTION

CBPM is a key beam instrumentation component only which could reach sub micron or nano resolution in all beam position measure solutions[1][7][8][10]. So it was seen as a necessary solution to measure beam position in the long undulator section of shanghai soft X ray FEL facility[2] which is on the way. Nowadays, CBPM signal processing system is on the stage of development and some preliminary system hardware frame has been completed, and relevant offline signal algorithms also have been verified and implemented in Matlab[4]. The whole system hardware frame contains RF front end accomplished by using microwave connectors and high speed ADC board integrated digital signal processing chip-FPGA on which the online algorithm was implemented. It also makes pulse-by-pulse position measurement come true. Some bench test results have been acquired. But in the aspect of system integration and cost, the current system did not behave well. So taking all the elements into account we decided to develop the new RF front end by using surface mounted components on the PCB. Also the RF front end, including the RF signal conditioning module and ADC module, by using high speed connectors, was integrated into a digital board which consists of Vetex 5 FPGA chip and ARM signal board computer[3]. So the dedicated and high integration level signal processor for CBPM may replace the previous system as results of cost saving.

* Work supported by National Natural Science Fundation of China (11075198)

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## LAYOUT DESIGN

The RF front end topology used a single stage three channels digital IF receiver architecture[9] which contains three sections: an RF signal conditioning module, a based phase locked loop (PLL) LO and ADC module. Figure 1 shows the schematic of RF front end.

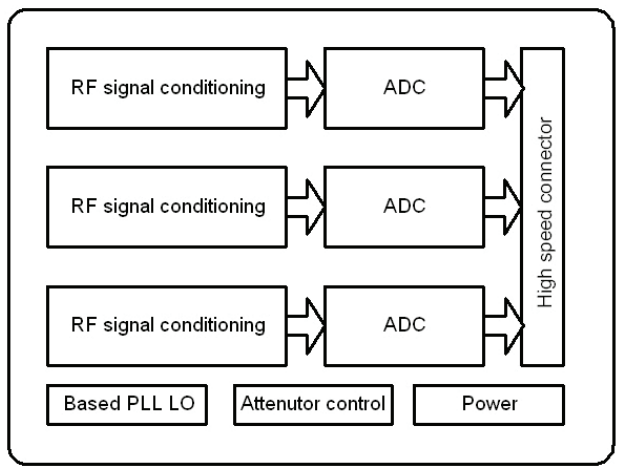


Figure 1: Schematic of RF front end.

In the signal conditioning module, the output signal of CBPM must enter into band pass filter to eliminate interference from other resonant mode. But surface mounted band pass filter was not chose in our design since its characteristic of stop band attenuation could not meet CBPM requirement of high quality factor [4]. So a connector of resonant cavity BPF was also needed prior to the board level RF front end.

## RF CONDITIONING

The function of RF signal conditioning module is to downconverted RF signals to IF signals which could be digitized by some high precision ADC. Details about signal conditioning module were shown in Figure 2.

Considering the protection of amplifier against high power surges, we chose a limiter prior to the amplifier as its maximum input power is about 11dBm. And then RF signals were first amplified by low noise amplifier (LNA) of 16dB gain. A digital attenuator was used to adjust the signal intensity and make the RF channels compatible to high Q and low Q cavity. A mixer converted the RF signals down to 20MHz IF signals. A 22MHz cutoff low



ISBN 978-3-95450-119-9

pass filter (LPF) was used to remove high order harmonics in the process of frequency conversion. Before the IF signals was digitized, IF amplifier must be used to improve the signal intensity to match the ADC input requirement and make it work in the optimal circumstance. As the 1 dB output compression point of the IF amplifier was 21.5dBm, more than the maximum input level of ADC, Pi attenuator was added to readjust the signal intensity. Harmonics generated by the IF amplifier was suppressed by the last LPF, which has the function of anti aliasing.

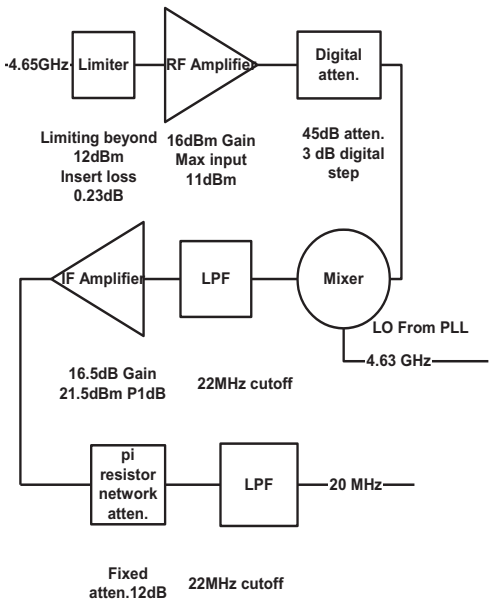


Figure 2: Electronics of RF signal conditioning module.

The LPFs have different frequency cutoff for the same package, such 30MHz and 40MHz. So we could flexibly change the LPFs to subject to the high Q or low Q cavity.

Based on .s2p files of all the components from corporations, we did some simulations about gain budget and noise figure. Figure 3 illuminates gain budget of RF channel.

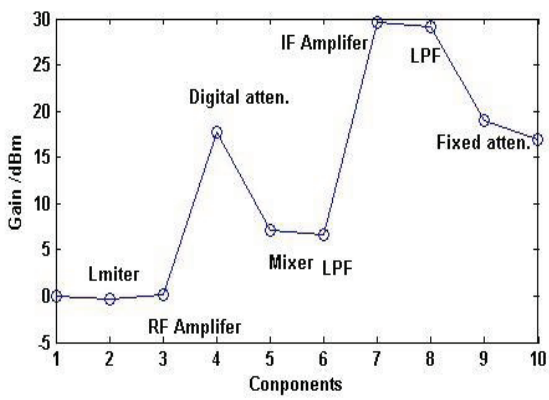


Figure 3: Gain budget of RF channel.

In the simulation, we acquired 17dB RF gain, and by using the digital attenuator we could get dynamic range from 0dB to 45dB. Noise figure simulation was shown in Table 1. Noise figure is 7.364dB.

Table 1: Noise Figure Simulation

| Components | Comp_NF(dB) | NF_chan(dB) |
|---|---|---|
| Limiter | 0.230 | 0.230 |
| RF amplifier | 2.500 | 2.730 |
| Digital atten. | 2.500 | 2.777 |
| Mixer | 6.500 | 6.147 |
| LPF | 0.900 | 6.164 |
| IF amplifier | 5.000 | 7.087 |
| LPF | 0.900 | 7.088 |
| Fixed atten. | 12.000 | 7.364 |

## ADC AND PLL

The IF signals from RF channel were sent to ADC module, which could reach 125MSPS sampling rate and 16 bit precision. The ADC module adopted different pair transmission line to transmit digital signals so as to avoid interference from common mode signals and be immune to external EMI. And then digital signals were transmitted to a digital board which was developed by our lab. The single board was demonstrated in Figure 4[3]. The Xlinx Vertex 5, as the key digital signal processing device on the board, extended memories, clock, trigger etc. Samsung's S3C6410 based ARM11 core[6] was used as embedded controller on the board so as to implement data access. The controller also extended 100M Ethernet used to build up distributed industrial Ethernet. The processor could implant based linux kernel embedded operation system. So based EPICS embedded control system come true.

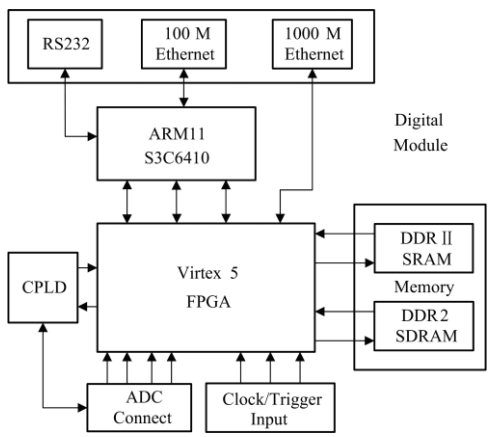


Figure 4: Digital board.



ISBN 978-3-95450-119-9

By using the connectors, we could integrate RF front end on the digital board to build up a dedicated CBPM signal processor.

In order to achieve phase synchronization with beam, we utilized PLL to generate LO which can be locked to 119 MHz facility timing reference. Details about the PLL module was shown in Figure 5.

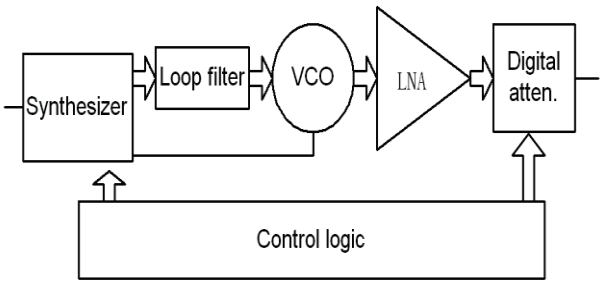


Figure 5: PLL module.

In our design, we employ a integer architecture synthesizer which made the 119MHz timing reference divided by 119, the PFD frequency reference is 1MHz. our LO goal is 4630MHz, So 4630MHz output of VCO was fed back to the synthesizer, and then divided by 4630 to implement phase locked. 100 KHz bandwidth of loop filter was chose so as to achieve short lock time.

Phase noise, a measurement of the purity of the LO, is the single most critical specification in the LO section with a direct bearing on RF front end sensitivity. The phase noise of PLL module can be described roughly as Equation 1[5].

$$PN_{TOTAL} = PN_{SYSNTH} + 20\log N + 10\log f_{PFD} \quad (1)$$

Where $PN_{TOTAL}$ is the total phase noise of the PLL, $PN_{SYSNTH}$ is the phase noise due to the PLL synthesizer circuit itself, $20logN$ is the increase of phase noise due to the frequency magnification associated with the feedback ratio, 1/N, $10logf_{PHD}$ is the increase of noise associated with the incoming phase frequency detector (PFD) frequency. According to the detail of PLL synthesizer datasheet, we could theoretically acquire phase noise of -86 dBc/Hz based on Equation 1.

## PCB CONDIDERATION

The electrical characteristics of PCB used to physically mount and connect the circuit components in a high frequency product will have a significant impact on the performance of that product. The potential magnitude of the effect of the PCB design increases with frequency as the parasitic elements tend to a similar magnitude to the typical lumped components used. As our working frequency is up to about 5 GHz, the parasitic elements which must be pay more attention is very strong, the PCB layout and trace routing must be adhered to RF circuit design disciplines.

Also PCB materials are important for the performance of RF circuit. Typical board materials are FR4, Roger. For about 5 GHz signals may be Roger preferred since it has smaller Dielectric constant, tolerance and loss tangent.

## CONCLUSION

Now schematic of board level RF front end for CBPM has been completed. PCB design and fabrication was undergoing. And dedicated CBPM signal processor, we could acquire based on the RF front end on which a digital board would be integrated, would come true. After fabrication, the RF front end equipped with the completed digital board will be test based on the SDUV facility. Good performance could be looked forward to according to all the previous consideration and simulation.

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