AN DBPM CALIBRATION METHOD IMPLEMENTED ON FPGA *

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Abstract

An calibration method on the four channels of DBPM is discussed. Using interpolation, the method is implemented on FPGA, which can handle the data on-line. The calibration algorithm is mono-channel dependent and is intended to solve the beam current dependence problem and increase resolution. Orientations of the method are presented. Basic design diagrams of the pipelined FPGA modules are listed and comparisons are made before and after the calibration.

INTRODUCTION

Due to the gain inconsistency across different channels of DBPM and the gain nonlinearity of the mono channel , problems of beam current dependence occur, which blurs beam position measurement.

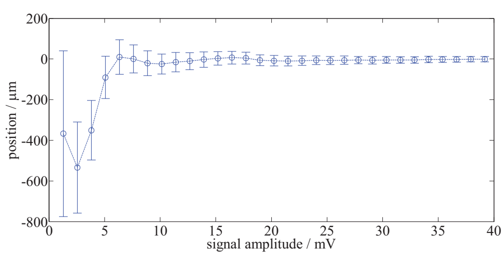

Figure 1: The beam current position dependence problem of the DBPM .

When Beam stays at the same position with increasing intensity, the same demodulated position output is expected but in practice not. The demodulated position output tend to be stable as beam current intensity increases as show in figure1. This is resulted from the fact that the channel give different gain to signal with the same frequency band but varying intensity, which we call signal channel nonlinearity and another aspect that four channels give different gain to the same signal.

The across channel inconsistency is caused by hardware inconsistency on the front end, which means that the four channel outputs differ with the same inputs, as shown in figure 2. whilst the mono channel nonlinearity refers to the fact that the gain of a channel to inputs with different intensity and deviates from a linear gain. The two aspects are shown together in figure3.

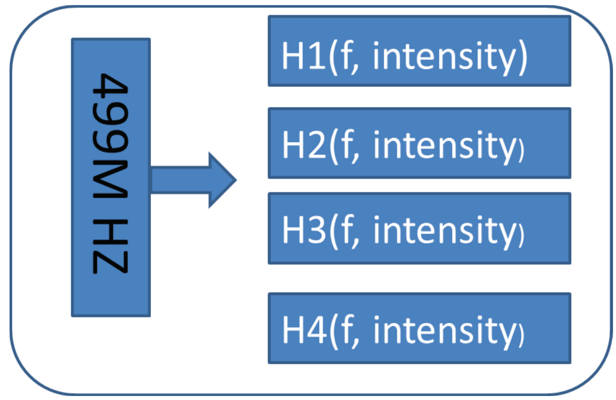

Figure 2: The four channel gain inconsistency of DBPM.

Different calibration methods have been proposed and implemented as a solution on respective instrument [2][4][5]. Libera EBPM use a Quasi-crossbar switch to randomly connect inputs to different channels thus in average remedy the inconsistency [2][3]. The SNS use the wave reflection to do calibration on the s plane analysis [5].

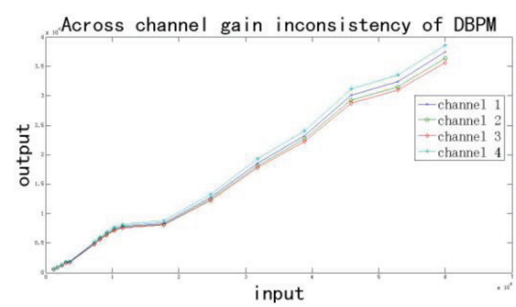

Figure 3: Across channel gain inconsistency of DBPM.

We have put forward a new approach based on DDC algorithm and attest its validity using Matlab on PC offline [4]. In this article, the calibration method using piece-wise linear interpolation is realized it on our self-developed DBPM using FPGA, thus the calibration is implemented on line directly after TBT data.

The advantage of our tactic is that it can remedy the inconsistency across different channels and the mono channel inconsistency together.

The basic idea of our method is that it try to align the four channel inconsistency to a single reference.

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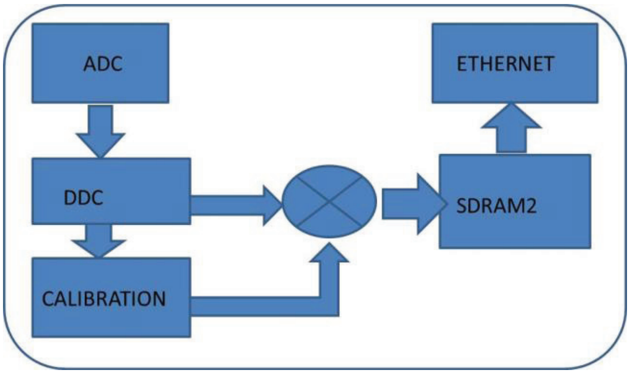

Figure 4: The calibration dataflow diagram.

OVERVIEW

The overall diagram is shown in figure 4, calibration is done to the TBT data after DDC process. A general description to our calibration strategy is as below: using standard signal source, inputs with constant frequency but varying power are fed to the four channels of the DBPM through a power splitter, response data after the processing of the 4 channels is acquired using an Ethernet interface and the energy at the critical frequency are constructed using harmonic analysis, thus a table is established that maps the processed data back to the original data. Gain experiments of the DBPM show that the nonlinearity of the gain of each channel can be well approximated by linear interpolation on small intervals. Herein, the dynamic range of the input is divided into N-1 sections, thus 5*N parameters are acquired after doing the calibration, as show in table 1.

Table 1: Calibration parameters

Input	CH1 response	CH2 response	CH3 response	CH3 response
I1	R11	R12	R13	R14
I2	R21	R22	R23	R24
……	……	……	……	……
IN	Rn1	RN2	RN3	RN4

The DDC process moves the frequency band in question down to the base band. Thus the amplitude variance reflects the energy of the critical frequency after the processing of the channel, a map back to the pre-processing state thus correct the four channel inconsistency and mono channel nonlinearity together.

$$\text{position} = \frac{\text{A - B}}{\text{A + B}} \quad (1)$$

The position calculation is carried out using formula1, while the processing gain of channel a and channel b will make the calculated position drift from the ideal one as shown in formula 2.

$$uncalibrated - position = \frac{a_G(A) - b_G(B)}{a_G(A) + b_G(B)} \quad (2)$$

The question then moves to how to use the 5*N parameters to construct the map from the TBT amplitude back to the signal source amplitude as shown in formula 3 ,where and is the map function.

$$calibrated - position = \frac{a_c[a_G(A)] - b_c[b_G(B)]}{a_c[a_G(A)] + b_c[b_G(B)]} \quad (3)$$

Here we use piecewise interpolation to thread the discrete input-response pair to approximate the amplitude response curve of DBPM in figure 3, thus giving the map function and

A general expression of interpolation is

$$I_h(x) = \sum_{j=0}^{n} f_j l_j(x) \quad (4)$$

Where (xi,fi) is the control point sampled. Lj(x) is the blending function or base function used to interpolate. When reduced to linear segmented interpolation, the blending function becomes linear, and the formula simplifies to

$$I_h(x) = \frac{xp - x}{xp - xn} f_n + \frac{x - xn}{xp - xn} f_p (xn \le x \le xp) \quad (5)$$

Figure 5 and Figure6 shows the blending function. Therefore, a core module in the FPGA would be a realization of formula 2 with inputs x, which is the uncalibrated DDC data, xn, xp, the lower and upper bound of x

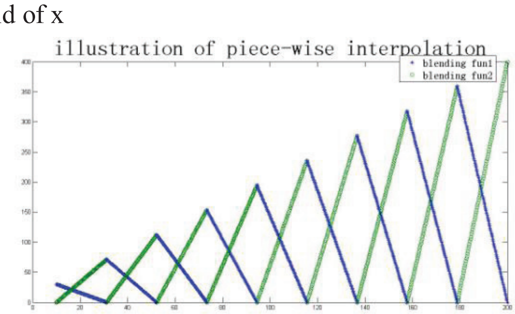

Figure 5: The global plot of blending function.

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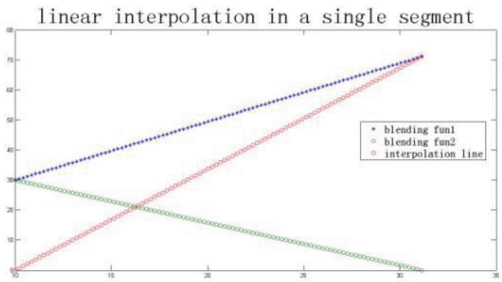

Figure 6: The local plot of blending function.

TECHNICAL DETAIL

General Layout

The algorithm is implemented on FPGA which is mounted on the digital board of the DBPM. A work flow of the calibration process looks like this:

First the data after the DDC(TBT data) are put into a segmentation module to judge which interval the current data belong to. The two ends of the TBT interval xn, xp and the corresponding signal source amplitude interval yn,yp are decided. Thus in this interval, all the parameters are determined in order to calculate the calibrated value using formula 5.

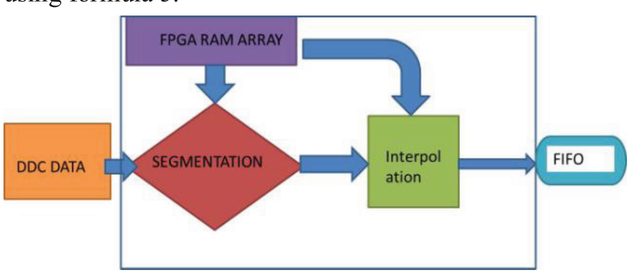

Figure 7: The working flow inside the FPGA LOGIC.

The 5*N calibration parameters in table 1 are stored on the FPGA IP CORE ram and can be dynamically altered. The whole FPGA logic is divided into several modules that are decoupled, ready for future update.

Results

Experiments are conducted which verified the feasibility of our approach. The beam current dependence problem is well suppressed as show in figure 8.

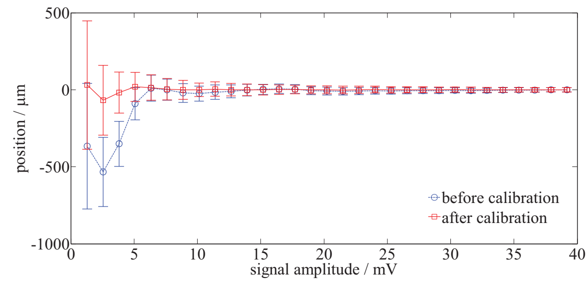

Figure 8: The beam current dependence comparison.

Disscussion

The discussed method try to align the 4 channel processing to a common reference which closely rely on the relative accuracy of the signal source. The signal source should be stable as time varies insuring an relative accurate power ratio between different input level during the calibration parameter acquire process.

Finite word length of the FPGA without floating point operation might impair the precision of the calibration but can be ameliorated by increasing the word length.

Refinements to our solution will soon be carried out. In the coming future, the whole calibration process will be controlled by the on board ARM and can be accessed remotely in an automatic way. Communication of FPGA and ARM is being brought out.

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