A GENERIC BPM ELECTRONICS PLATFORM FOR EUROPEAN XFEL, SwissFEL AND SLS

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Abstract

PSI is currently developing the 2nd generation of a generic modular electronics platform for linac and storage ring BPMs and other beam diagnostics systems. The first platform, developed in 2004 and based on a generic digital back-end with Xilinx Virtex 2Pro FPGAs, is currently used at PSI for proton accelerator BPMs, resonant stripline BPMs at the SwissFEL test injector facility, and a number of other diagnostics and detector systems. The 2nd platform will be employed e.g. for European XFEL BPMs, a new SLS BPM system, and the SwissFEL BPM system. This paper gives an overview of the architecture, features and applications of the new platform, including interfaces to control, timing and feedback systems. Differences and synergies of the different BPM and non-BPM applications will be discussed.

INTRODUCTION

As shown in Table 1, we will build an overall number of 720 BPM electronics of for different accelerators and BPM types in the next years. Moreover, we plan to use our new BPM digitizer and digital back-end electronics also for non-BPM applications.

Table 1: PSI BPM Activities and Related Accelerators

Accele-rator	***1st Beam***	***BPM Quantity***	***Status / Activity***
SLS	2000	~140(button, resonant stripline)	Digital BPM system since 2000. 2011: Start design of new BPM electronics.
SwissFEL Test Injector	2010	~25 (resonant stripline, …)	19 resonant stripline BPMs in operation. Test area for FEL cavity & button BPMs.
FLASH-II	2013	~20 (cavity)	PSI provides undulator cavity BPM electronics (E-XFEL pre-series).
E-XFEL	2014/15	~410 (button, cavity)	PSI provides electronics for ~290 button & ~120 dual-resonator cavity BPMs.
SwissFEL	2016	~150 (cavity)	Adaptation of E-XFEL cavity BPMs to lower charge & shorter bunch spacing.

European XFEL

PSI will provide the electronics for the European XFEL (E-XFEL) BPM system [1] as a Swiss in-kind contribution, with the exception of ~30 RF front-ends (RFFEs) for the re-entrant cavity BPMs in the cold E-XFEL linac that are designed by CEA/Saclay. First beam for the E-XFEL injector is scheduled for autumn 2014, beam in the main linac and undulators is expected one year later.

FLASH-II

A pre-series version of the E-XFEL undulator cavity BPM electronics will be used at FLASH-II [2], a 2nd undulator line for the VUV FEL facility FLASH to be commissioned mid 2013.

SwissFEL BPMs

SwissFEL [3] is a 0.1nm hard X-ray SASE FEL currently being developed at PSI. 1st beam in the undulators is expected mid 2016. PSI develops both the BPM electronics and the pickups for SwissFEL, based on the E-XFEL design but adapted to the lower charge (10-200pC vs. 100-1000pC) and shorter bunch spacing (28ns vs. 222ns) of SwissFEL.

SwissFEL Test Injector BPMs

In 2010, PSI commissioned the SwissFEL test injector facility (SITF), a 250MeV linac used for R&D and component development for SwissFEL. Since first prototypes of BPM electronics for E-XFEL and SwissFEL were still under development in 2010, the BPM system of SITF [4] is based on the previous generation of BPM electronics, using the same digital back-end board as the PSI proton cyclotron BPM system [5].

SLS BPM Upgrade

In 2011, PSI also started first developments for new SLS BPM electronics [6]. However, the present SLS BPM system that was commissioned 12 years ago [7] still has excellent mean time between failure (MTBF) and satisfies the present user requirements. Therefore the SLS upgrade activities have lower priority that our FEL projects where 1st beam milestones have to be met. Nevertheless, the timely development of a new SLS BPM system is motivated by long-term maintenance, growing user requirements, and the significant improvements in performance and functionality enabled by the latest analog and digital IC generations. Moreover, due to large synergies with the E-XFEL BPM systems, the development effort for the new SLS electronics is significantly reduced. As shown in Figure 1, FEL cavity and SLS button BPM electronics can use the same digital back-end mezzanine carrier FPGA board and same type of fast high-resolution (16-bit) ADC mezzanine. The main structural difference of the RFFEs is the lack of a mixer and local oscillator (LO) for the SLS, where the lower BPM pickup signal frequency of 500MHz allows direct undersampling.

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Table 2: PSI BPM Electronics Generations (generation 2.1 under development, also to be used for E-XFEL when ready)

Gene-ration	Final Application	Year	RFFE In/Out Frequency [GHz]	ADC Boards	Digital Back-End	ADC Data Deci-mation / Filter	Xilinx FPGA Type	# ADC Channels (per Digital Back-End) x max. Sample Rate [Samples/s]	ADC Interface Speed of Digital Back-End (max., per pin)
0	SLS	2000	0.5/0.036	BPM Specific	BPM Specific	ASIC	-	4x40M (12-bit)	<100Mbps (Single Ended)
1.0	Cyclotron	2005	0.1		Generic		Virtex-2 Pro	4x40M (14-bit)	<100Mbps (Single Ended)
1.1	SwissFEL TI	2010	0.5			FPGA		4x5G (S&H) / 33M (14-Bit)	
2.0	FLASH-II	2013	3.3/0	Generic			Virtex-5 FXT	12x160M (16-bit)	<1.25Gbps (LVDS)
	E-XFEL	2015	various					16x500M/12x160M (12/16-bit)	
2.1	SwissFEL	2016	3.3-4.8/0				Artix-7 / Kintex-7	12x160M (16-bit) or more	
	SLS New	2016+	0.5					8x160M (16-bit) or more	

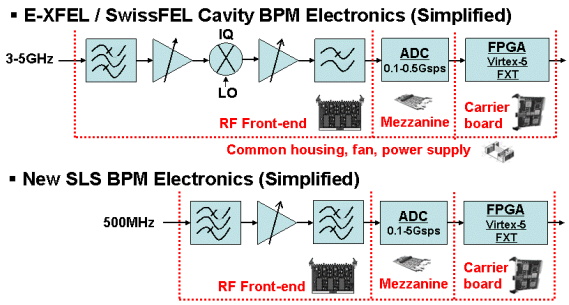

Figure 1: Modules of FEL and SLS BPM electronics prototypes (final version: Newer FPGA type).

EVOLUTION OF PSI BPM SYSTEM DESIGN

Modularity and Re-Usability

In order to minimize the development and maintenance effort for our different BPM projects, we are following a modular design approach, with the goal to maximize the number of re-usable ("generic") hardware, firmware and software components. Table 2 shows the different BPM electronics generations developed by PSI since 2000. Generation 0, the SLS DBPM1 system [7], already has a modular design with separate printed circuit boards (PCBs) for RFFE, ADC mezzanines, and ASIC-based digital back-end. However, all boards are BPM-specific and not suitable for general-purpose use.

The next generation already has a generic digital back-end with two Xilinx Virtex-2 Pro FPGAs and is used for a larger number of BPM and non-BPM applications, including PSI proton cyclotron and SITF BPMs. However, the digitizer boards for these generations, realized as VME rear transition board (proton BPMs) or PMC mezzanine (SITF), are BPM-specific, using e.g. analog filters or digital downconverters (DDCs) that make them unsuitable as general-purpose digitizers.

In contrast, for our present generation 2 FEL BPM prototypes both the digital back-end FPGA board and ADC mezzanine are generic, where all digital filters and signal processing are implemented in FPGAs on the digital back-end, while all BPM-specific analog circuitry is located on the BPM-specific RFFE.

In general, having RFFE, ADCs and digital back-end on separate board allows to develop and test them independently, thus aiding an efficient parallel design process. In addition to the possibility to use different combinations of back-end, ADC and RFFE for different applications, the modular design approach also allows to upgrade e.g. ADC boards independently, or to develop new versions for different requirements, which minimizes version diversity and long-term maintenance effort.

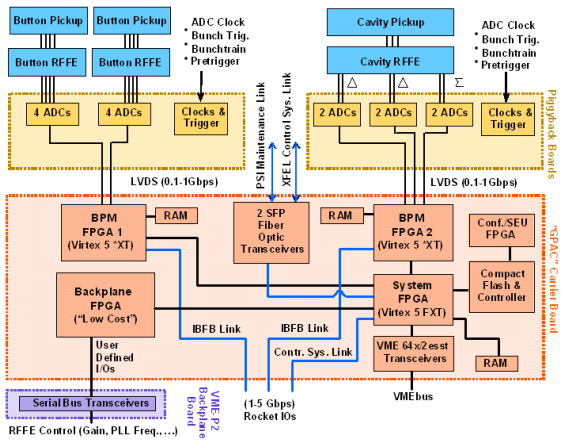

Figure 2: E-XFEL BPM electronics generation 2.0 block diagram (simplified). Blue: Pickup/RFFE. Yellow: ADC mezzanine. Red: Digital back-end carrier board.

ADC Interface Speed

For the signal transmission from RFFE to ADCs, electronics generation 2 uses compact differential coaxial connectors, thus avoiding a degradation of signal quality and resolution due to ground loops etc.

As shown in Table 2, one major difference of electronics generation 2 to previous ones is the use of terminated LVDS lines instead of unterminated single-ended lines for the interface between ADC mezzanine and FPGAs on the carrier board. This not only allows an increase of the supported maximum sampling rate of ADCs with non-DDR (dual data rate) parallel interfaces from 100MSamples/s to >1GSamples/s, but also minimizes noise, since the LVDS lines avoid ground bounce and interference noise of nearby circuits.

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For the SITF BPMs that have 500MHz resonant stripline pickups, we used digital back-end generation 1 with its low (<100Msps) speed interface. Therefore we employed an analog multi-channel waveform sampler chip developed at PSI, where the 500MHz signal of the resonant stripline BPM RFFE is sampled with 5GSamples/s in 1024 analog sample/hold (S&H) capacitors in the chip. Its internal multiplexer allows the comparatively slow readout of the S&H cells for all channels by a single 33MSample/s 14-bit ADC that could easily be interfaced to the generation 1 carrier board.

Mezzanine Form Factor & Connector Standard

Each of the two mezzanine connectors of our generation 2 digital back-ends provides 96 differential signal pairs for ADC data, supporting mezzanines with up to six 16-bit ADCs (for one E-XFEL cavity BPM) or eight 12-bit ADCs (for two E-XFEL button BPMs) with parallel differential outputs. In addition, the pinout we chose for the mezzanine connector has a number of other signals like ADC clocks and strobes, 8 optional multi-gigabit links (e.g. for multi-SFP mezzanines), JTAG, I2C for board management, 3.3V and 5V supply voltage with current and voltage monitoring on the mainboard, etc.

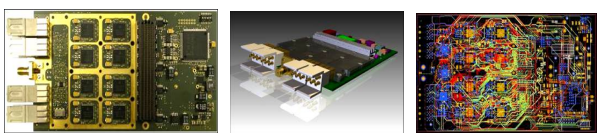

Figure 3: E-XFEL button BPM ADC mezzanine (8-channel 12-bit 500MSamples/s).

Our PSI-specific mezzanine standard is similar to the VITA 57 FMC (FPGA Mezzanine Card) standard, but has ~50% more user IO pins and a more than 2x larger PCB area that we both need for our applications. Therefore we kept our standard (developed in 2006/2007) and did not migrate to FMC (that uses the same connector version, but with 100 pins less, and different pinout) when it was introduced in 2008.

Digital Back-End and RFFE Form Factor

Digital back-end and RFFEs of all our BPM generations use the VME or VME64x standard, with the exception of the proton BPM RFFE that is a standalone box close to the beam.

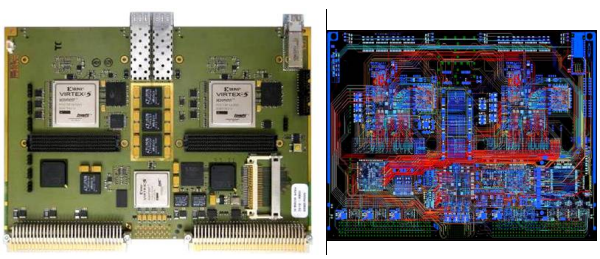

Figure 4: Digital back-end generation 2.0 prototype (GPAC = Generic PSI ADC Carrier). Left: Photo (old version with unmounted VXS connector & front-panel, mezzanines also not mounted). Right: PCB Layout.

Generation 0 required the VMEbus to operate the digital back-end. In contrast, generations 1 and 2 also work standalone, using multi-gigabit links for control, timing and feedback interfaces, where the VME P1 and P2 backplane connectors mainly provide power and some user-defined low-speed (<100Mbps) control/status signal connections between back-end and RFFE, e.g. for programming/readout of RFFE attenuators, PLL phases and frequencies, temperature sensors, bias voltages etc.

While first generation 2 prototypes used a VXS backplane connector that allowed multi-gigabit links in special VXS crates (when mounted), our present version has a new P0 connector that supports high speed (6.5Gbps/pin) data transfer in normal VME64x crates. Our present generation 2 board version provides eight full-duplex multi-gigabit links between FPGAs and P0 connector, thus supporting multi-gigabit links between different boards via suitable rear transition modules e.g. with SFP(+) or PCIe connectors, both in standard VME64x crates or in the customized “MBU” (Modular BPM Unit) crate of the E-XFEL BPMs.

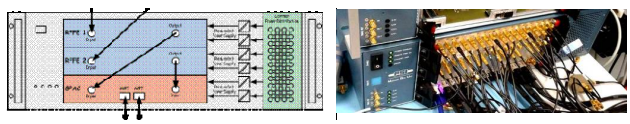

Figure 5: Modular BPM Unit (MBU), with digital back-end (bottom) and two cavity BPM RFFEs (top).

PCB Space, Crate Volume and Hardware Test Considerations

The most important performance figures of a BPM system are determined mainly by the RF front-end and ADCs: Resolution, drift, bunch charge and filling pattern dependence, etc. Initial estimations showed that the desired functionality of RFFEs and digital back-end both fit (just) onto a VME64x size board, but would not fit on form factors with smaller PCB sizes without sacrificing performance and functionality, which was confirmed by our present prototypes. This was one motivation to use the VME64x standard also for our latest electronics generation. RFFEs and digital back-end are plugged onto a back plane via slots at the front side of the crate. The relevance of the different modules for the overall system performance and functionality is reflected by the fact that about 2/3 of the respective front area crate volume are available for the RFFEs.

An added benefit of our RFFE form factor and interface concept is that an RFFE can be tested outside of a crate, since one only has to connect power and some relatively slow digital control IOs to the backplane connector to operate it. During RFFE test and development, the board is thus fully accessible from both sides for measurements with probes etc.

Cooling and Active Temperature Stabilization

Our present crate and form factor concept results in a mainly homogeneous distribution of the generated power over the crate volume. The spatial separation of RFFE

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and digital back-end minimizes both interference noise and drift caused by variations of the power dissipation of digital back-end components (FPGAs, processors) during operation. Our latest FEL RFFE versions also minimize drift via active temperature stabilization, using several on-board heaters and temperature sensors on the RFFE PCB.

MTBF and System Management

Our latest FEL BPM electronics generation and its MBU have a redundant crate power supply, redundant fans, voltage and current monitoring as well as overcurrent protection individually for each board and each ADC mezzanine. Live extraction and insertion of the boards is also possible. Remote identification and configuration are supported by I2C EEPROMs with a unique serial number and configuration information on each PCB.

Control System Interface

The present interface concept allows to use our BPM electronics both at the VME64x dominated PSI accelerators as well as in non-VME environments, where our latest electronics generation 2.x can also be interfaced to non-VME systems based e.g. on the xTCA standard, via a variety of supported interfaces and protocols like PCI Express (PCIe), Ethernet, SerialRapidIO, etc.

Table 3: BPM Electronics Serial Interfaces and On-Board Processors

Gene-ration	Final Appli-cation	Ether-net / PCI Express Speed [Gbps]	Multi-Gigabit Serial Links to External Connectors & SFP(+)	PSI Timing Interface / Any Baud Rate Supported	On Board Pro-cessor / Linux
0	SLS	-	-	-	-
1	Cyclotron SwissFEL TI	- -	2x2.1Gbps	Y / -	Y / -
2.0	FLASH-II E-XFEL	1/2.5	26x6.5Gbps	Y / Y	Y / Y
2.1	SwissFEL SLS New	1-10/5	22x6.6Gbps+ 4x12.5Gbps		

As shown in Table 3, our present carrier board version 2.0 supports 1G Ethernet and PCIe Gen1 (2.5Gbps, end point), while generation 2.1 that is currently being developed will also support 10G Ethernet and PCIe Gen2 (5Gbps, root complex or end point).

Processors and Position Computation

BPM electronic generation 0 of the present SLS BPM system needed an external DSP board for tasks like position calculation, RFFE gain control, triggered data recording in waveforms etc, while generation 1 performs such tasks autonomously via PowerPC405 processors in its Virtex-2 Pro FPGAs.

Electronics generation 2.0 still has PowerPC440 processors in Virtex-5 FXT FPGAs, while the Artix-7 and Kintex-7 FPGAs on the latest generation 2.1 that we are currently designing have no on-chip PowerPCs any more.

For FEL and new SLS BPMs, the beam position is directly calculated in the FPGA in firmware (VHDL). The resulting ultra-low latency of some 100ns for the FEL BPMs allows to use them the for the E-XFEL transverse intra-bunch train feedback (IBFB) [8], where we aim for a feedback loop latency <1.5µs.

For our latest digital back-end generation prototype, we have currently foreseen an additional on-board DSP (digital signal processor), in order to be able to use the board also as orbit feedback computation engine and for measurement data analysis tasks. Both our present (2.0) and new (2.1) back-end support on-board Linux.

Timing System Interface

The generation 2.x digital back-end can also be directly interfaced to the timing systems of E-XFEL, SwissFEL and SLS. These timing systems are based on multi-gigabit links where the digital back-end FPGAs can decode the protocol and provide triggers and synchronous clocks.

ADC Clock Generation

For the E-XFEL button BPMs, the fiber optic timing interface of our electronics also generates the bunch-synchronous ADC clock, by recovering the baud rate clock of the multi-gigabit bitstream in an FPGA on the digital back-end, plus a PLL for jitter reduction. For the E-XFEL and SwissFEL cavity BPMs where higher performance is needed, the ADC clock is generated by the RFFE that derives both ADC clock and LO frequency from an external SMA input fed by the ultra-low jitter reference RF clock distribution system of the accelerator. For SLS, the ADC clock will be generated by the RFFE that is connected to the 500MHz SLS reference RF clock distribution. Both for SLS and FELs, ADC clock and RFFE LO frequency and phase are programmable and can be changed in real-time by the digital back-end.

Feedback Interfaces and Memory

As shown in Table 3, interfaces to fast beam-based feedback networks for E-XFEL, SwissFEL and new SLS BPMs are provided by several optional multi-gigabit links, employing fiber optic SFP(+) transceivers with multi- or single-mode fibers (depending on cable length).

Table 4: BPM Electronics Memory

Back-End Gene-ration	Final Appli-cation	External FPGA RAM		Non-Volatile Memory (Configuration, Hard-Disk, …)
		Σ Size [Byte] Type)	Σ Band-width [Byte/s]	
0	SLS	<100k (FIFO)	...	EEPROM
1	Cyclotron SwissFEL TI	4M (ZBT)	1G	Compact FLASH
2	FLASH-II E-XFEL	16M & 256M (QDR2 & DDR2)	4+4G (R+W) & 4G	Compact FLASH
2.1	SwissFEL SLS New	5G (DDR3)	20G	µSD Card

Table 4 shows the on-board memory for the different BPM electronics digital back-end generations. For our

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next generation 2.1, we intend to use DDR3 SDRAM for all purposes, with max. 20GByte/s integral overall bandwidth, 5GByte overall size, and a µSD card for non-volatile data storage (e.g. FPGA configuration).

BPM SYSTEM STATUS

SwissFEL Test Injector BPMs

The SITF resonant stripline BPM system is operational since autumn 2010, achieving 7µm RMS resolution and typ. <0.2% charge resolution from 5-500pC [4].

FLASH-II and E-XFEL BPMs

Digital back-end, ADC mezzanine and RFFE for the E-XFEL and FLASH-II undulator cavity BPMs are presently in a pre-series stage. Recent noise correlation tests [9] with three E-XFEL undulator cavity BPMs, installed in a test area in the SITF linac at PSI, showed that the present electronics prototype already fulfils the E-XFEL resolution requirements, i.e. <1µm RMS from 0.1-1nC at ±0.5mm range.

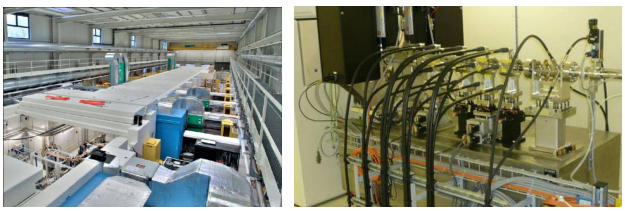

Figure 6: Left: SwissFEL Injector Test Facility (SITF). Right: Cavity BPM test area at SITF.

At Q=180pC, we obtained e.g. 180nm RMS resolution (±0.5mm range) that scales ~1/Q for lower charges. The IQ imbalance correction necessary to obtain this resolution was performed offline, but is currently being implemented in the FPGA on the digital back-end. Long-term drift measurements still need to be performed.

The E-XFEL button BPM electronics is currently being tested in the lab, with beam tests planned until end 2012.

SwissFEL BPMs

The above mentioned E-XFEL undulator cavity BPM beam tests at SITF showed a resolution of 11µm RMS at 2pC and ~2.5µm RMS at 10pC. In order to reach the desired resolution of < 1µm RMS at 10pC for SwissFEL, we are currently developing a cavity pickup that provides higher signal at lower charge [10]. A first prototype that should provide ~3x better resolution at low charge has already been fabricated, and will be tested with beam in the near future.

SLS BPM Upgrade

Our modular electronics concept allowed us to assemble a first SLS BPM prototype just by recombining modules of our FEL BPM hardware: We connected the SITF 500MHz resonant stripline RFFE to the ADCs and digital back-ends of the E-XFEL BPMs, using a 500MHz signal generator and 4x splitter to simulate a centered SLS beam. Combined with our newly developed VHDL-based digital downconverter and position calculation FPGA firmware [6], we obtained a position resolution of ~80nm RMS for a 10mm geometry factor, which is already ~10x better than our present BPM system. We are currently developing a dedicated new SLS BPM RFFE, aiming not only at <100nm RMS resolution, but also comparable long-term stability/drift.

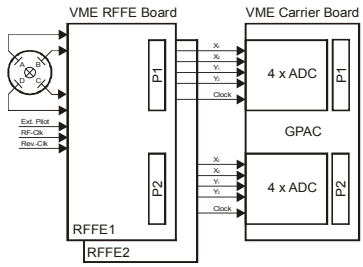

Figure 7: Topology of the new SLS BPM electronics.

SUMMARY AND OUTLOOK

The development effort for our different BPM electronics projects is significantly reduced by a generic modular design approach. While the present FEL BPM electronics prototypes are already close to the final versions, with sub-micron resolution for cavity BPMs, the development for the SLS BPM upgrade has just recently started, but will benefit from strong synergies with FEL systems, sharing the same digital back-end and similar ADCs. In addition to BPMs, our present electronics platform will also be used for non-BPM systems. Examples are e.g. longitudinal diagnostics systems for SwissFEL, where e.g. prototypes of a bunching monitor and beam arrival time monitor, based on our present generation 2 BPM back-end and ADCs, are presently being commissioned at the SwissFEL injector test facility.

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