CAMERALINK HIGH-SPEED CAMERA FOR BUNCH PROFILING

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Abstract

In the context of upcoming SwissFEL linear accelerator, we are working on a high-speed high-resolution instrument capable of delivering good sensitivity even in dark conditions. The camera selected is a PCO.Edge with SCMOS technology and an ultra-low noise sensor with 2560x2160 pixel resolution working at 100Hz. This allows for single bunch monitoring in SwissFEL, allowing eventually for on-the-fly inter-bunch image processing.

The communication between the PCO.Edge camera and a last-generation Kintex7 FPGA has been demonstrated using a prototyping evaluation board and an 850-nm optical link connected to a 10Gbit SFP+ transceiver. Rudimentary packet processing has been implemented to confirm the satisfactory operation of the new link-layer protocol X-CameraLinkHS, specifically development for high-speed image transmission. We aim for online image processing and investigating the feasibility of achieving inter-bunch feedback (< 10 ms).

SYSTEM DESIGN FOR PROCESSING IMAGE AT ON-THE-FLY

The system is designed to monitor bunches of electrons with a high-resolution high-speed camera, capturing frames at 100Hz, the working frequency of the SwissFEL laser gun [1]. A last-generation FPGA will process such frames at a high speed, extracting the relevant parameters, comparing these values to programmable thresholds and eventually allowing for fast feedback to the machine without the intervention of the operator (see Fig. 1).

Frames need to be transmitted from the camera to the processing system over a distance of up to 1km, using for this purpose an 860-nm multimode optic fibber, which comfortably allows for the 10Gbps data rate of the camera. The preference of optic fibber over cooper cabling is advised due to the long distances and noisy environment in which the system will be deployed.

Data is formatted in the camera according to the Camera-Link High Speed (CLHS) Protocol [2], which has been designed to provide low latency and low jitter in real-time signals for high-bandwidth image transmission. This is a proprietary link-layer protocol which can be implemented over commodity Ethernet connectors, thus benefiting in terms of price and availability of hardware. Particularly in our design, we use two Small form-factor pluggable transceivers (SFP+), a widely-spread standard in the communication industry for optic fibbers.

The frame grabber has been implemented on a KC705 Prototyping Platform from Xilinx. This board includes a last-generation Kintex7 FPGA, which is the targeted device for the final design implementation. On this board, DDR3 memory and one PCI connector are available, which are a powerful asset for further expanding the system capabilities. For deploying the instrument in the accelerator tunnel, we will transfer the firmware to a General Purpose Carrier Board v.3.0 (GPAC), which is expected to be the workhorse electronic board for future SwissFEL instruments.

The embedded system includes the Frame Grabber (an Intellectual Property (IP) Core) running along many other modules. For instances, the 10GBASE-KR core from Xilinx conveys the physical signals into CLHS packets (it is actually our PHY layer). The CLHS packets are decoded and transformed into frames by the X-Protocol decoder, provided by PCO, the camera manufacturer [3]. From this point on, the data format is presented as rows and columns of pixels. Together with the corresponding context data, the frame can be rebuilt.

At this point, we have two options. Data can be either processed at wire-speed on the FPGA in order to extract the relevant parameters or it can be alternatively stored on a temporary local buffer, waiting for retrieving from the control system an eventually processed offline. Both options present its advantages and drawbacks. Buffering large amounts of information require of fast big buffers, which can only be implemented with a reasonable cost on DDR memories. Even in this case, only some ms of video streaming can be stored.

A second option consists in processing the frames on-the-fly using a set of Hardware Accelerators specifically designed for this purpose (*Schwerpunkt* Extractor, Gradient Machine…). If fast enough, this early extraction of information from the frames may allow for inter-bunch feedback to the actuators, greatly speeding up the precise calibration of the machine. In this last case, the need for a large buffer would be overcome, though at the price of increasing design effort while flexibility for later modifications becomes more difficult.

SCMOS SENSORS

Many scientific imaging applications demand multi-megapixel focal plane sensors that can operate with very high sensitivity and wide dynamic range. Scientific CMOS technology delivers a very large high field, together with a low noise figure, that can be up to one degree of magnitude smaller [4]. This is especially the case when the number of photons is very low, as it is in our case, when only a handful of photons (~200) excite the sensor.

This high performance is obtained without reducing the fps rate, so the sensor is capable of capturing frames at 100 Hz without the traditional trade-off in CCD cameras that requires reducing resolution to increase frames per

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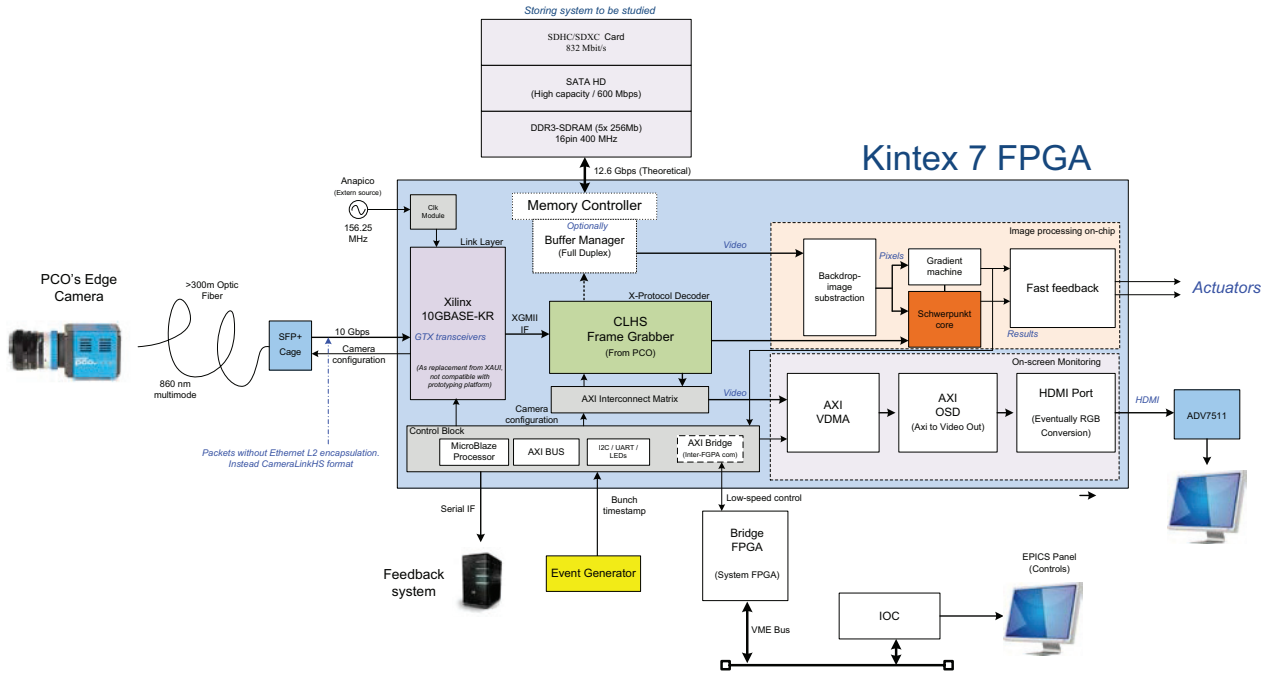

Figure 1: Prototype being implemented on a Xilinx's Kintex7 Prototyping Platform (KC705) with a K7 FPGA (xc7k325-2).

second or alternatively increasing fps but reducing the noise-to-signal figure.

In our case, one particularly interesting option is dynamically selecting a region of interest (ROI) and so capturing only a small portion of the image. The bunch usually excites less than 10% of the sensor, being its position variable before setup but quite stable during machine normal operation. This provides us with higher resolution and reduces the amount of data to be transmitted/processed to/in the FPGA.

STATUS AND NEXT STEPS

At the moment, the Frame Grabber is up and running on our test environment, being able to communicate with a camera prototype (the final camera is not yet available). Frames are received over optic fibber, and the PHY and Link Layer cores are up and working. The CLHS frames have been observed using a logic analyser. Together with this, a Test *Schwerpunkt* Extractor has been implemented to begin experimenting with data manipulation and control of the video streaming. This part of the system (which we could describe as data plane) is configured and monitoring by the control plane. For this purpose, a full-fledged on-chip Microblaze processor system together with its AXI communication matrix has been implemented to support the data plane.

In the coming months, we aim at extending the set of hardware accelerators. Priority has been given to communicating via PCI-Express with a fast PC to monitor the video stream on-the-fly on a screen, hence validating the correct setting of the camera. Alternatively, we study the option of using the VDMA cores included in the Xilinx Vivado programing suite, directly driving a HDMI Port from the FPGA without the need of a supporting PC.

Eventually, the system will be transferred from the current prototyping platform to a General Purpose Analog Carrier board (GPAC v3.0). This PSI board will include different last generation FPGAs, including several seven series. Taking advantage of existing Firmware, the system will connect to a control board over a VME bus and from there to the SwissFEL network. Monitoring and control will be done over EPICS panels in the same way as the rest of the instrumentation on the accelerator.

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