PAL-XFEL MAGNET POWER SUPPLY SYSTEM

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Abstract

This paper presents an overview of the magnet power supply (MPS) for the PAL-XFEL. The number of total MPS is up to 624 and they will be installed along the accelerator and the undulator sections. The power capacity of the MPS was ranging from about 1 A to 300 A. These MPSs were required to meet the high stability that was subjected from the beam dynamics specifications. This paper described the overall MPS requirements, MPS assembling, test process, control scheme, installation plan and so on.

INTRODUCTION

The PAL-XFEL is the 4th-generation light source, base on a single pass FEL, under constructing at Pohang Accelerator Laboratory in Korea. This project aims at the generation of X-ray FEL radiation in the range of 0.1 to 10 nm for users. The machine consists of 10 GeV linear accelerator and hard and soft X-ray undulator beamlines. The accelerator will operate at a 60 Hz and will be extended to 120 Hz [1]. Total 624 set of MPS are used for beam orbit correction and maintained for the beam trajectory. To reach the best performances expected from a 4th-generation source, very demanding specifications have been targeted notably on magnetic field stability and reproducibility of the various magnets, hence on the currents delivered by the power supplies. The power supplies have ratings which range from about 1 A to 300 A. The topologies of the MPSs are buck and H-bridge chopper type. This paper describes the MPS developing status and installing plan and so on.

MAGNET POWER SUPPLY SPECIFICATIONS

Table 1 describes the specifications of the three kinds - quadrupole, dipole and corrector - magnet power supplies for the PAL-XFEL.

Table 1: Total MPSs Number for PAL-XFEL

Magnet	MPS type	Qty	Stability(ppm)
Corrector	Digital	283	10 & 50
	Analog	108	50
Quadrupole	Unipolar	122	100
	Bipolar	86	
Dipole	Unipolar	20	20
	Bipolar	2	
Solenoid	Bipolar	3	20

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Based on the maximum operating current and voltage, 213 quadrupole magnets are divided into 11 families, 48 dipole magnets are 7 families. The 391 corrector magnets are grouped 3 families base on the current rating and stability. The power supplies can be categorized as unipolar and bipolar power supplies.

HARDWARE STRUCTURE AND CONTROL SCHEME

The basic structure of a power supply with controller, ADC and interface to the control system is shown in figure 1. The topologies of the converters are either buck or H-bridge. It is based for the unipolar of dipole and quadrupole MPS on the following chain of elements: 12-phase transformer, rectifier, input filter, energy storage, switching device and output filter.

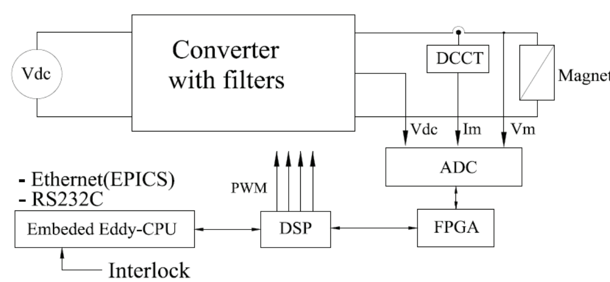

Figure 1: PS control structure overview.

The transformers adapted to the higher power capacity have two secondary windings, one delta-connected and the other wye-connected to configure the 12 phase rectifier in order to reduce the AC ripple on the DC link of the power supply. The bandwidth of the input filter should be less than 30 Hz to have a good output performance. A freewheeling diode and an L-C filter are put across the output stage. The cut-off frequency of output L-C filter is about 5 kHz. It gives a good dynamic control performance. A soft charge circuit on the rectifier limits the inrush current during power on.

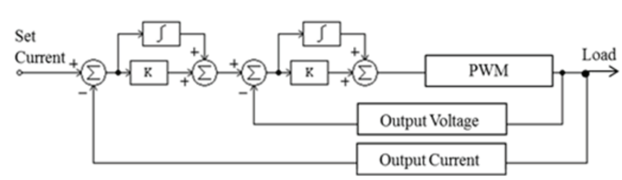

Figure 2: Control loop structure.

Figure 2 shows the control loop structure of MPS. The control loops for the switching mode power supply are consisted of a cascaded current and voltage feedbacks, the inner loop controls the output voltage, and outer loop

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controls the output current [2]. The control loops are executed at every PWM switching frequency.

Since the introduction of digital signal processor, a fully digital-controlled MPS has many advantages over the analog one. Its output characteristics are less sensitive to noise and less susceptible to parameter variations from thermal and aging effects. Also, it has flexibility in control system [3]. Digital control processing for MPS will be built on the DSP TMS320F28335 from TI Co. It has 6 enhanced PWM modules with 150 ps micro edge positioning [4]. The uC5282 embedded microprocessor module from Arcturus Co. was assembled into the DSP board to support Ethernet.

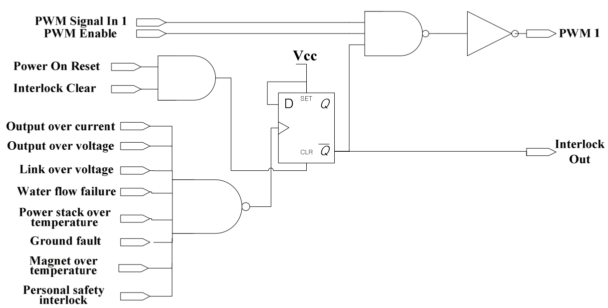

Figure 3: Logic diagram of Interlock signal process.

Interlock signal process is shown in figure 3. All MPS are equipped with latched interlocks to detect abnormal MPS and magnet conditions such as shown in figure 3. When interlock is occurred, MPS output is blocked by hardware logic and it transfer the state to control room. In this time, interlock state is latched and it was returned to normal state by reset switch or consol command.

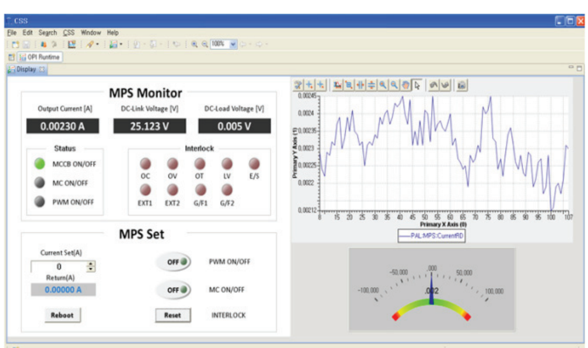

Figure 4: MMI display at computer.

Figure 4 shows the MMI (Man Machine Interface) example of MPS. This panel is made by CSS tools [5]. The EPICS IOC was embedded in the uC5282 board of the MPS controller. The MPS also included the RS232C port to interface in the front of the MPS site. These MPSs included the small web server to make easy maintenance.

MAGNET POWER SUPPLY ASSEMBLING

There is a lot of numbers MPS assembling. Whole power supply should be modularized to install in 19' rack size. Figure 5 shows an example of the corrector MPS installation diagram.

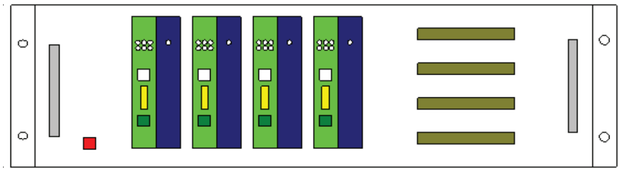

Figure 5: Corrector MPS mounting diagram.

We plan the 4 - corrector MPSs (below 400W) is installed in 3U unit of standard 19' rack. These corrector MPS has independent controller, but communication module is shared by 2 MPS. The switching frequency of these 4 corrector MPS should be design to synchronize. The size of quadrupole MPS for less than 400W is 1/2 of 4U unit. All MPS cabinets have safety ground which was connected to the distribution board.

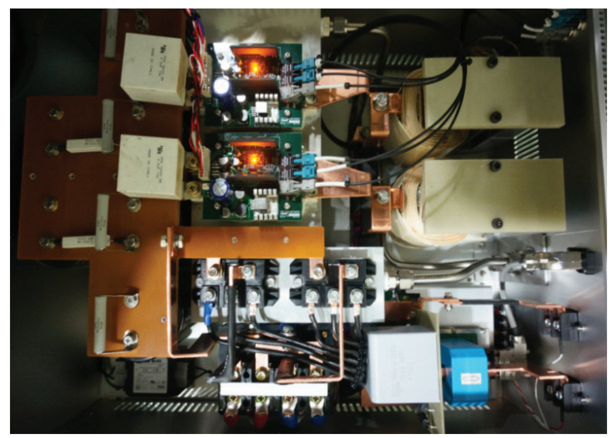

Figure 6: Power stack of 90A Bipolar MPS.

Figure 6 shows the power stack of 90A bipolar MPS. The left side is source input and right side is output. It shows the IGBT modules and input, output filters.

TEST PROCESS

In factory stage, the acceptance test will focused on the power circuit. During the 8 hour's operation at 100% normal current, DC link capacitor bank and IGBT module temperatures will be checked.

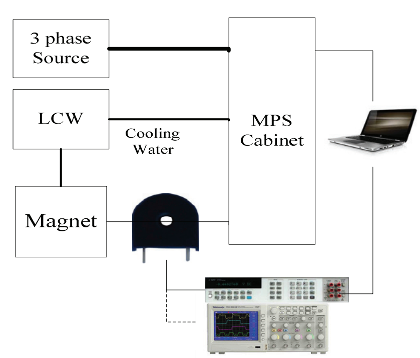

Figure 7: MPS performance test scheme.

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Figure 7 shows the MPS performance test scheme. For the measurement of DC output current, digital volt meter (DVM), HP3458A, and external high precision DCCT MACC150 from HITEC are used and output ripple voltage is measured by oscilloscope [6]. The DVM has an 8 1/2 digit resolution, and 0.6 ppm accuracy [7]. To measure the insulation resistance, mega ohm tester is used. All data is acquired by computer to verify the MPS performance.

Figure 8 shows the performance test result of prototype power supply and magnet for PAL-XFEL. The short term stability of the MPS is below 5 ppm for 30 minute at full output power.

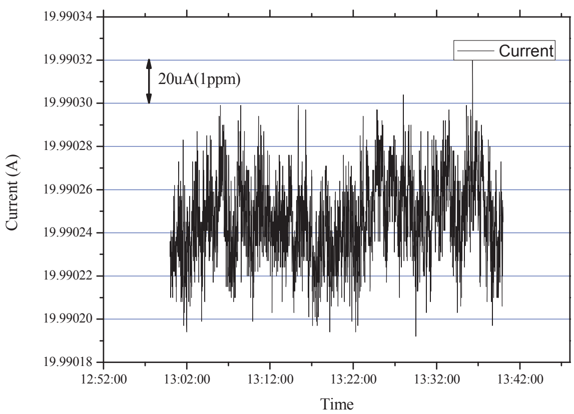

Figure 8: Current stability for 30 minute at 20A and 5V output.

Figure 9 shows the reproducibility test results. The current was set to 10 A and 8A repeatedly by 5 times. It shows the difference of output is less than 2.5 ppm.

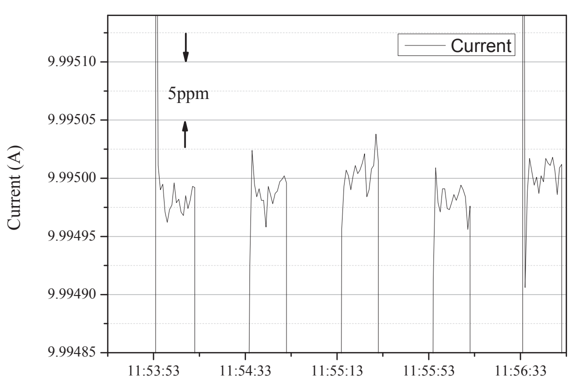

Figure 9: Reproducibility test result.

INSTALLATION PLAN

We will prepare the installation plan and verify the schedule and procedure. All assembled MPSs are evaluated the performance at before installation. To remove the interference between the accelerator devices and MPSs, 3D model drawing of magnet and MPS rack will be draw. The output cables of MPS are non-radioactive and current capacity is 1.5 A/mm^2 for above 100A and 2 A/mm^2 for below 100A. When the devices are installed in site, field tests are done for verifying the performance. The MPS will be begin to install in March and ended in June 2015. The whole MPS site tests will be carried out for 3 months from July 2015. We hope all errors are cleared out and keep for normal status for the best beam commissioning.

CONCLUSION

This paper described the overall MPS requirements, control scheme, MPS assembling, test process, installation plan for PAL-XFEL. In factory stage, the acceptance test will focused on the power circuit. After the 8 hour's operation at 100% normal current, DC link capacitor bank and power stack temperature will be checked. These MPS included the small web server to make easy maintenance. The MPS will be installed from March 2015 and operation tests will begin July 2015.

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