NSLS-II RF BEAM POSITION MONITOR UPDATE*

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Abstract

The NSLS-II RF BPM development was undertaken to create a state-of-the-art BPM with the goal of exceeding capabilities and performance that has been demonstrated to date. The architecture of the RF BPM has been carefully conceived to provide a robust design with substantial flexibility to serve as a platform for other systems, one of which is the Cell Controller, which is used to process BPM data for fast orbit feedback.

INTRODUCTION

The NSLS-II RF BPM program began in August of 2009. Successful beam tests were conducted at the LBNL Advanced Light Source (ALS) 15 months into the program. Now 2.5 years into the program all operational features have been implemented and verified on user beam at ALS. All 60 Injection system BPMs have been built and tested with an additional 15 production units in circulation for test and development.

In this paper we will report on the final BPM architecture, performance and production tests.

BPM ARCHITECTURE

The NSLS-II RF BPM consists of an AFE and DFE board housed inside a 1U 19" chassis. Power is supplied to each board through independent switching power supplies. The Analog Front End (AFE) uses on-board low dropout linear regulators to filter the 6V switching power supply. The Digital Front End (DFE) includes on-board switching regulators to convert the 5V supply to required voltages for FPGA and associated components. A picture of a production RF BPM is shown below in Figure 1.

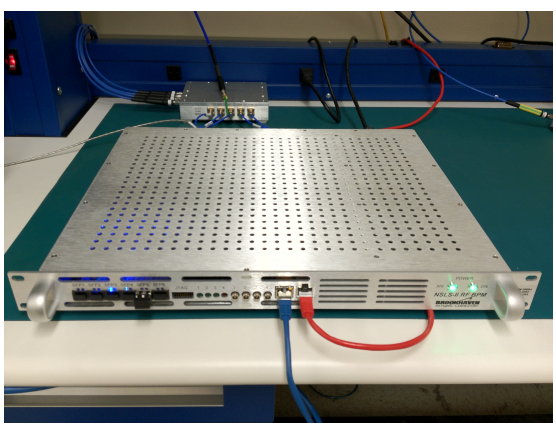

Figure 1: NSLS-II RF BPM (Production Unit).

The RF BPM has adapted a generic architecture such that the RF BPM is parametrically configured for Single-Pass, Booster, and Storage Ring. Each RF BPM is assigned a unique IP address, which is stored in FLASH memory and is mapped to a geographical location in the NSLS-II.

When the RF BPM is turned on the IP address is examined to determine proper configuration mode. The RF BPM then automatically configures itself in one of the three possible operational modes.

The Digital Signal Processing (DSP) architecture is also generic; all three operational modes are derived from storage ring revolution frequency.

Table 1: RF BPM Data Transfer Capabilities

Data Type	Mode	Max Length
ADC Data	On-demand	256Mbytes or 32M samples per channel simultaneously
Single-Pass	Streaming	800hr circular buffer (1Hz Injection)
TBT	On-demand	256Mbytes or 5.3M samples Va,Vb,Vc,Vd, X,Y,SUM, Q, pt_va,pt_vb,pt_vc,pt_vd
FOFB 10KHz	Streaming via SDI Link and On-demand	Streaming - X,Y,SUM For On-Demand: 256Mbytes or 5.3M samples Va,Vb,Vc,Vd, X,Y,SUM, Q, pt_va,pt_vb,pt_vc,pt_vd
Slow Acquisition 10Hz	Streaming and On-demand	80hr circular buffer Va,Vb,Vc,Vd, X,Y,SUM, Q, pt_va,pt_vb,pt_vc,pt_vd
System Health	On-demand	80hr circular buffer AFE temp, DFE temp, FPGA Die temp, PLL lock status, SDI Link status
FFT Coefficients	On-Demand	TBD

Analog Front End (AFE)

The AFE topology is based on bandpass sampling architecture which subsamples the 500MHz impulse response of the SAW bandpass filter at ~117MHz.

The response of the filter produced for a single bunch results in an impulse of approximately 30 samples or ~300ns in length. Coherent timing is derived from an external 378Khz revolution clock supplied via differential CML. An analog phase-locked loop is used to synchronize ADC VCXO based clock synthesizer. The received revolution clock is transmitted to the DFE to serve as a time reference for the DSP engine.

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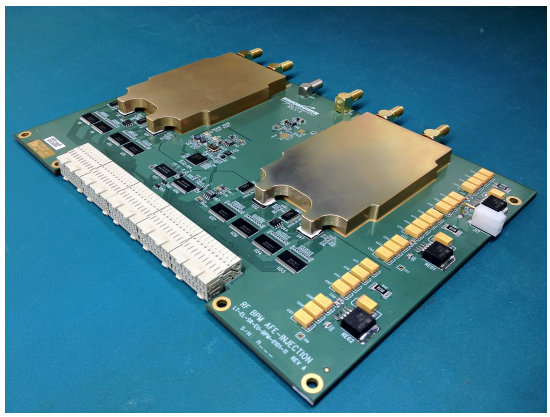

Figure 2: Analog Front End (AFE).

Digital Front End (DFE)

The DFE is responsible for all DSP of the button signals and communication of the results with the control system. The DFE is based on a Xilinx Virtex-6 Field Programmable Gate Array (FPGA). The fixed-point DSP engine calculates TbT position based on a single-bin DFT algorithm. FOFB 10KHz data and 10Hz slow acquisition data are derived directly from the TbT calculation [1].

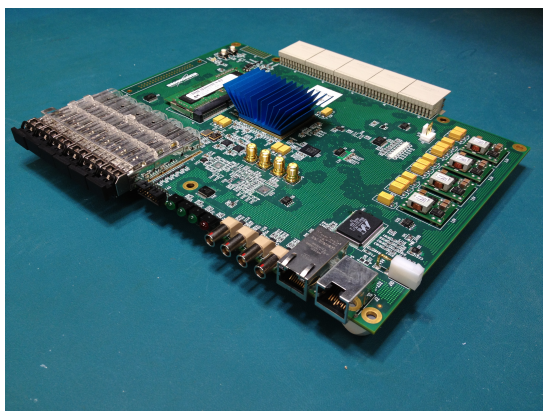

Figure 3: Digital Front End (DFE).

Pilot Tone Combiner (PTC) Module

The PTC is a custom design consisting of an RF board mounted in an aluminium housing. The PTC is mounted in the tunnel directly below the BPM pickups. A pilot tone generated on the AFE is coupled to the forward beam signals.

The PTC is characterized by comprehensive S-parameter measurements. S21 channel-channel variations are removed via automatic calibration routine, which maps the pilot tone to the received beam signal via measured S21. Post calibration results of TbT data are illustrated in Figure 5. Higher dispersion above 20dB of receiver attenuation is a result of reduced SNR. Longer calibration records could compensate this for. However, it is unlikely this amount of receiver attenuation will be necessary.

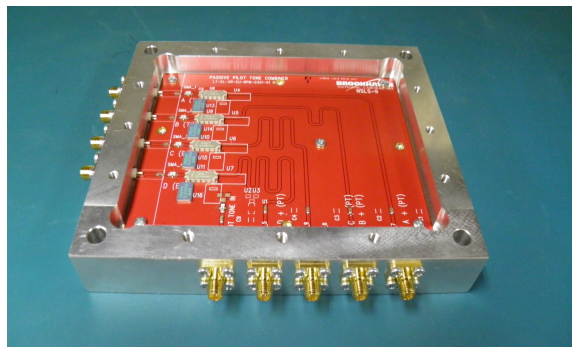

Figure 4: Pilot Tone Combiner (PTC).

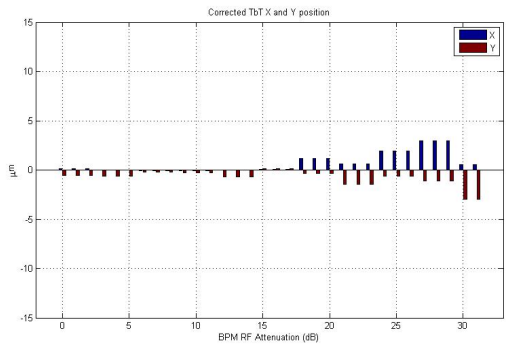

Figure 5: Static gain calibration.

PRODUCTION TEST

Overview

The RF BPM is currently in full scale production. Board level and system tests are automated via Matlab scripts which communicate to the BPM via TCP/IP using Mathworks Instrumentation Control Toolbox.

AFE Testing

It is necessary to connect the AFE to a dedicated DFE to parametrically configure AFE clock synthesizer, pilot tone and RF attenuators for testing. An automated Matlab script is run to quantify performance. Results are captured and stored in PDF or HTML format using Matlab publishing feature. The BPM laboratory is equipped with NSLS-II timing system and identical NSLS-II network configuration to enable comprehensive system level testing. A comprehensive set of tests on each unit ensure performance including; power spectral density, phase noise, and ADC histograms. System tests are run via EPICS to test end-to-end network communications and IOC functionality. Test time is 15min per AFE.

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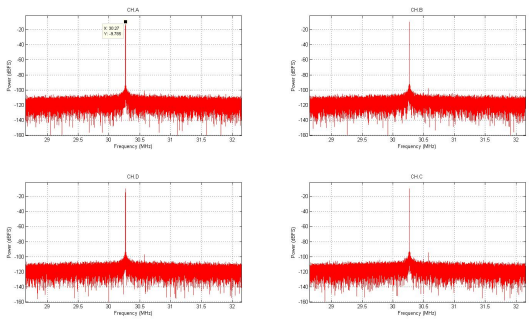


Figure 6: FFT or 1M ADC Samples.

Shown in Figure 6 is an FFT of 1M raw ADC samples with receiver attenuation set to minimum 0dB setting. The receiver is also quantified using a histogram of the raw ADC data. The discrete structure of the ADC histogram shown in Figure **7** is a result of coherent synchronous sampling. An ADC histogram with system not phase locked is also captured to check for missing codes.

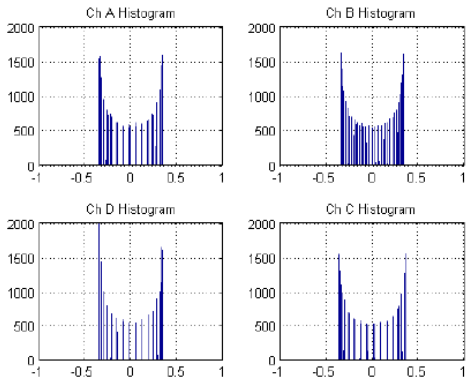


Figure 7: Histogram of ADC samples.

The phase noise of each AFE is measured at the ADC phase noise test port (spare PLL clock output) using Rhode & Schwartz FSUP8. An R&S SMA100 was used as the master oscillator to the timing system. Typical measured RMS jitter is 700fs.

DFE Testing

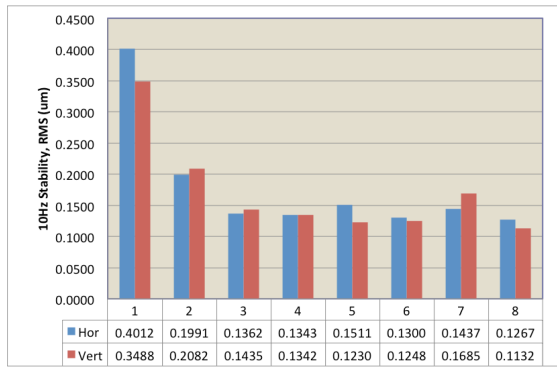
Comprehensive testing of the DFE is also performed via automated Matlab scripts with the DFE connected to a "golden" AFE. All features of the DFE are tested and captured in Matlab report. Test time is 30 min per DFE, 15 min dedicated to loading firmware.

LONG TERM STABILITY

The NSLS-II RF BPM achieves the 200nm long-term stability goal by minimizing time-varying thermal dynamic influences [2]. Long-term stability (i.e. 8hrs) has been demonstrated by thermal regulation to +-0.1°C without active dynamic correction. An active pilot-tone algorithm to provide further correction is implemented in hardware. The correction algorithm is currently under development.

Long-Term Stability Test Results

Thermal stability tests are conducted by placing the BPM electronics inside the thermally stable rack. Power splitters and cables are also placed inside the rack. A Matlab program has been developed which streams 10Hz data from DFE 80hr circular buffer for analysis.



	1	2	3	4	5	6	7	8
Hor	0.4012	0.1991	0.1362	0.1343	0.1511	0.1300	0.1437	0.1267
Vert	0.3488	0.2082	0.1435	0.1342	0.1230	0.1248	0.1685	0.1132

Figure 8: Measured 10Hz Stability (8hr), without Pilot-Tone.

The top location of the rack consistently yields the highest stability dispersion. We are currently investigating to determine if this is related to thermal dynamics of the rack configuration.

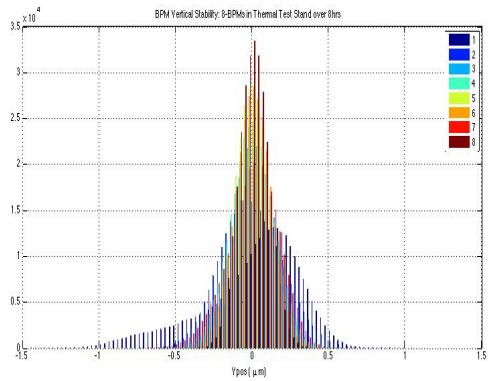


Figure 9**:** Vertical 8hr stability (10Hz data).

Figure 10: Thermal Test Rack (20-BPMs shown).

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SUMMARY

The development of a sub-micron BPM for the NSLS-II has successfully demonstrated performance and stability. The production of 60 Injection BPMs has been completed two months ahead of schedule. An additional 15 units have been produced for R&D. Production build of 240 Storage Ring units is currently under way.

ACKNOWLEDGEMENT

We would like to thank Marshall Maggipinto for his exceptional technical support that has played a significant role in the success of this program.

REFERENCES

[1] K.Vetter et al., "NSLS-II RF Beam Position Monitor", PAC11, New York, March 2011

[2] B. Kosciuk, et al., "Optimizing The Thermal Management of NSLS-II RF BPM", Proceedings of BIW 2012, Newport News, VA

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