DIGITAL SIGNAL PROCESSING FOR BUNCHED BEAM INTENSITY MEASUREMENTS*

N. Liu#, A. Ibrahim, A. Semenov, M. Wendt, Fermilab, Batavia, IL 60510, USA

Abstract

Intensity measurements of bunched beams are typically based on AC-coupled toroidal transformers (toroid) or broadband resistive wall current monitors (RWCM). Read-out technologies based on an in-house designed 8 channel VME digitizer board are presented. This paper gives an overview of the entire measurement system, discusses the hardware and performance of the 125 MS/s digitizer, and provides details on the FPGA-based digital signal processing. We present the different FPGA algorithms, applied for single- and multi-bunch beam intensity measurements in pulsed proton or electron linacs, as well as beam-lines.

INTRODUCTION

To ensure, the beam intensity remains close to pre-determined levels, beam intensity monitors with magnetically-coupled toroidal pickups are used as a non-interceptive method to measure the total transferred intensity in the H^- linac and transport lines at Fermilab. The beam intensity monitor basically consists out of the toroid assembly, as well as the signal conditioning and processing circuits. The toroid pickup is inserted around the beam tube with a ceramic insulator, and follows basic transformer theory (see Figure 1).

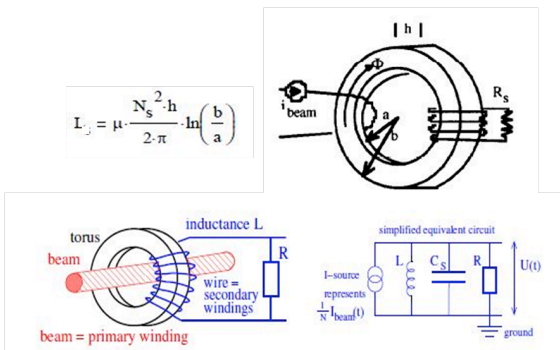

Figure 1: Toroid-based beam current measurement.

Followed by a simple low-pass filter / gain stage, an in-house designed digitizer board is used for digital signal processing and data acquisition of the toroid waveforms. The digitizer is a 6U VME board and has 8 analog input channels with selectable AC or DC coupling. On-board ADC chips are capable of a sampling rate up to 125MS/s. A programmable clock distribution circuit offers flexible timing configurations. Other elements on the board are the Cyclone III FPGA chip for signal processing, and 192MB of DDR2 memory for data buffering (see Fig. 2).

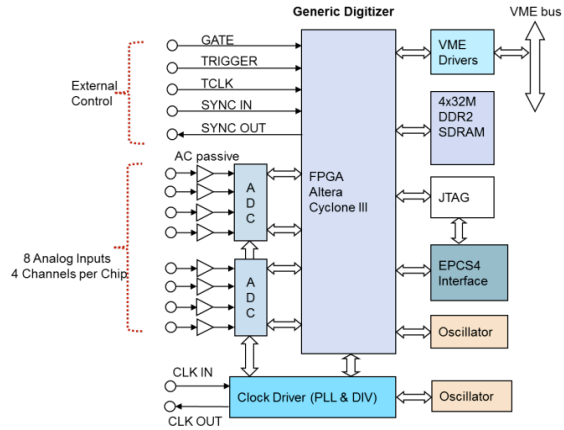

Figure 2: 8 channel VME 125 MS/s VME digitizer.

The FPGA firmware includes both, design blocks for standard infrastructures, as well as user specific applications. Standard support infrastructures include algorithms for data packaging for the analog-to-digital converter (ADC), for handling beam sync signals, and for configuring hardware components on the digitizer through the serial interface. The user-specific applications are reflected within the data processing scheme.

TOROID SYSTEM

The beam intensity, or number of charged particles in the beam, has to be monitored and must be kept within pre-determined safety and operational envelopes, i.e. by assuring all beam within a few percent is transported throughout the beam-line. At Fermilab beam intensity signals are detected using several magnetically-coupled toroidal pickups along the transport lines, to provide a non-destructive method to measure the total transferred intensity. Most transport lines are equipped with a minimum of two of these intensity monitors.

- The first part of the monitor is the beam pickup, i.e. the toroidal magnetic core, including its mechanical assembly, ceramic gap, shielding, etc., as part of the beam vacuum system within the tunnel enclosure. A ceramic insulator provides an electric break in the metallic vacuum chamber. This gap along the beam tube allows magnetic and electric fields of the beam to locally exit the beam pipe, and forces wall currents to find a path outside the vacuum chamber. The toroid couples to the magnetic field components of the beam, i.e. detects the beam intensity. The support and shielding structure provides a well-defined path of low impedance for the wall currents.
- The second part of the beam intensity monitor is the signal conditioning and processing of the toroid's output signal, as described in the next section.

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#ningliu@fnal.gov
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The toroidal pickup follows the basic transformer theory. Passing through the center of the toroid, the beam forms a single-turn primary coil of the transformer. An N-turn secondary coil is wound around the core, and the induced voltage is measured across a burden resistor which terminated the secondary winding (Figure 1).

The toroidal pickups installed at Fermilab have a limited bandwidth, typically substantially lower than the RF beam spectrum. As a result, most of the bunch time structure, i.e. bunch-by-bunch information, is lost. Thus, the waveform of the toroid signal reflects the "envelope" of the beam pulse (Figure 3). Using both, *Ohm*'s law and transformer relationships, the amplitude of macro-pulse is linear with the respect to the beam current within the bandwidth of the toroid. Furthermore, this relationship can be written in terms of the pickup's sensitivity or transfer impedance:

$$Z_{\text{toroid}}(\omega) = \frac{V_{\text{out}}(\omega)}{I_{\text{beam}}(\omega)} \quad (1)$$

A preamplifier may be added to provide additional gain to increase the toroid signal, such that the dynamic range of the readout provides the best resolution for the system. Consequently, the amplitude of the toroid signal at the digitizer input is the product of, the pickup's sensitivity and the preamplifier gain.

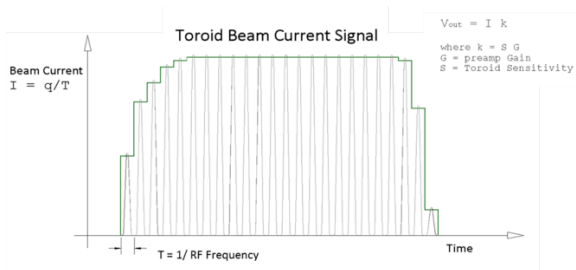

Figure 3: Processing the envelope of the toroid's beam current signal.

After acquiring the toroid signal, the electronics' primary function is to integrate the macro-pulse envelope signal to provide total beam intensity, and / or average beam current. The total beam intensity, or number of particles per beam pulse N can be calculated from Q_{total}, divided by the charge per particle e=1.602e-19 As.

$$\text{Total Beam Intensity}, N = \frac{Q_{\text{total}}}{e} \approx \frac{T}{k\,e}\sum_{n=0}^{M} v_n \quad (2)$$

The average current of the transferred beam pulse can be computed as:

$$\text{Beam Current}, I_{\text{AVG}} = \frac{Q_{\text{total}}}{\text{PW}} \approx \frac{T}{k\,\text{PW}}\sum_{n=0}^{M} v_n \quad (3)$$

where PW is the width of the measured beam macro-pulse. The macro-pulse width is determined by "edge detectors", implemented within the FPGA firmware.

Although the toroid's output is AC-coupled, therefore has no DC response, additional digital filtering and / or algorithms, e.g. baseline correction, may be needed to improve signal-to-noise ratio, linearity and accuracy of the reported, calibrated beam intensity, etc.

THE DIGITIZER

Used for both, data acquisition and signal processing, the 125MS/s digitizer is implemented on an in-house designed 6U VME board. Figure 2 shows the simplified diagram of the digitizer board.

There are eight analog input channels; each can be configured either for AC, or for DC coupling. The DC coupled input has two stage pre-amps from Analog Devices, with a bandwidth of 2.3GHz at unity gain. These provide differential inputs centered at DC level. AC coupled inputs use two-stage ADT1-1WT transformers from Mini-Circuits, with bandwidth from 400kHz-800MHz. The full scale input range, in either configuration, is +/- 1.15V.

The digitizer is equipped with an clock distribution circuit which can reference to the on-board oscillator or external clock source. A clock driver chip, programmable through the FPGA, provides a flexible clock source for different applications. Input signals are sampled by two ADS6445 analog-to-digital converters (ADC) which can sample at a rate of up to 125MS/s.

An Altera Cyclone III FPGA chip is used for hardware configuration and on-board data processing. The FPGA algorithms provide smart timing schemes with external trigger, gate and sync inputs.

There are also 192MB of DDR2 SDRAM for data buffering.

SINGAL PROCESSING IN THE FPGA

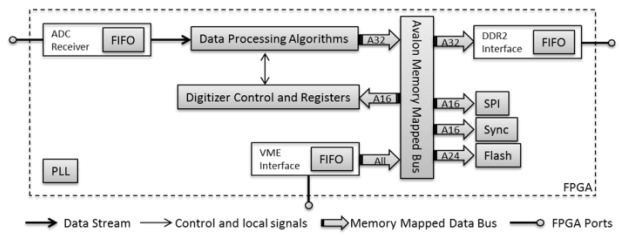

Figure 4: Simplified data flow.

The FPGA firmware can be divided into two coding categories. One supports the basic infrastructure required for any general application: an ADC data receiver, a VME bus driver, a memory driver, a serial port interface and a sync signal decoder for smart triggering. The other supports application specific algorithms.

The connection between these design blocks was developed using the SOPC builder tool provided by *Altera*, the FPGA manufacturer. The above block diagram gives a simplified view of data flow between the various design blocks. The actual interfaces between the blocks follow guidelines of the Avalon Memory Mapped data bus and the Avalon Streaming data interface (Figure 4).

Timing Schema

There are three clock domains in the firmware design. The ADC data processing is clocked at the same rate as

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the sampling frequency. General control blocks and the data bus operate at a separate clock rate from an on-board oscillator. The DDR2 memory interface is clocked at higher rate than the sampling frequency for improved data buffering performance.

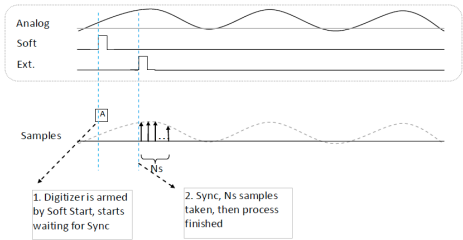

Figure 5: Timing Diagram for data processing.

To synchronize these clock domains, an external trigger is used. After arming the digitizer by a software command, the data processing algorithms are started by the external beam sync trigger signal. When the processing is finished, the digitizer returns to its default state and waits for the next sync pulse (Figure 5).

Waveform data from all eight channels are processed in parallel. For each channel the sampled raw data are converted from serial to parallel and then packaged into a 16-bit data format.

Toroid-Based Beam Intensity Measurements

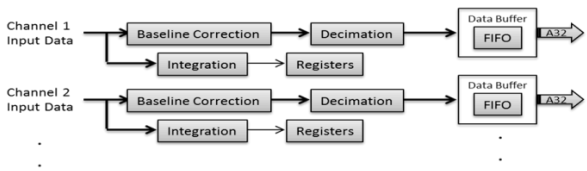

Figure 6: Simplified data path for the digitizer.

The toroid-based beam monitoring system provides the total beam intensity and the average current to the Fermilab AcNet control system. The beam intensity values are the result of both, integration and baseline correction algorithms. The average beam current is evaluated as result of an edge detection algorithm and the beam intensity calculations.

Furthermore, the acquired toroid data is corrected for the baseline-shift of the input data and saved to memory for waveform readout by the control system applications. Data decimation can be applied as an option (Figure 6).

Trapezoidal Integrator

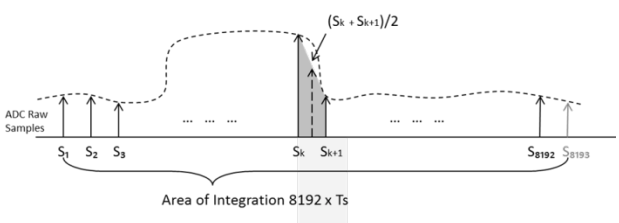

Figure 7: Trapezoidal integration.

To balance accuracy and complexity, the integrator uses the trapezoidal integration algorithm (Figure 8):

$$Int \approx \sum_{k=1}^{8192}\left(\frac{s_k + s_{k+1}}{2}\right) = \sum_{k=1}^{8192} s_k + \frac{s_{8193}}{2} - \frac{s_1}{2} \quad (4)$$

The implementation of the integrator includes a shift register. Consequently, trapezoidal integrations under the predetermined window size are calculated on every clock cycle (Figure 8).

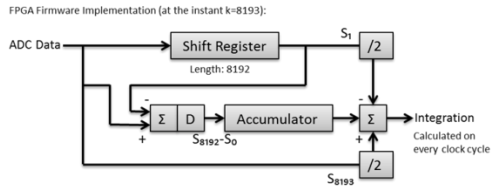

Figure 8: Implementation of the integrator.

Baseline Correction The raw data samples are integrated within time windows of predefined length, first for the baseline, and then followed for the beam pulse.

A first trigger event starts the integration for the baseline measurement, this integration time window is set prior to the actual beam pulse. Following, the baseline measurement the integration of the actual beam pulse starts. The difference of the two will give the baseline corrected beam pulse intensity.

The baseline corrected raw data is also saved to the memory. Decimation can be configured according to computing resource and requirements

Edge Detection An optional edge detecting procedure helps to detect the duration of the pulse. We calculate the average pulse level based on intensity calculation and edge detection. In our firmware implementation, a buffer keeps track of the variation of the baseline. When the input samples exceed the maximum recorded variation by a predetermined threshold, the front edge of the pulse is detected. The trailing edge of the pulse is detected in a similar way, after the signal drops below the recorded pulse variation by a preset ratio, the trailing edge is recorded. Having the two edges determined, the width of the beam pulse is calculated (Figure 9).

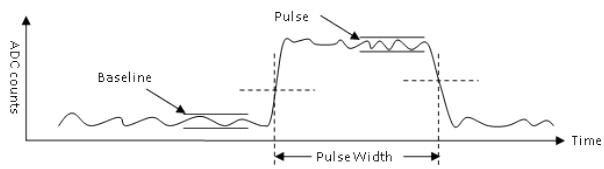

Figure 9: Edge detection of the beam pulse.

RESULTS AND CONCLUSIONS

A toroid-based beam intensity measurement system for linac and transport lines uses an in-house developed digital signal processing schema. Preliminary measurement results look very satisfactory.

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