# Radiation effects on Detectors and Electronics

Outline

- Radiation types and effects on silicon
- Radiation effects in detectors (bulk effects)
- Radiation effects on electronics
  - Bipolar
  - CMOS
  - SOI
- Single event effects
- Practical Considerations

My point of view – not an expert but a victim

# Radiation types

- Radiation
  - Electromagnetic ($\gamma$, $\beta$, x-ray).
    - Ionization, e-hole pair creation.
  - Hadronic (n, $\pi$, p). Damage to the bulk material caused by displacement of atoms from lattice sites in addition to ionization
- Electronics are affected primarily by ionization
  - Charge buildup in insulating layers
  - Charge injection into sensitive nodes
- Sensors are affected by bulk damage and ionization
  - Crystal structure damage
  - Introduction of traps
  - Introduction of mid-band states

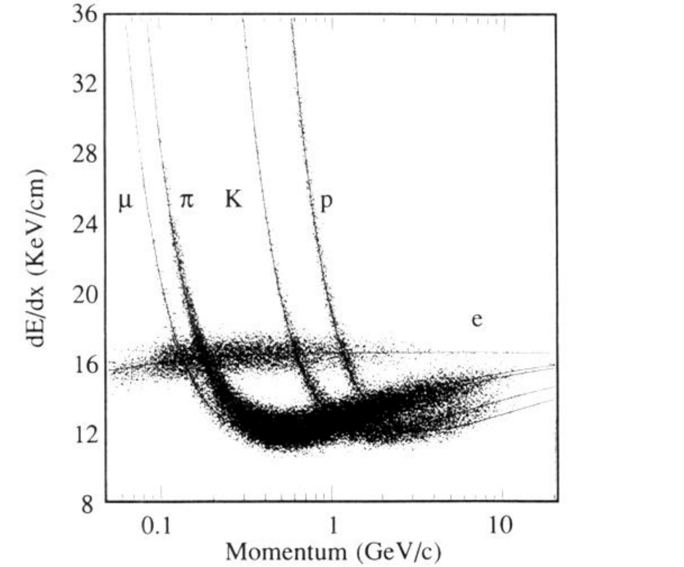
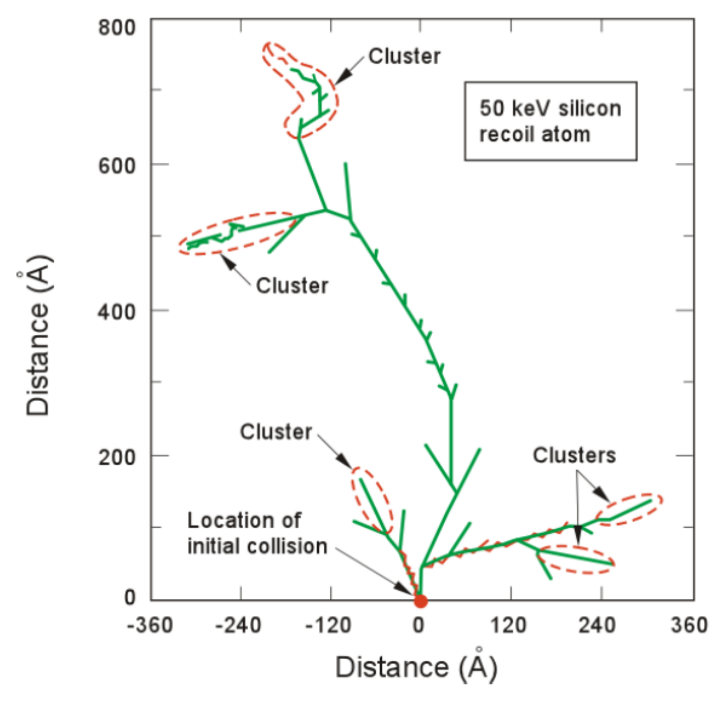


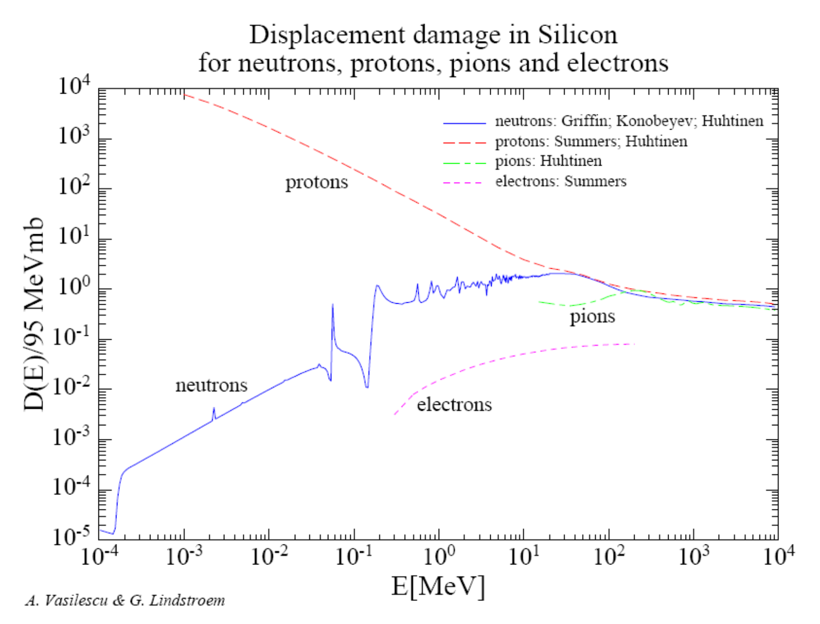

FIG. 2. Distribution in $dE/dx$ vs momentum for particles in multihadron events. Lines indicate the predicted average $dE/dx$ as a function of momentum for different species.



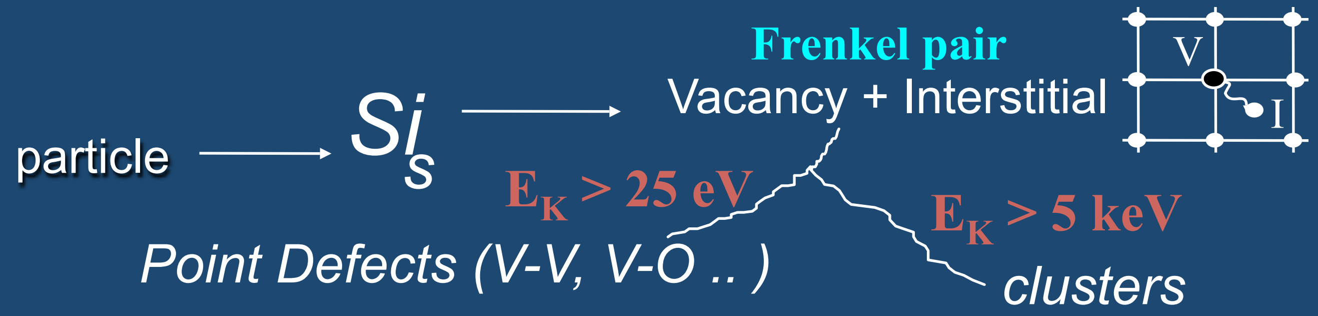

Ref 1.

# Displacement Damage in Silicon

- Displacement of atoms in the crystal lattice
  - Described by displacement damage (MeV mb) or Non Ionizing Energy Loss (NIEL - keV$cm^2$/g) in the material
  - For silicon 100 MeV mb = 2.144 keV $cm^2$/g
  - Typically scaled to NIEL values for 1 MeV neutrons for various types, energies
  - Pattern of damage clusters depends on particle type and energy
    - NIEL scaling not always valid
    - Differences between neutrons, protons, and pions can be significant
  - Damage leaves vacancies (empty lattice sites) and interstitials
    - These can be electrically active
    - Charge traps
    - Leakage current sources
    - Combine with oxygen and other impurities



# Production of Vacancies and Interstitials

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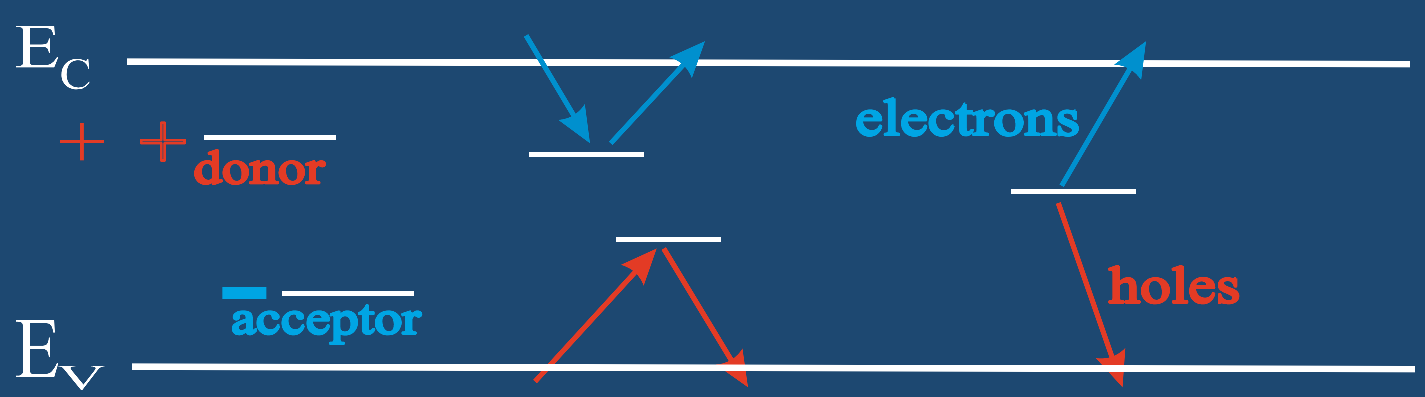


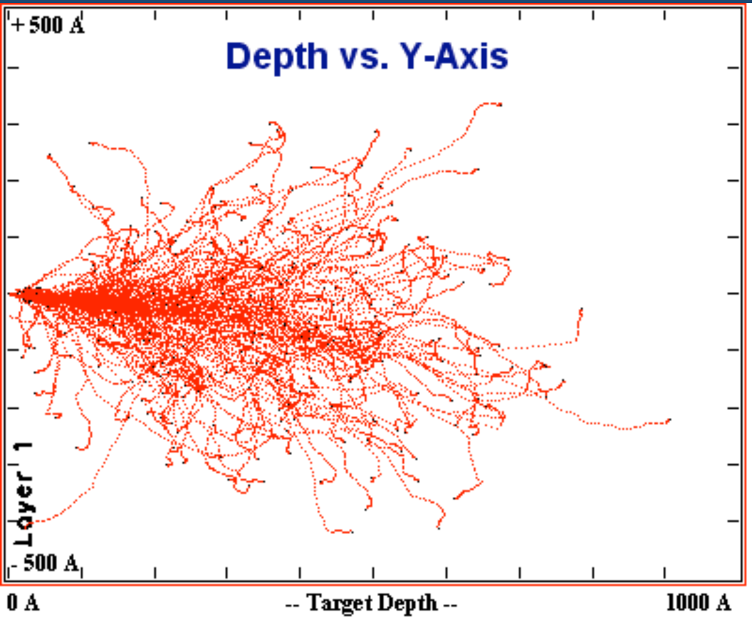

**charged defects**
**⇒ $N_{eff}$ , $V_{dep}$**
e.g. donors in upper and acceptors in lower half of band gap

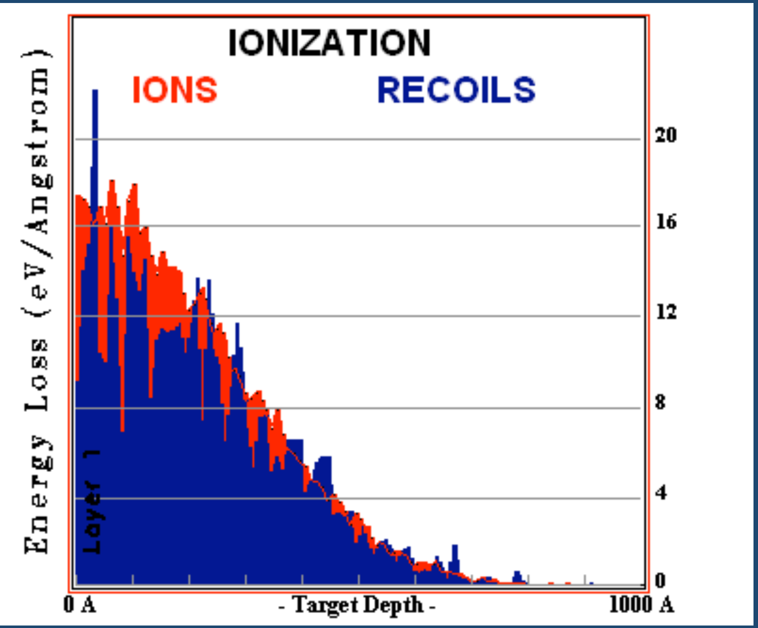
**Trapping (e and h)**
**⇒ CCE**
shallow defects do not contribute at room temperature due to fast detrapping

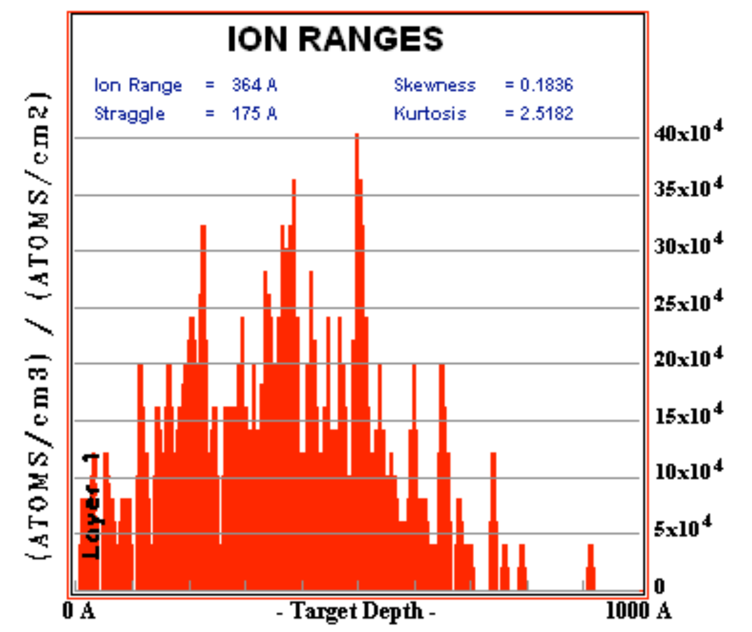
**generation**
**⇒ leakage current**
Levels close to midgap most effective

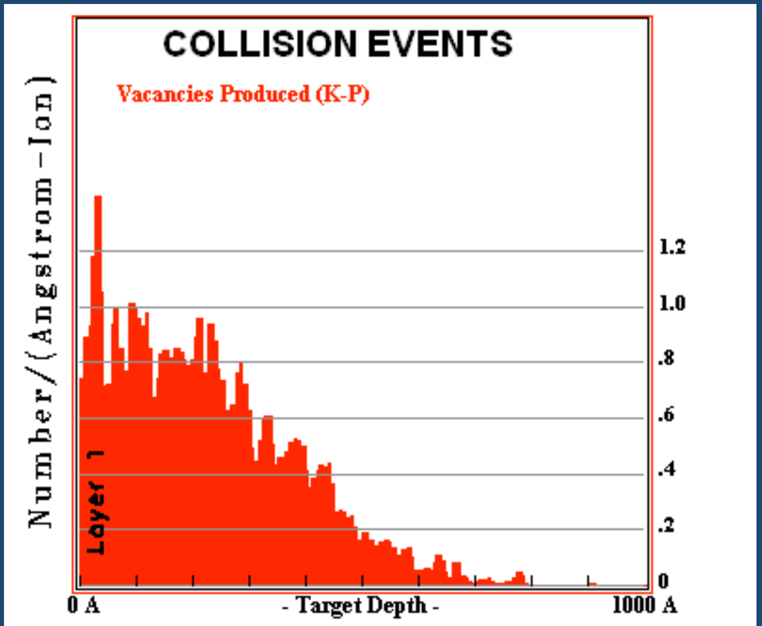
# Simulation of 25 KeV recoil

SRIM Simulation



# Radiation effects on Detectors

- HEP silicon *detectors* used at the Tevatron and LHC are primarily affected by bulk damage. Associated electronics are affected by primarily by ionization damage.
- Detectors are unique
  - Lightly doped silicon
  - Thick structures
  - Regular array of electrodes
- Several different bulk effects:
  - Increase in leakage current
  - Changes in doping concentration
  - Increased charge trapping
- All of these depend on time and temperature, sometimes in complex ways.

# Effects – Leakage current

Ref 3.

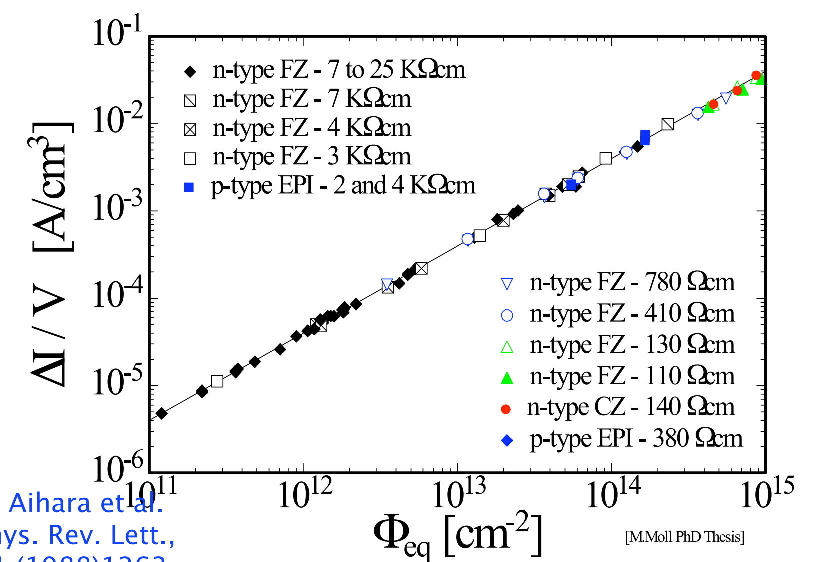
- Most obvious effect is an increase in device leakage current

$$I_{det} = I_0 + \alpha\,\Phi \times Volume$$
$$\alpha = 2 - 3\times 10^{-17}\ A/cm$$

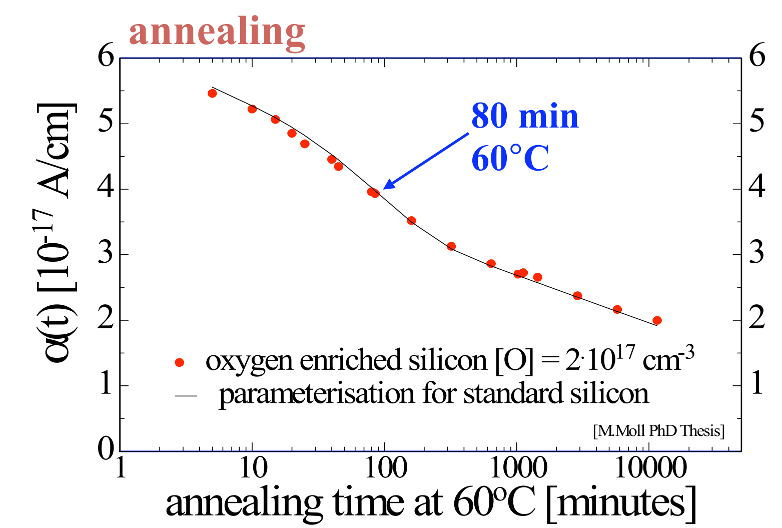
  - Almost universal effect
    - Dependent on NIEL
    - Independent of silicon resistivity and doping
  - Temperature dependent

$$I \propto T^2 \exp\left(-\frac{E_g}{2k_BT}\right)$$

  - There is a strong annealing effect

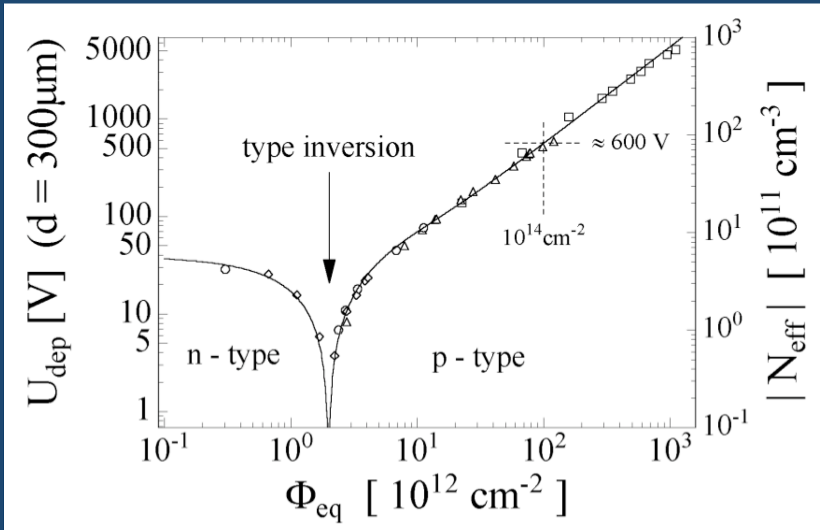



H. Aihara et al. Phys. Rev. Lett., **61** (1988)1263



# Effects – Space Charge Inversion

- SSC- era studies discovered an unusual effect detectors became more p-type with radiation exposure
- Two effects - donor removal and acceptor creation
- This effects limits the lifetime of detectors in high radiation environments.
  - Device becomes more p-type
  - Depletion voltage goes up
  - Detector eventually breaks down or draws too much current

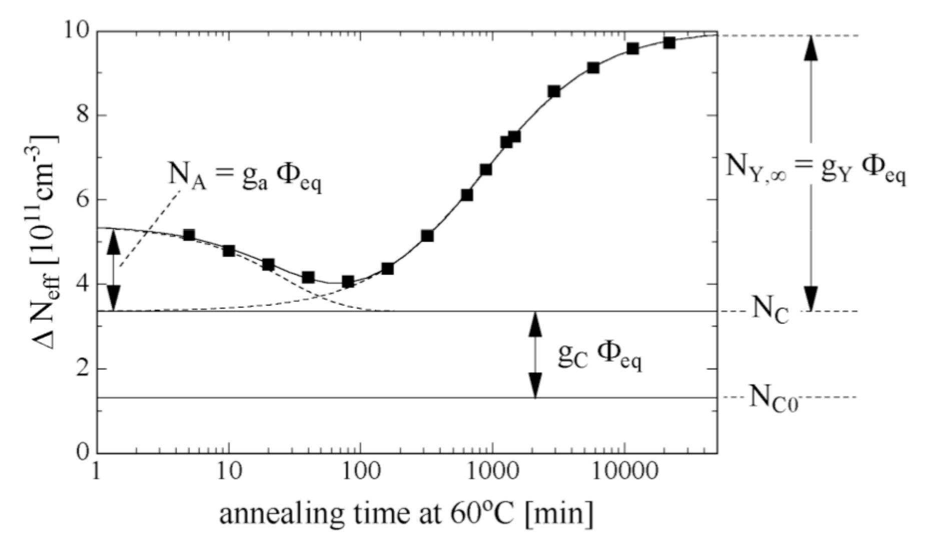



- Very carefully studied by LHC groups, which also explored variations in silicon geometry and doping to reduce the problem
  - Oxygenated silicon
  - Increase breakdown voltage by design
  - Single sided detectors
- Complex annealing behavior

# Annealing effects

$$N_{eff}(\Phi) = N_{d0}e^{-c\Phi} + g_c\Phi + g_s\Phi e^{-t/\tau(T)} + N_Y(\Phi, t, T)$$

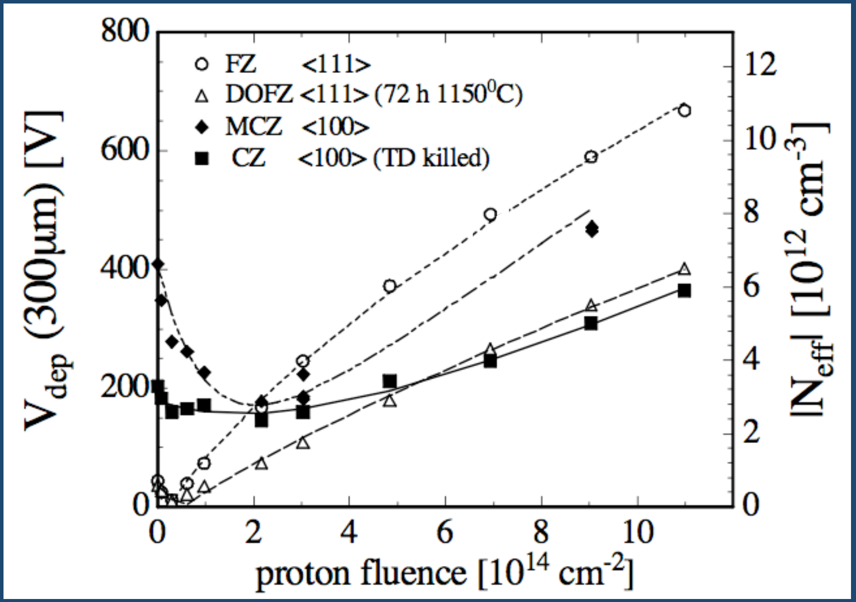
Donor removal | Acceptor creation | Beneficial annealing | Reverse annealing




- Short term: "Beneficial annealing"
- Long term: "Reverse annealing"
  - time constant depends on temp:
    - ~ 500 years (-10°C)
    - ~ 500 days ( 20°C)
    - ~ 21 hours ( 60°C)
  - Detectors must be cooled even when the experiment is not running!

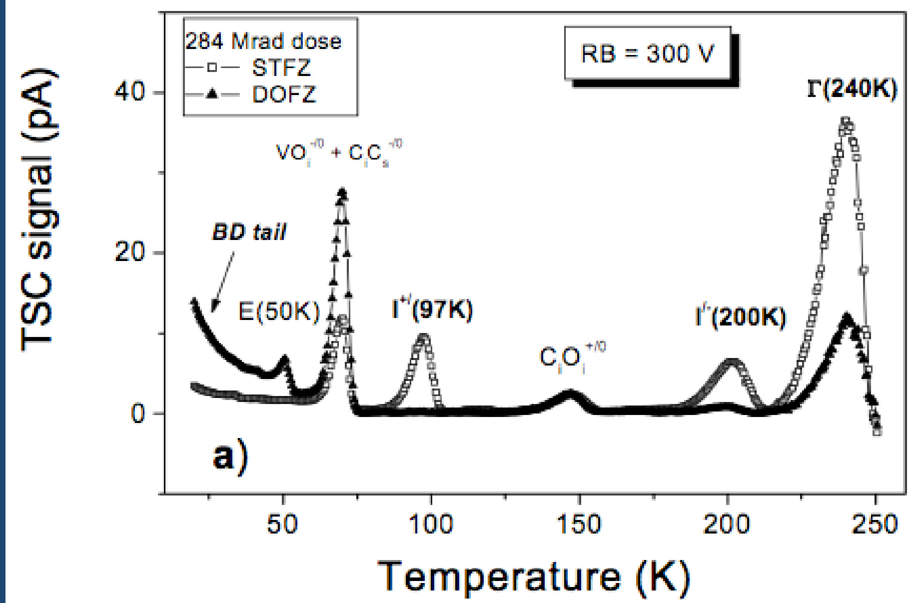
# Defect Characterization

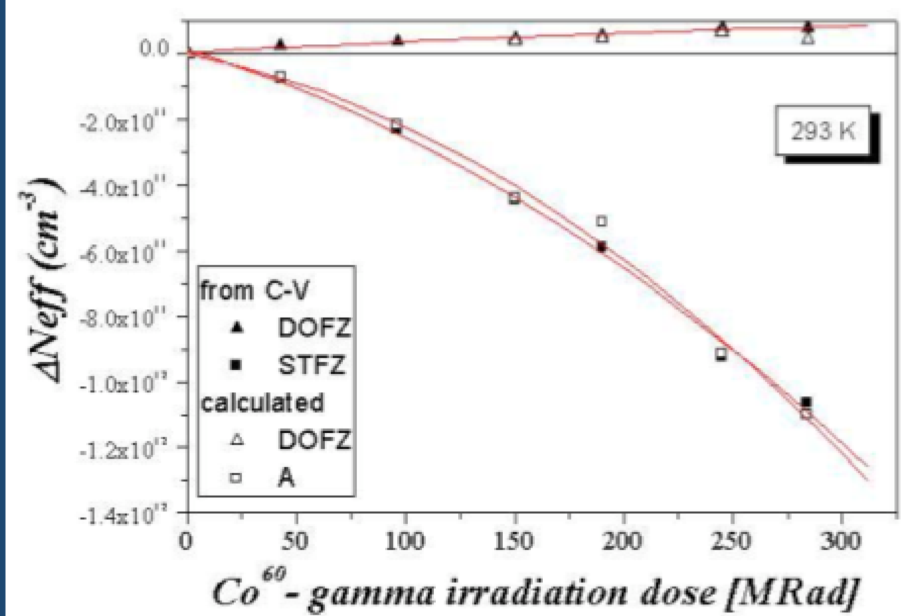
- RD 48 and 50 has had an ongoing program to understand and characterize radiation-induced defects
  - Engineered dopants (oxygen, carbon …)
  - Different materials
    - Magnetic Czochralski
    - Epitaxial silicon
    - Diffusion oxygenated float zone (DOFZ)
- Various beams (pion, proton, neutron)
- Results:
  - Oxygenation retards reverse annealing
  - MCZ does not undergo type inversion (original diode remains)
  - Epitaxial silicon similar to MCZ



# Trap Characterization

- Deep Level Transient Fourier Spectroscopy (DLTFS) and Thermally Stimulated Current (TSC) techniques
  - "I" and "Γ" defects differ with oxygen content
  - I defect identified with much of the space charge inversion effect
- Identification of DLTS states with specific defects difficult
  - I is probably $V_2O$
- Picture changes with cluster generating radiation, material
- Understanding at a basic level much better, but work ongoing



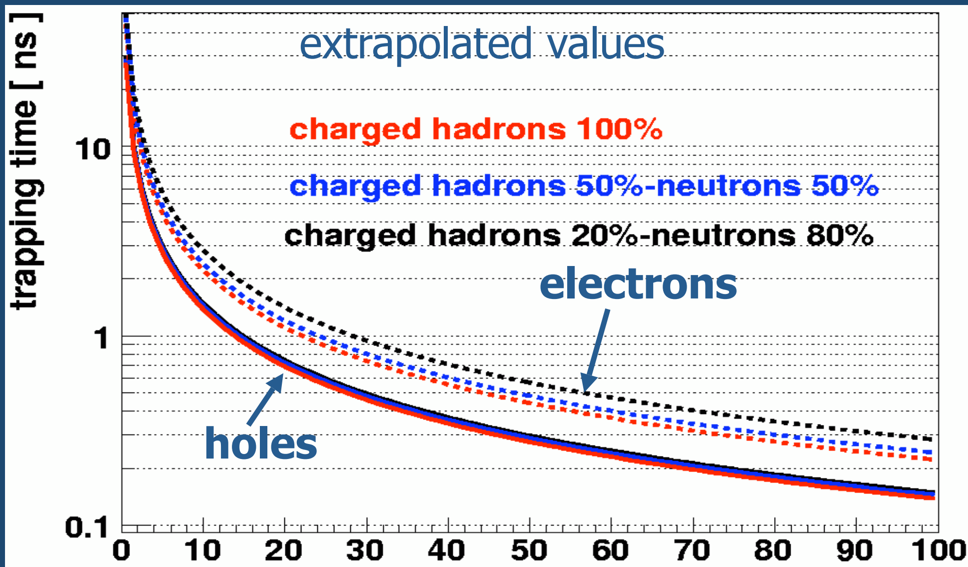

Point defects in Co60 irradiation
Ref 18

# Effects – Charge Trapping

$$\tau_{eff,e,h} << t_{drift}$$

$$\frac{300\mu m}{v_{sat}} \approx 3ns$$

- Particle detectors typically collect charge from a 200-300 micron thick substrate
- Bulk damage introduces traps which can intercept drifting charge.
- Effect depends on type of exposure
  - independent of material type (FZ, CZ, epi) and properties (std, DO, resistivity, doping type).
  - independent of irradiating particle type and energy
  - only small annealing effects (as studied up to T = 80°C)

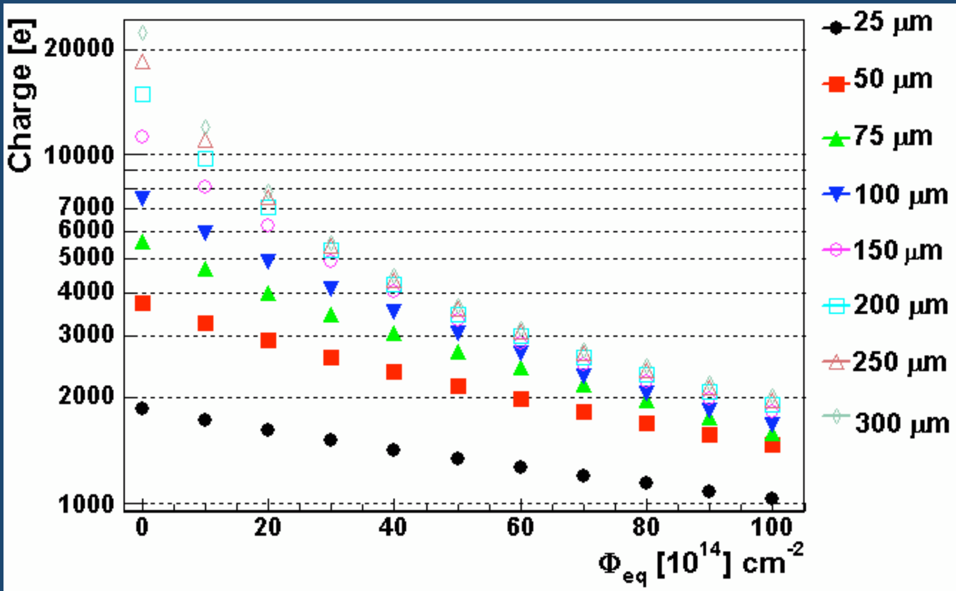


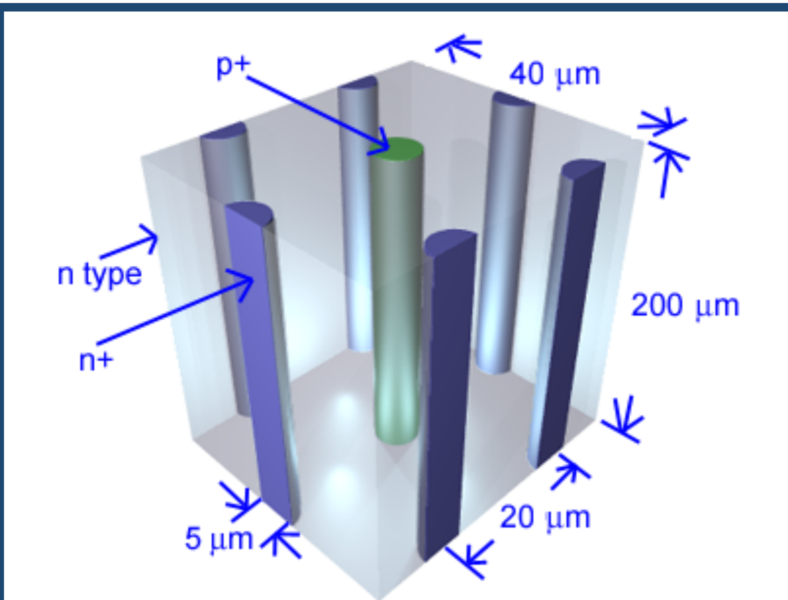

Ref 4.

- Can be reduced by reducing electrode spacing
  - Thinned detectors
  - $V_d$~thichness$^2$
  - 3D detectors with electrodes in silicon bulk.

# Sensor Design

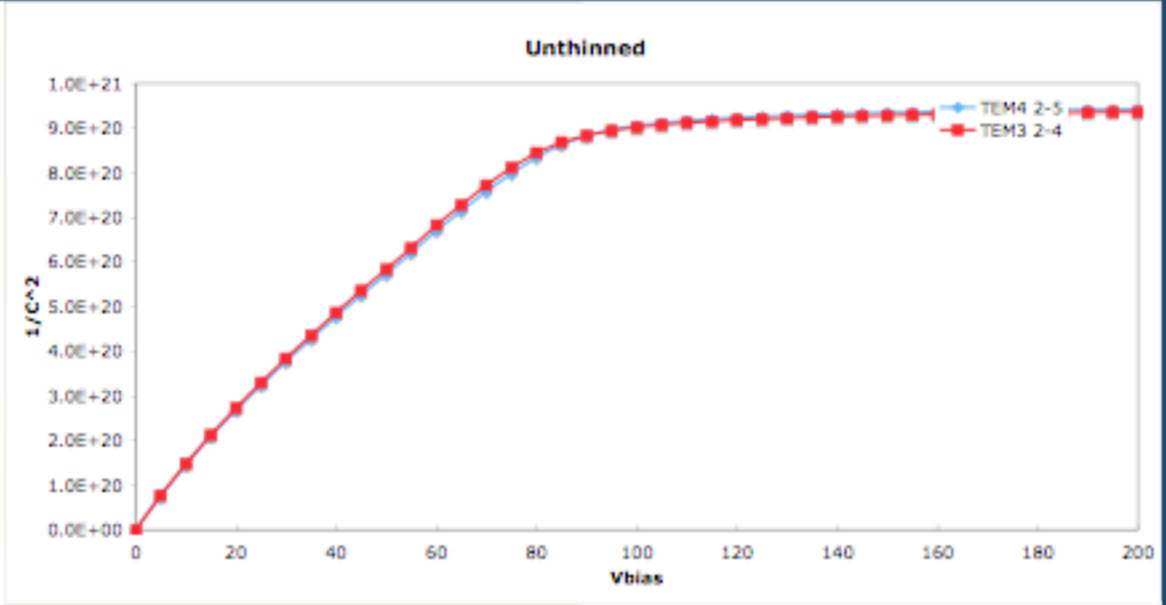
- Charge collection may be the ultimate limit to silicon radiation hardness at sLHC
  - Thinned sensors can collect as much charge as full thickness sensors at high dose
  - Voltage needed to deplete smaller ($\sim t^2$)
  - Smaller leakage current
  - Larger internal fields
  - Can use techniques from SOI and commercial thinning processes
- Can adapt deep reactive ion etching from nanotechnology to generate electodes in the silicon bulk, the effective thickness is the electrode spacing

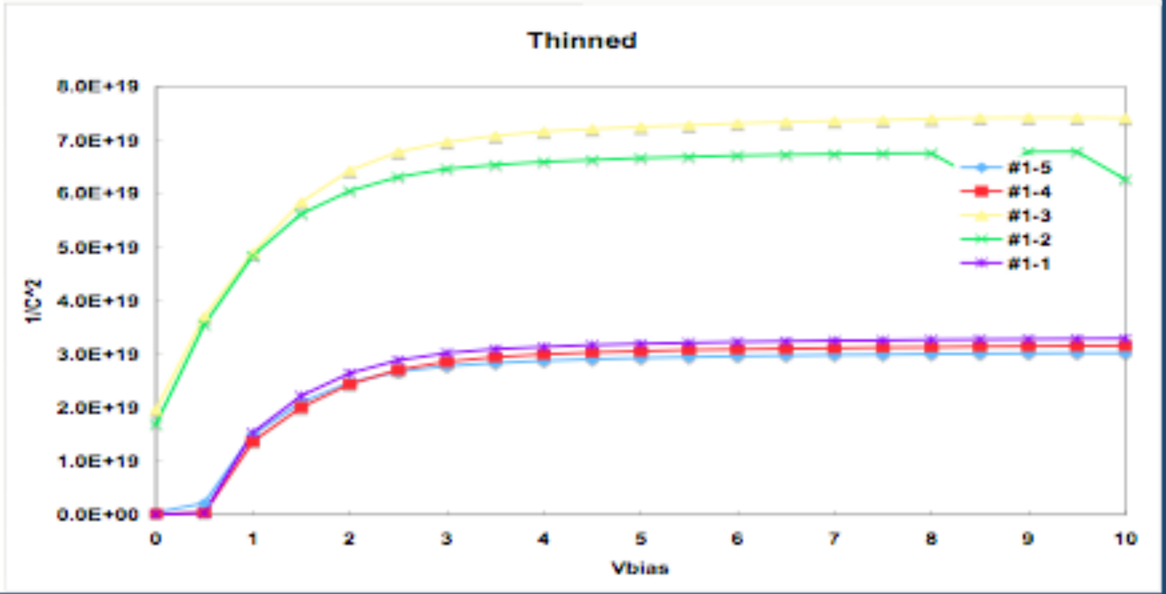


# Thinned Sensors

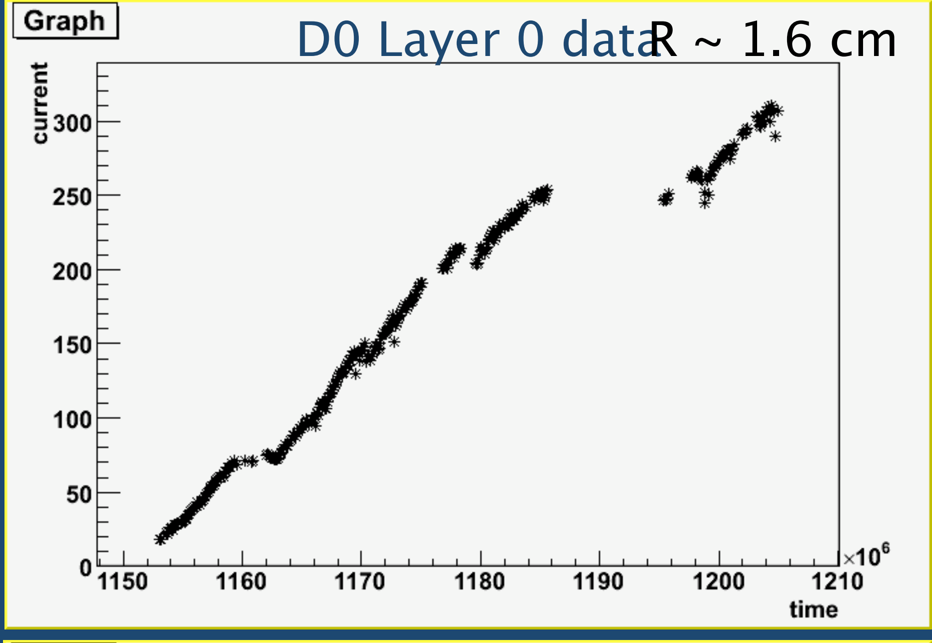
- Thinning techniques well developed in industry
- Challenge form backside contact without full 1000 deg anneal
- 280 micron 6” sensor
  - Mount on pyrex handle
  - thin to 50 microns
  - Backside polish
  - Ion implant
  - laser anneal
- $V_d$ ~ thickness$^2$
  90 V -> 2.8 V

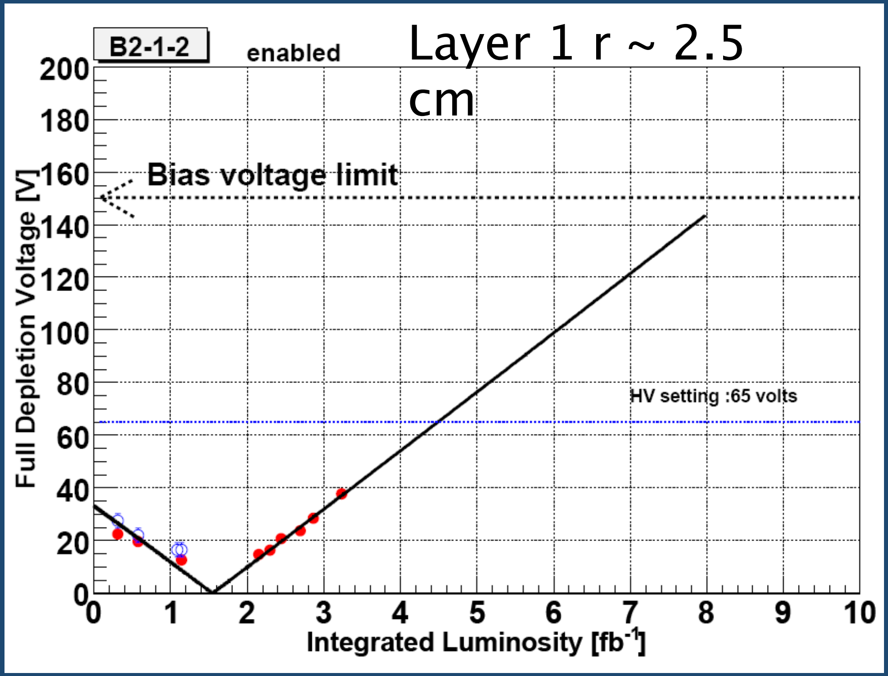


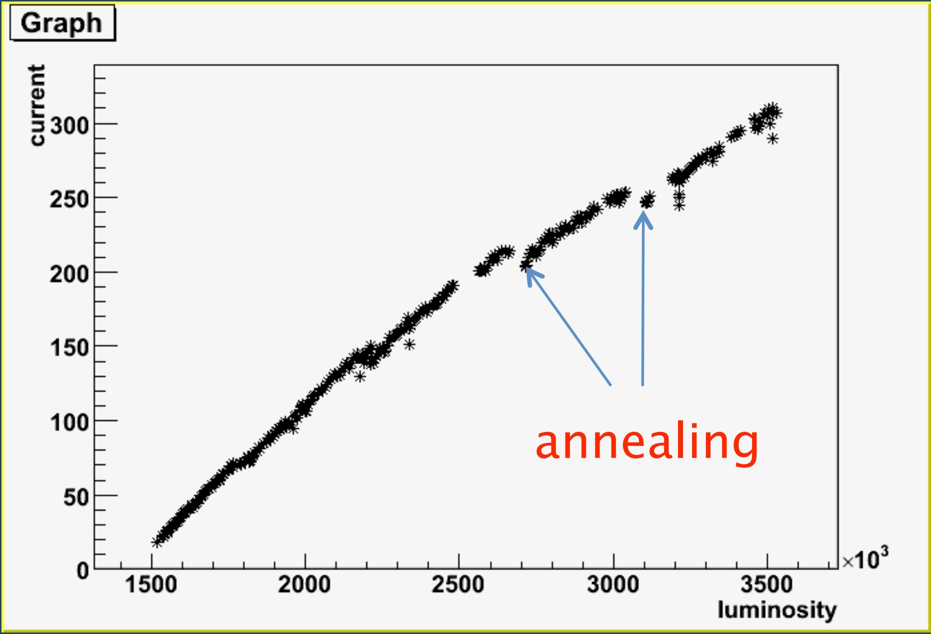



# Data From D0

- Preliminary on-line data from D0 monitoring system
- Silicon detectors running since 2000



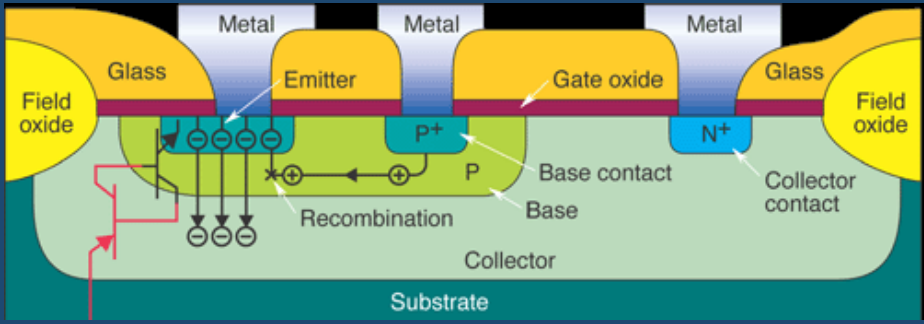



# Radiation Effects in Electronics

- Effects vary greatly with technology
- Characterized by
  - Changes in gain
  - Changes in noise
  - Changes in characteristics
  - Sensitivity to single ionizing events
- Technologies:
  - Bipolar transistors
  - FETs
  - Bulk CMOS
  - SOI
- Bulk CMOS is most universal

# Bipolar Transistors

(Ref. 6)




- Bipolar Transistors
  - Damage induces mid-gap states as in detectors
    - Traps reduce conduction current through the base
    - Reduced gain

$$\frac{1}{\beta_{DC}} = \frac{1}{\beta_0} + \frac{\Phi}{f_T} \qquad f_T = unity\ gain\ freq$$

  - Fractional change in doping due to radiation is small because initial doping is large ($10^{16\text{-}20}$) compared to detectors ($10^{12}$)
  - Noise remains ~constant but s/n falls due to reduced gain

Saturation of traps – increased gain

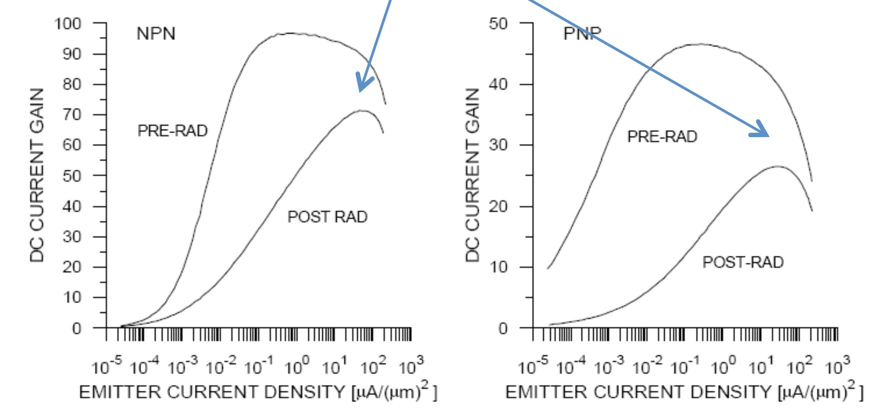
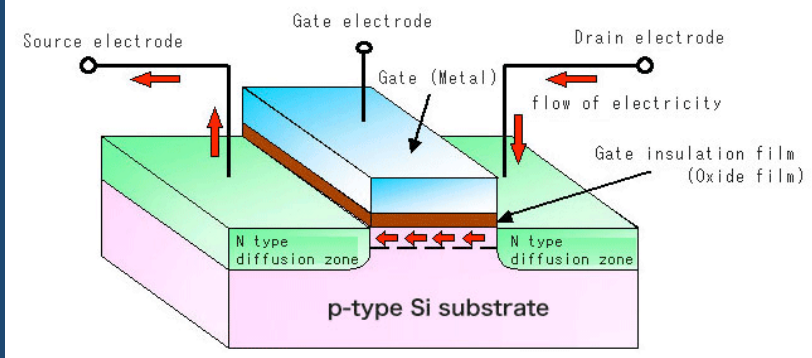



**FIGURE 4.** DC current gain of npn and pnp transistors before and after irradiation to a fluence of $1.2{\cdot}10^{14}$ cm$^{-2}$ (800 MeV protons).

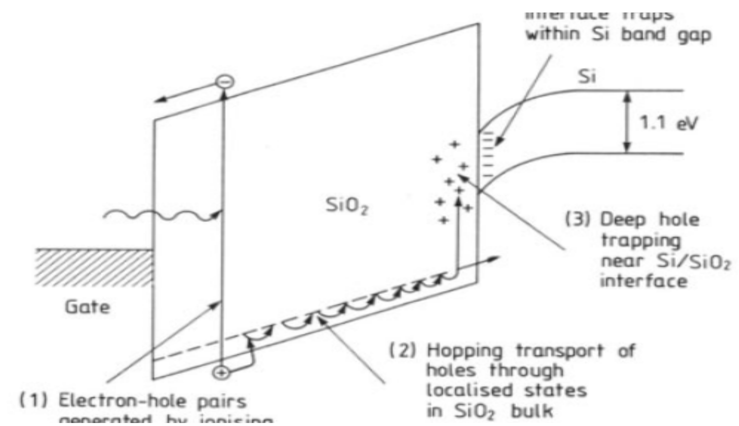
Ref 5

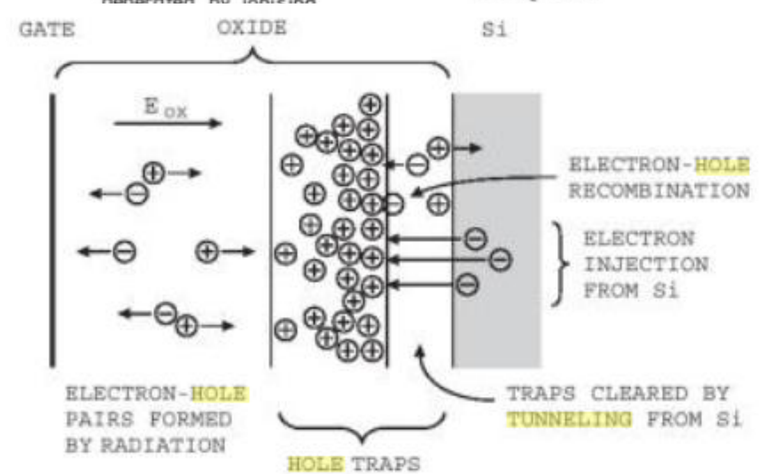
# MOS Transistors

- Radiation generates e-hole pairs in insulating oxides
  - Electrons are mobile and are removed by the gate-substrate field
  - Holes are trapped – either in the bulk or by deeper traps near the silicon-oxide junction
  - Holes can recombine with electrons from the silicon
  - Tunneling electrons recombine with holes near interface
- Oxide quality and geometry is crucial to radiation sensitivity of CMOS




Construction of MOSFET



# Threshold Shifts

- Large feature size CMOS threshold shifts were significant for “moderate” doses
  - Significant dependence on irradiation conditions (temperature, bias …)

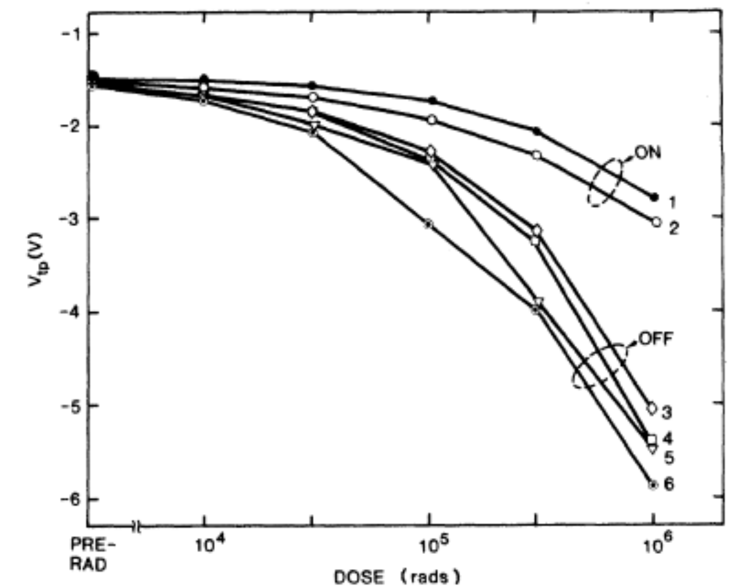



Figure 3. P-channel threshold voltage for each of the six bias configurations during irradiation.

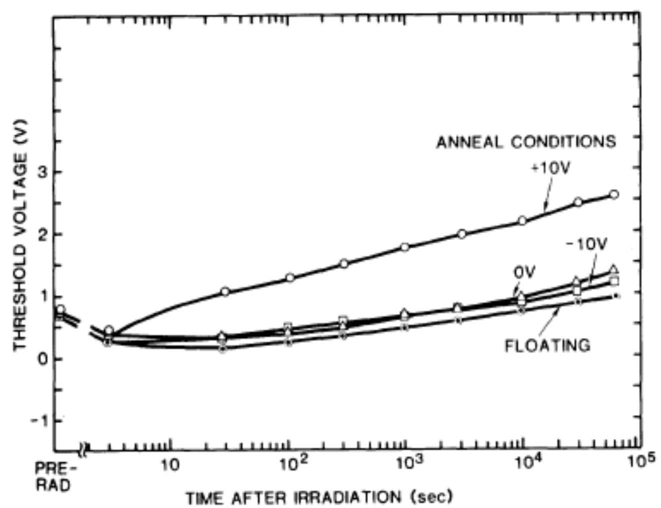



Figure 7. N-channel threshold voltage versus time after irradiation to $3 \times 10^5$ rads(Si), biased "OFF" during irradiation, with different anneal conditions.

Ref 8

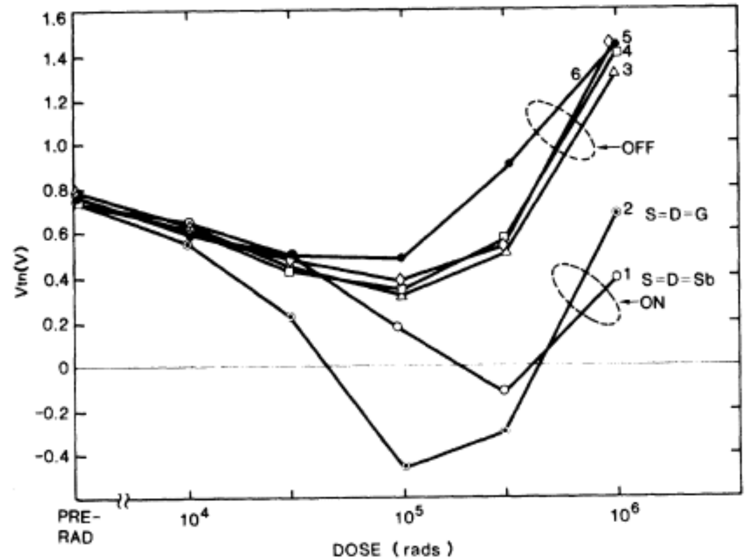
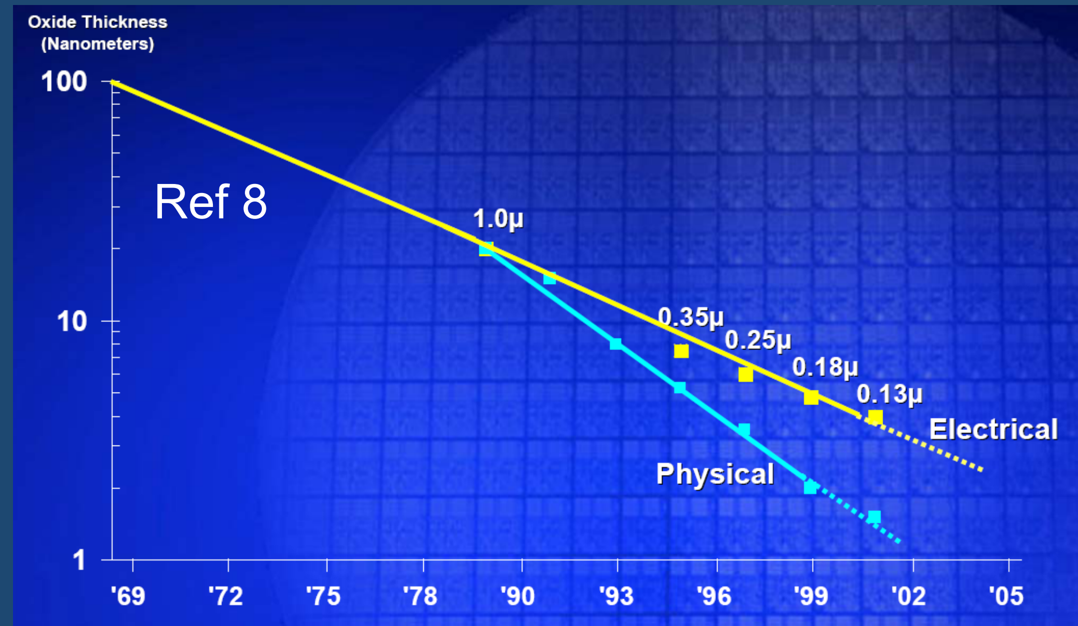
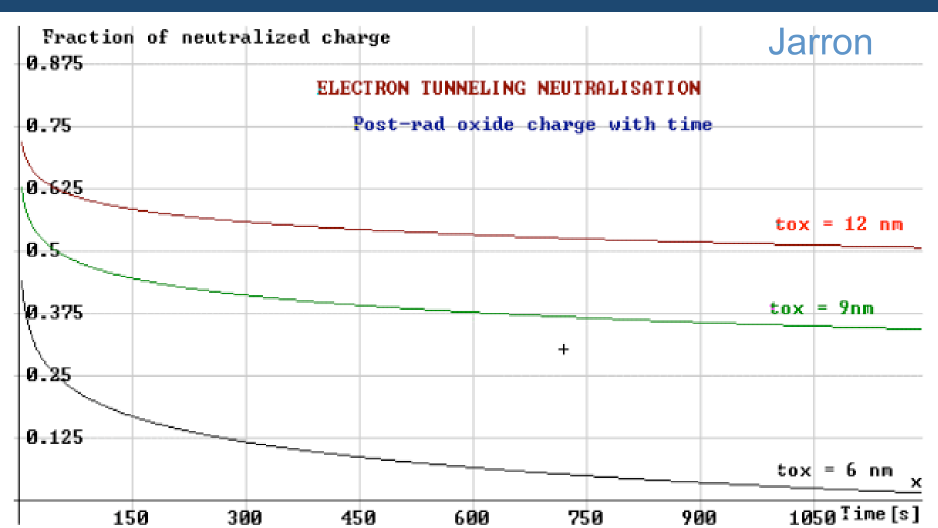


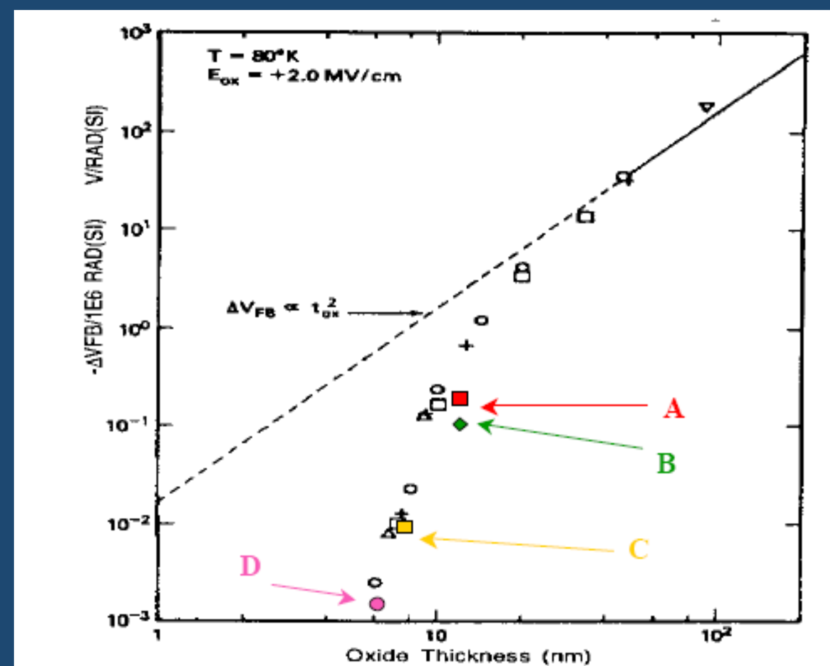

Figure 2. N-channel threshold voltage versus dose for each of the six bias configurations during irradiation.

# Oxide Thickness

- The thin oxides inherent in deep submicron technology provide naturally radiation tolerant transistors
- Quantum tunneling through the thin oxides in deep submicron processes drive the voltage shifts well below extrapolation from larger feature size technologies.



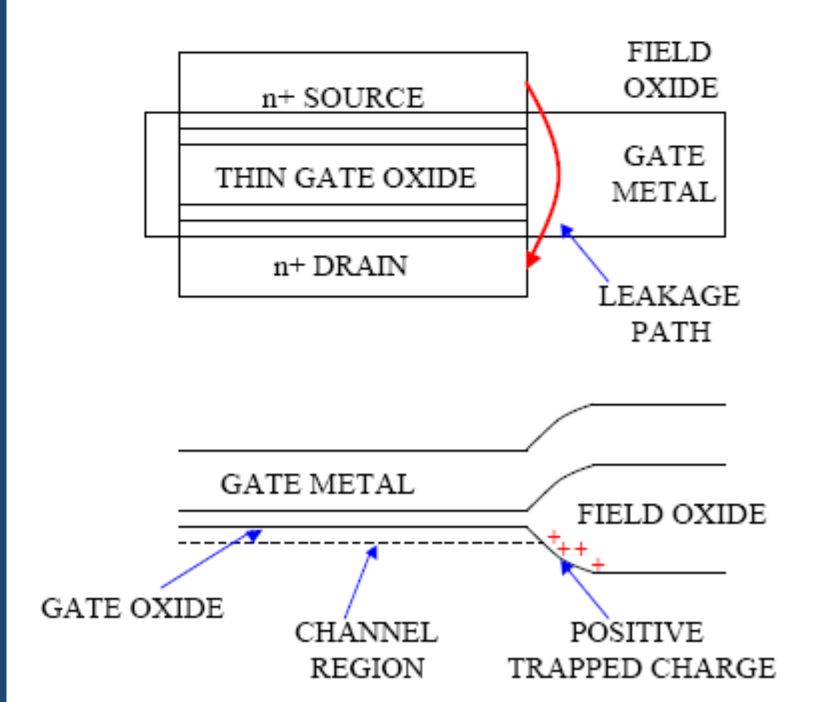




After N.S. Sacks, M.G. Ancona, and J.A. Modolo, IEEE Trans.Nucl.Sci., Vol.NS-31 (1984) 1249

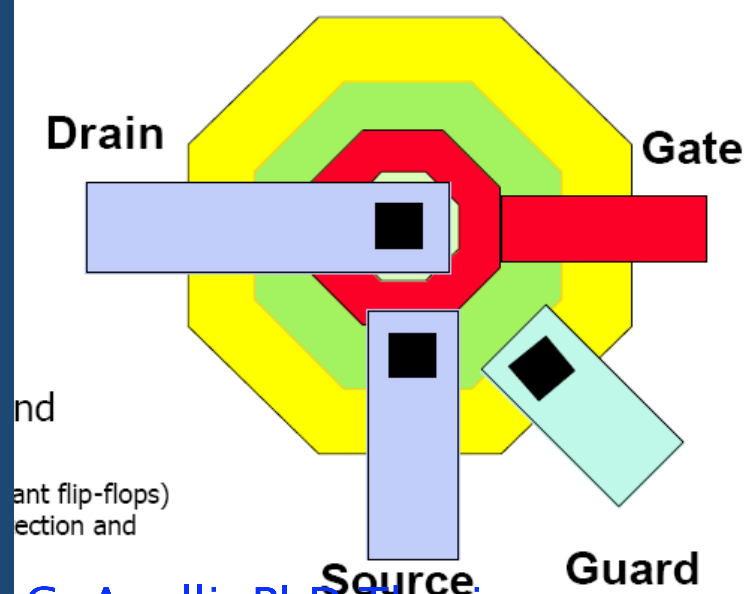
# Radiation Tolerant Design

- Thin oxides reduce overall radiation sensitivity of deep submicron CMOS These transistors are surrounded by thicker "field oxide", which can still trap charge
- This trapped charge can form a channel for leakage currents from source to drain
- Enclosed layout transistors eliminate this effect by using a geometry that does not provide a drain-source path path near field oxide

This is radiation hard by design



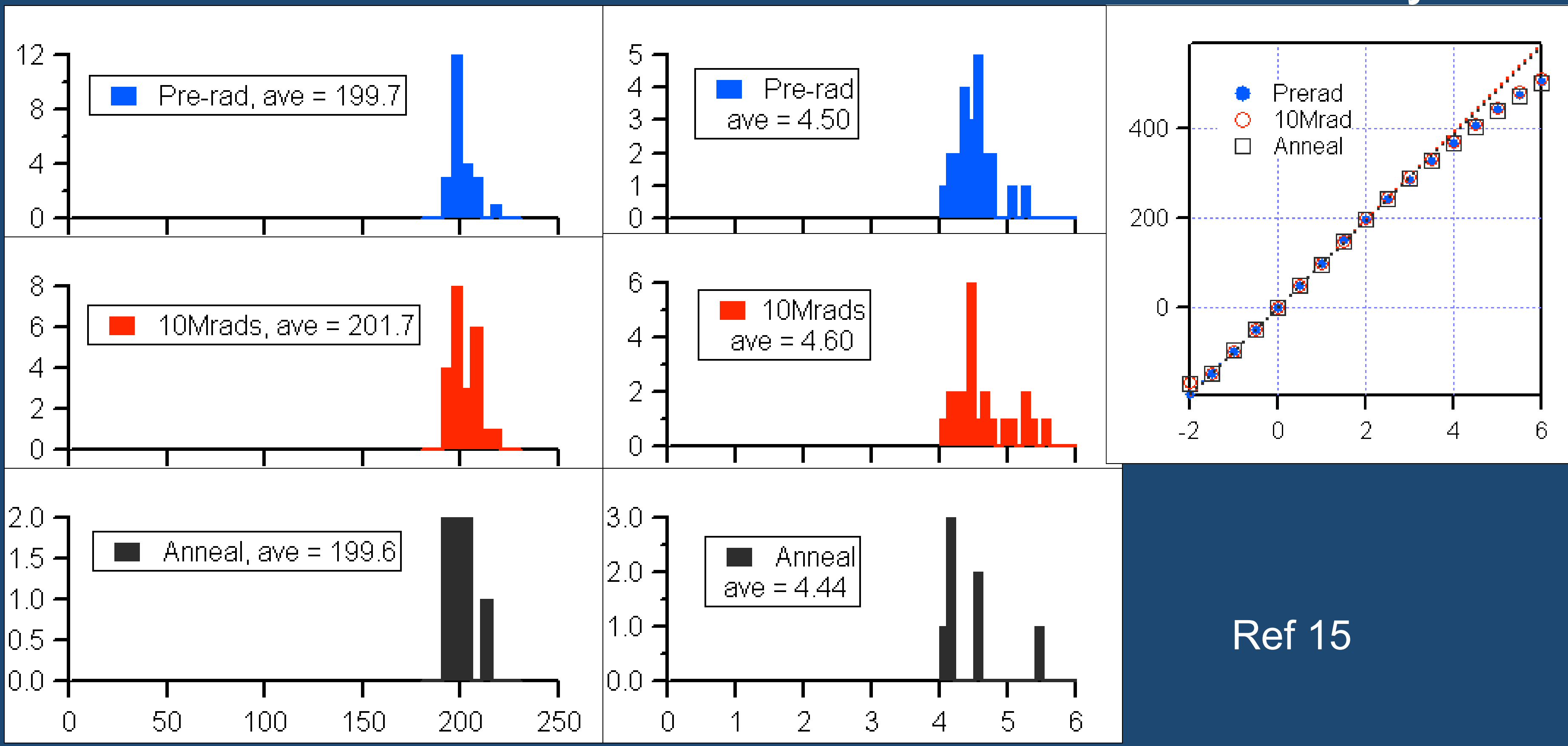

After T.R.Oldham et al., IEEE Trans.Nucl.Sci., Vol. NS-34 (1987) 1184




G. Anelli; PhD Thesis

# APV25 0.25μm CMS Rad

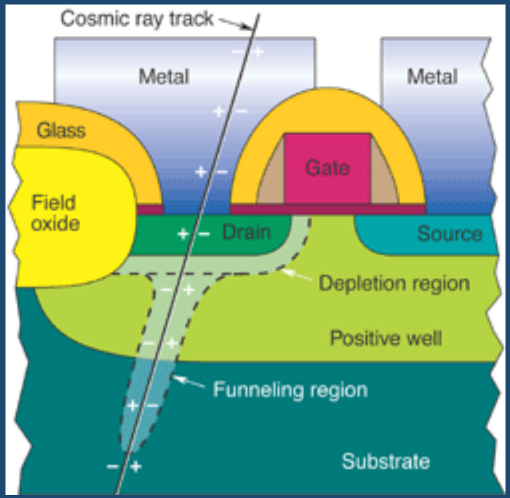
Gain | noise | Linearity




rms ADC units

Ref 15

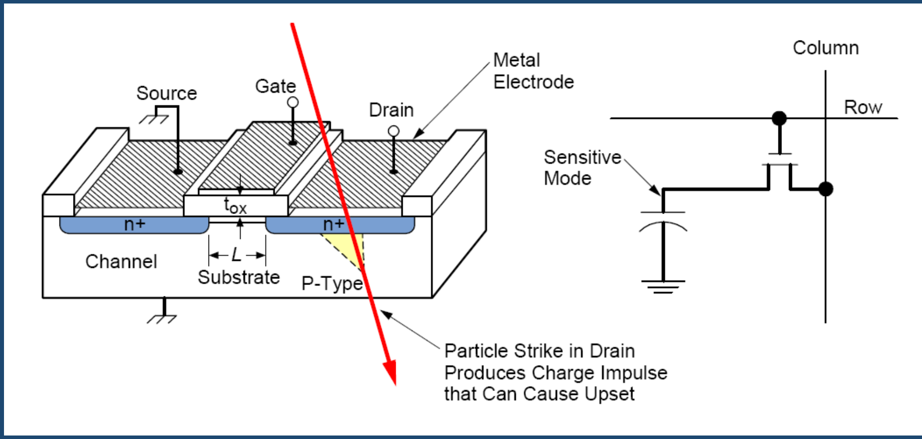
# Single event Effects

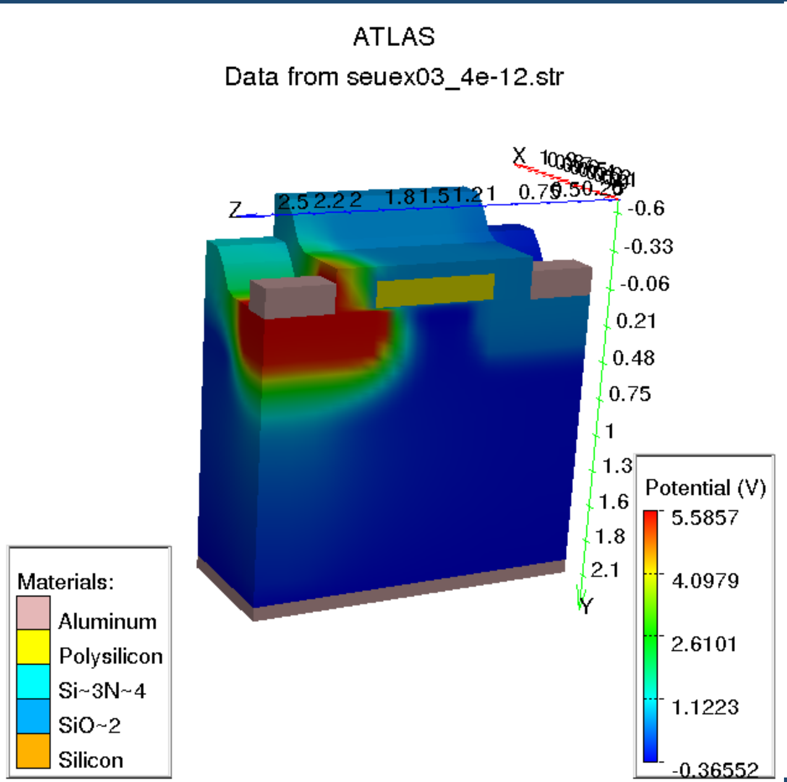


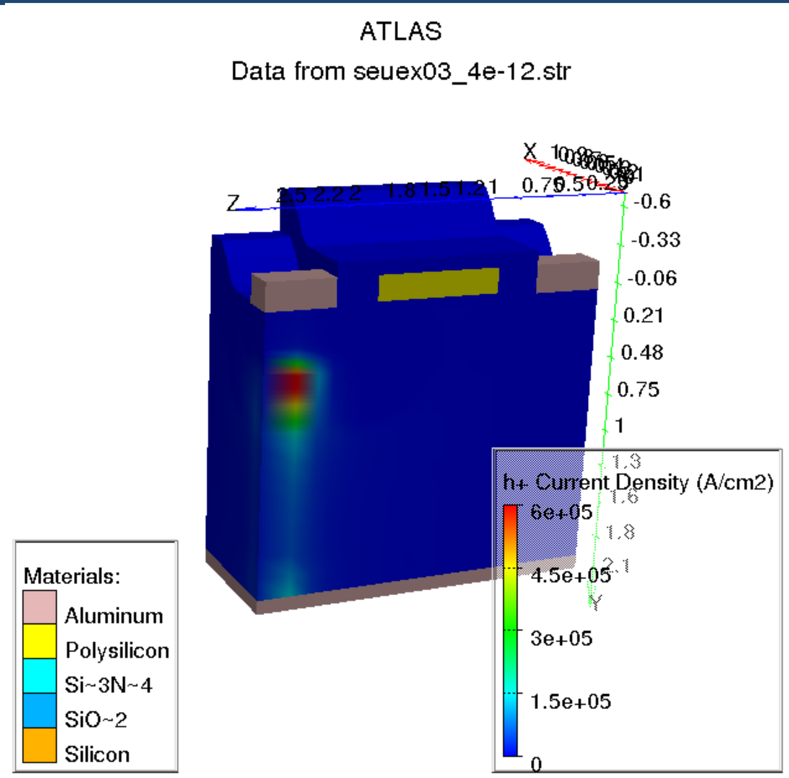

- Linear Energy Transfer (LET):
  dE/Dx of ionizing radiation. LET is typically expressed in units of MeV·cm²/mg of material.
- Single event upset (SEU):
  Change of state of a transistor due to radiation. Reversible.
- Single event latchup (SEL):
  Latched change of state of a circuit due to radiation. May need to power cycle to reset
- Single event burnout (SEB):
  Destruction of a circuit element due to radiation.

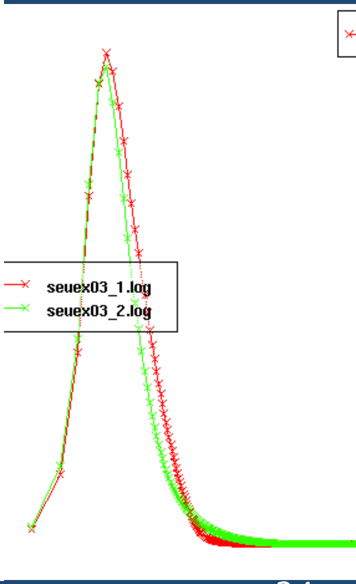
# Single Event Upset

3D Simulation of a single event in a CMOS transistor using Silvaco



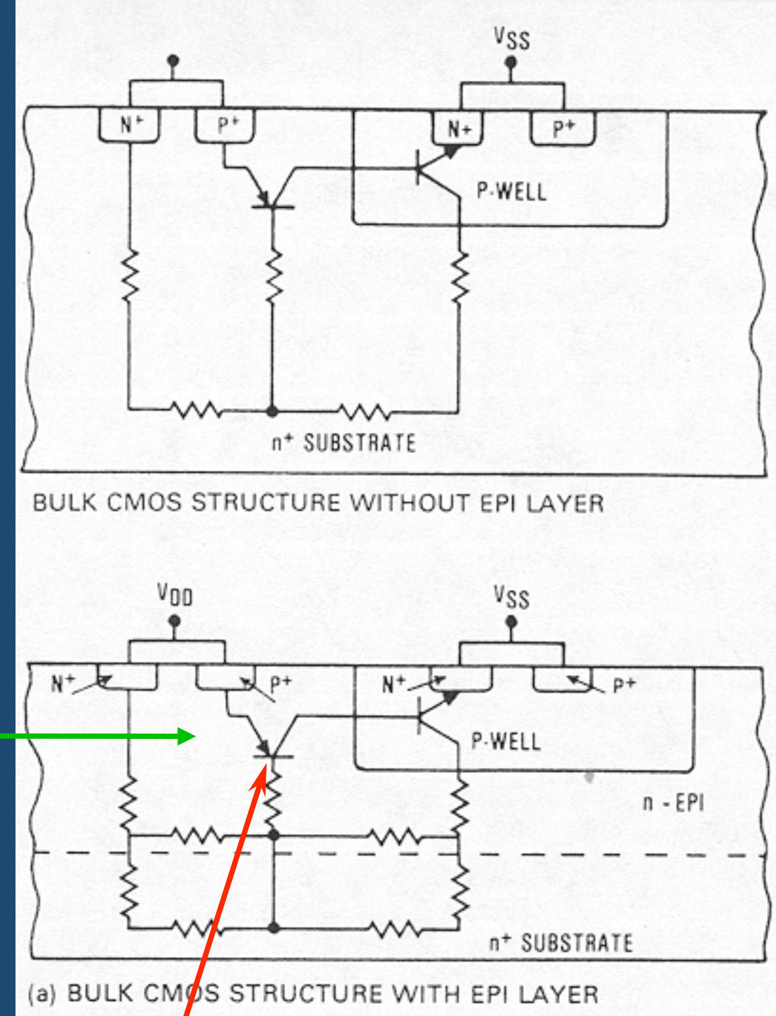



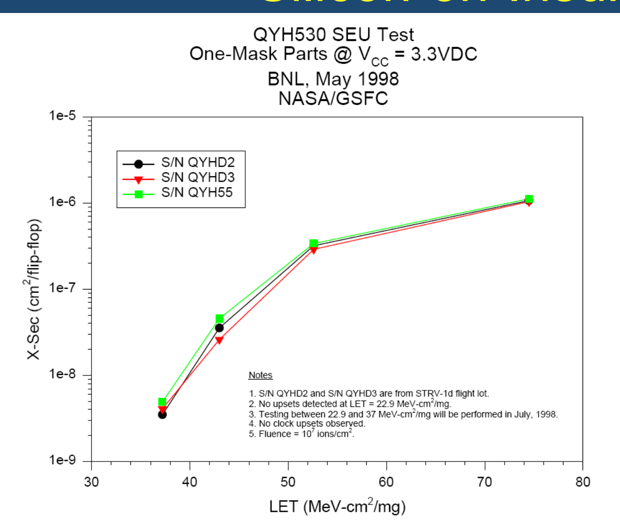
# Single Event Latchup

- Bulk CMOS contains parasitic bipolar transistors interconnected by the bulk CMOS substrate – forms a parasitic thyristor.
- Can cause burnup if not current limited
- Mitigated by:
  - Thin, high resistivity epitaxial layers
  - Trench isolation
  - Silicon-on-Insulator (SOI)




Harris Semiconductor

Negative charge pulse lowers gate potential



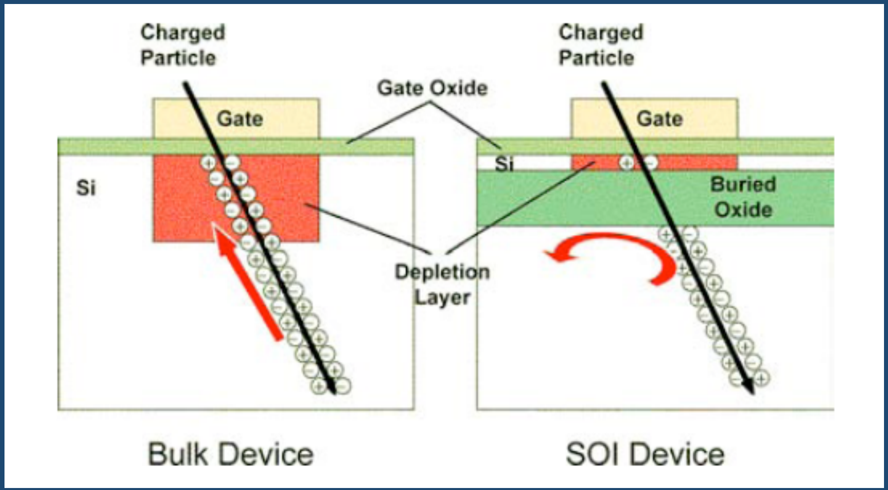

NASA test of gate array

# Single Event Burnup

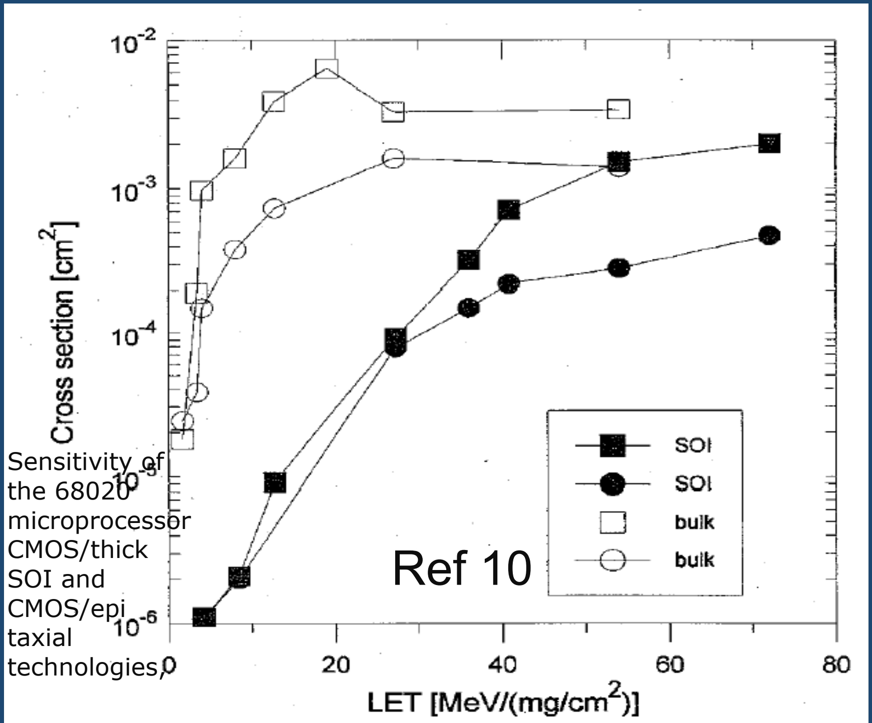
- Usually in power MOS and BJT
- Transistor is off
  - High potential across reverse bias junction
  - Highly ionizing event deposits charge in the high field region
  - Avalanche multiplication in the silicon causes high currents which are amplified in the transistor
  - Junction breaks down
- NMOS more sensitive than PMOS because of larger avalanche multiplication for electrons

# Silicon On Insulator

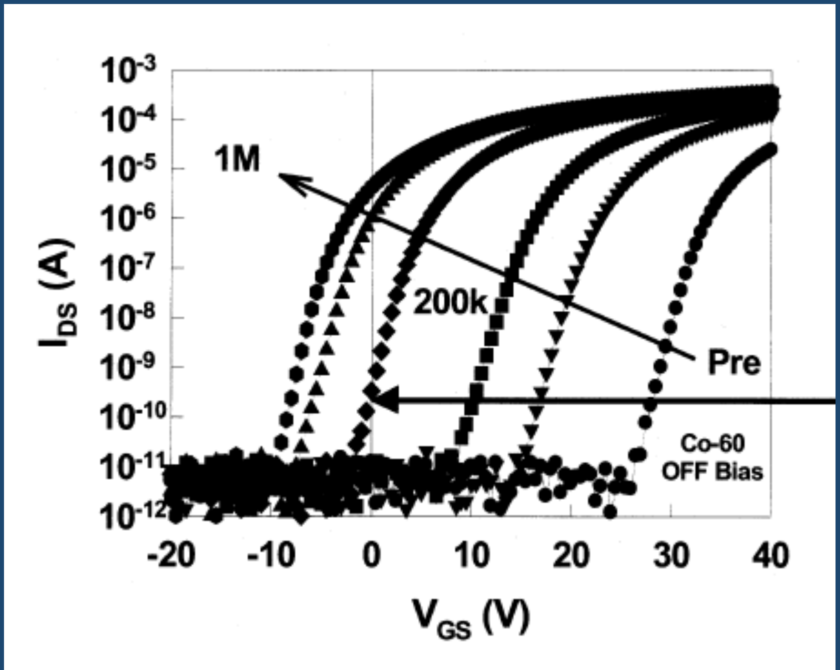
- SOI structures provide smaller region for charge collection – lower SEU cross sections




- But the “buried” oxide layer is sensitive to charge-up similar to CMOS gate oxides – sensitive to TID
- Led to additional dual gated structures

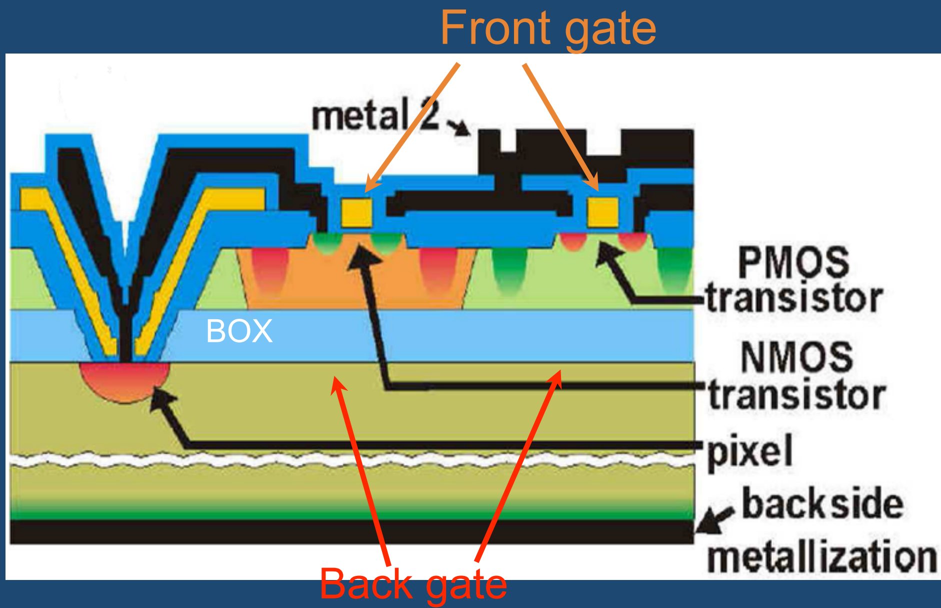


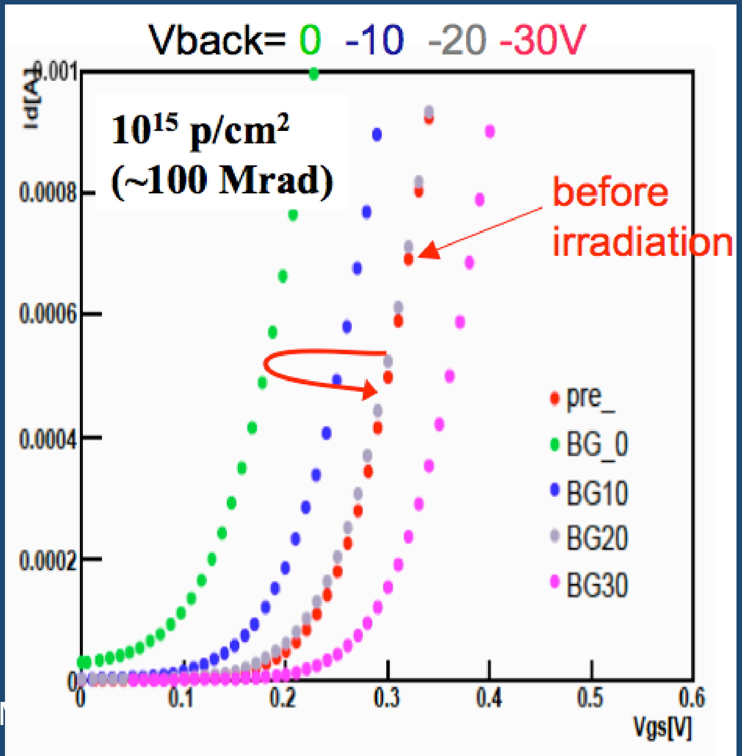

Sensitivity of the 68020 microprocessor CMOS/thick SOI and CMOS/epitaxial technologies

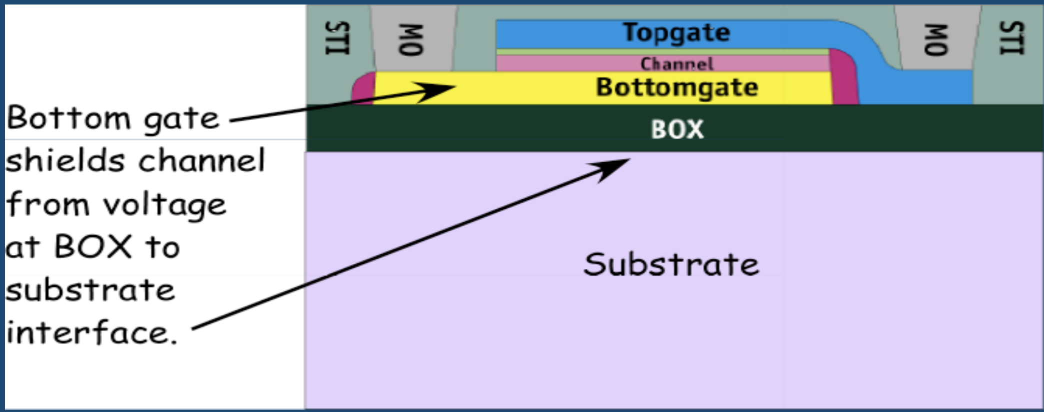


# Silicon On Insulator Structures

- Back "handle wafer" can be biased to counteract radiation-induced shifts
- Multiple gate structure to shield transistor channel
- Handle wafer can also be used as a detector



# Commercial Parts

- Deep submicron CMOS ASICs have become more TID hard as feature size shrinks
  - Not true for SEE
  - Diversity of process variations makes general statements difficult
- Parts (ASICs, FPGAs …) are reasonably easy to test for SEE and TID in cyclotrons and with sources
- Packaged system tests are more difficult to evaluate, especially if the problem is buried in a subsystem.
- There are extensive databases for “space qualified” parts
- But the space environment has a different character than accelerators (more ionizing radiation, fewer neutrons and pions)
- CERN testing program for LHC components (Ref 16)

# NASA Model (ref 14)

Assign lead radiation effects engineer for each project

- Define the hazard
  - Radiation environment
- Evaluate the hazard
  - Estimate effects of TID, displacement damage and SEE
- Define requirements
  - TID safety factor of 2
  - Vary requirement by system performance need
  - Fluences for worst case, nominal, and peak
- Evaluate device usage
  - Screen parts list wrt database
    - Has process changed?
    - Lot date different?
    - Testing environment?
  - Evaluate SEE rates
  - Understand degradation of performance with TID

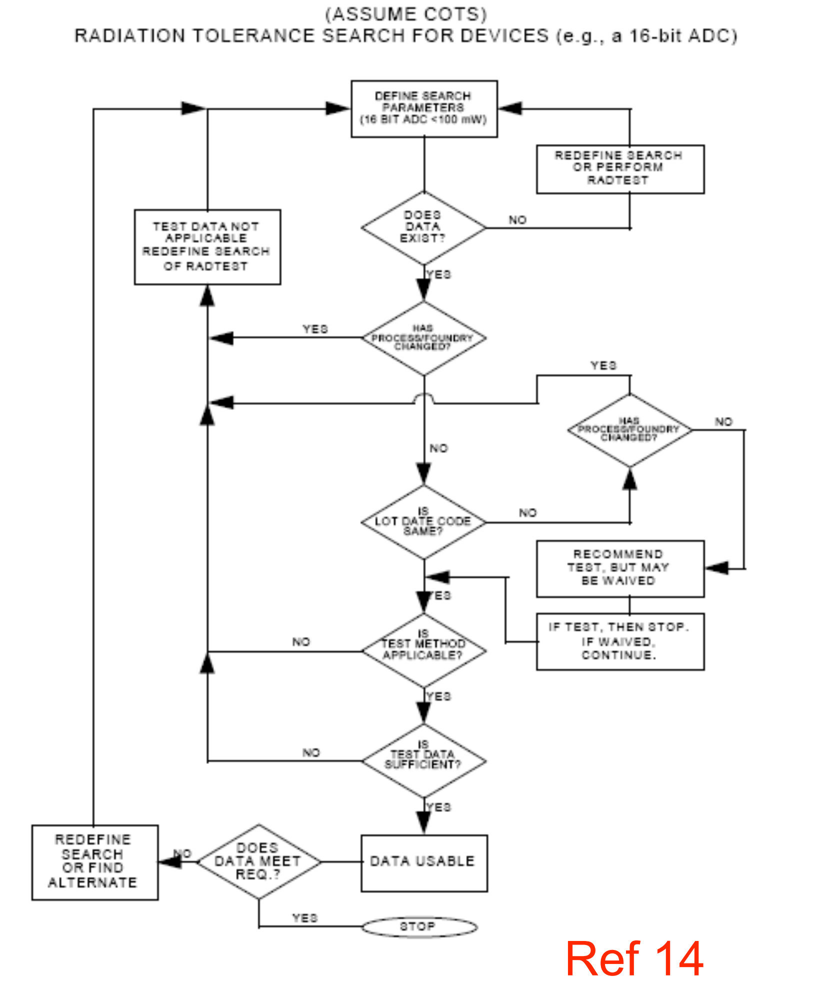



Figure 6: Basic method for data search and definition of part usability. The example is for a 16-bit ADC.

# Conclusions

- Radiation damage is complex and multidimensional
  - Detector effects reasonably well understood
    - Mitigation techniques allow for ~5-10 Mrad exposures
  - Basic causes and effects in electronics have been carefully studied but modern electronics are a moving target
    - Rapid advance of technology
    - Introduction of mixed technology devices
    - Changing feature size
- Test as extensively as possible

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