

ALS FPGA-BASED TRANSVERSE FEEDBACK ELECTRONICS*

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Abstract

The Advanced Light Source Transverse Feedback System currently consists of a refrigerator sized analog delay line system. The new system is the 2nd generation Transverse Feedback System, derived from work done for PEP-II in 2004 [1]. It uses the latest generation Virtex-5 FPGA, and has 12-bit ADCs and DACs for bunch-bunch feedback at 500MHz. In addition, this system provides networked capability for setup and diagnostics.

INTRODUCTION

At the ALS, coupled bunch instabilities are driven by the RF cavity dipole higher order modes (HOMs) and the resistive wall impedance of the vacuum chamber [2]. The existing ALS Transverse Feedback (TFB) System adequately damps these beam oscillations, but does not provide any diagnostic information or remote control capability. Recent experiences using an ADC-FPGA-DAC architecture for bunch-by-bunch feedback systems have proven largely successful. These digital systems provide extensive diagnostic capability with deep memory capable of storing hundreds of turns of bunch data. Set points and diagnostic data can be transferred to and from the system via the control system network.

The existing TFB electronics consist of two microwave receivers for detecting horizontal and vertical moment, a system (shown as two variable attenuators) for mixing the signals from the two pickup stations, a delay, and a power amplifier for driving the kicker [2]. The electronics upgrade replaces the delay element (currently a long cable) with an FPGA-based digital system. Figure 1 shows the diagram of the upgraded electronics.

The new digital system will be based on the model of the PEP-II TFB upgrade [1]. Using the latest technology, the system is capable of feedback at the full ALS bunch rate of 500MHz. Data converters with 12-bit resolution clocked at 500MHz (effective) sample the pickups and drive the kicker outputs for bunch-by-bunch feedback. The Xilinx® Virtex™-5 LX50 FPGA provides filter, delay, data capture, and control system interface functions. This paper describes the design details of the new ALS TFB electronics.

HARDWARE

The new TFB system electronics consist of a two board set: a commercial FPGA evaluation board connected via a high-speed connector interface to a custom in-house designed board containing the high-speed analog interfaces. The block diagram for the TFB hardware is shown in Figure 2.

* This work was supported by the U.S. Department of Energy, under Contract No. DE-AC03-76SF00098

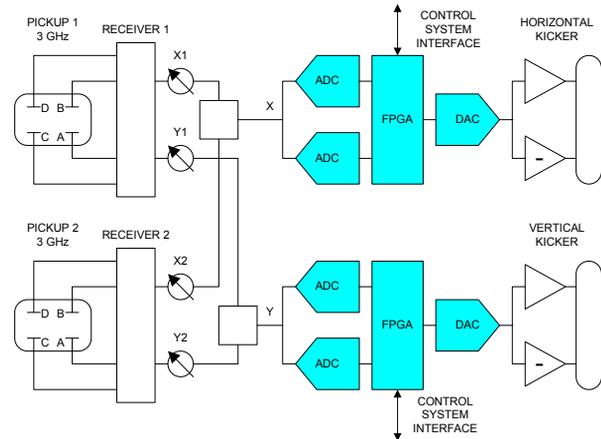


Figure 1: ALS Transverse Feedback Electronics.

The demo board chosen for this design is the Xilinx® Virtex™-5 LX Evaluation Kit from Avnet. This board contains many of the desired system components including a V5LX50 FPGA, EXP high-speed expansion connectors, 64MB DDR2 SDRAM, 16MB Flash Memory, and Ethernet PHY [3]. The FPGA contains sufficient programmable logic resources for the desired functionality and runs comfortably at the required clock speed of 250MHz. The EXP expansion connectors are controlled impedance Samtec QSE/QTE series connectors specified to run up to 750MHz for differential signals [4]. These connectors provide sufficient I/O to connect the FPGA to the high speed 12-bit data converters and other interfaces on the custom EXP daughter card. The SDRAM contains the software code to run the control system interface and the memory used for data capture diagnostics. The Flash Memory provides flexible boot options for the control system software. The Ethernet interface allows connectivity with the ALS Control System network.

The custom board is an EXP expansion daughter board that contains the high-speed data converters, clock distribution and programmable delay, and a moderate performance two-channel 16-bit DAC to set the kicker amplifier gains. Two 12-bit LTC2242-12 ADCs, sampling at $f_{RF}/2 = 250\text{Mps}$ 180 degrees out of phase, sample the pickup signals on every bunch. The pickup data is transferred to the FPGA, clocked at 250MHz, which calculates the correction value to apply to the kickers on the two separate data paths. The correction data is fed through the FPGA DDR output buffers to the DAC at 500 MHz. The 12-bit MAX5886 DAC provides correction output to the kickers at 500Mps. This custom board receives the 500MHz bunch rate clock from the ALS timing system and divides and distributes it to the FPGA, DAC, and ADCs. Two MC100EP195 programmable clock delay chips can be used to fine tune the DAC and ADC clocks in 10ps increments over a 10ns range.

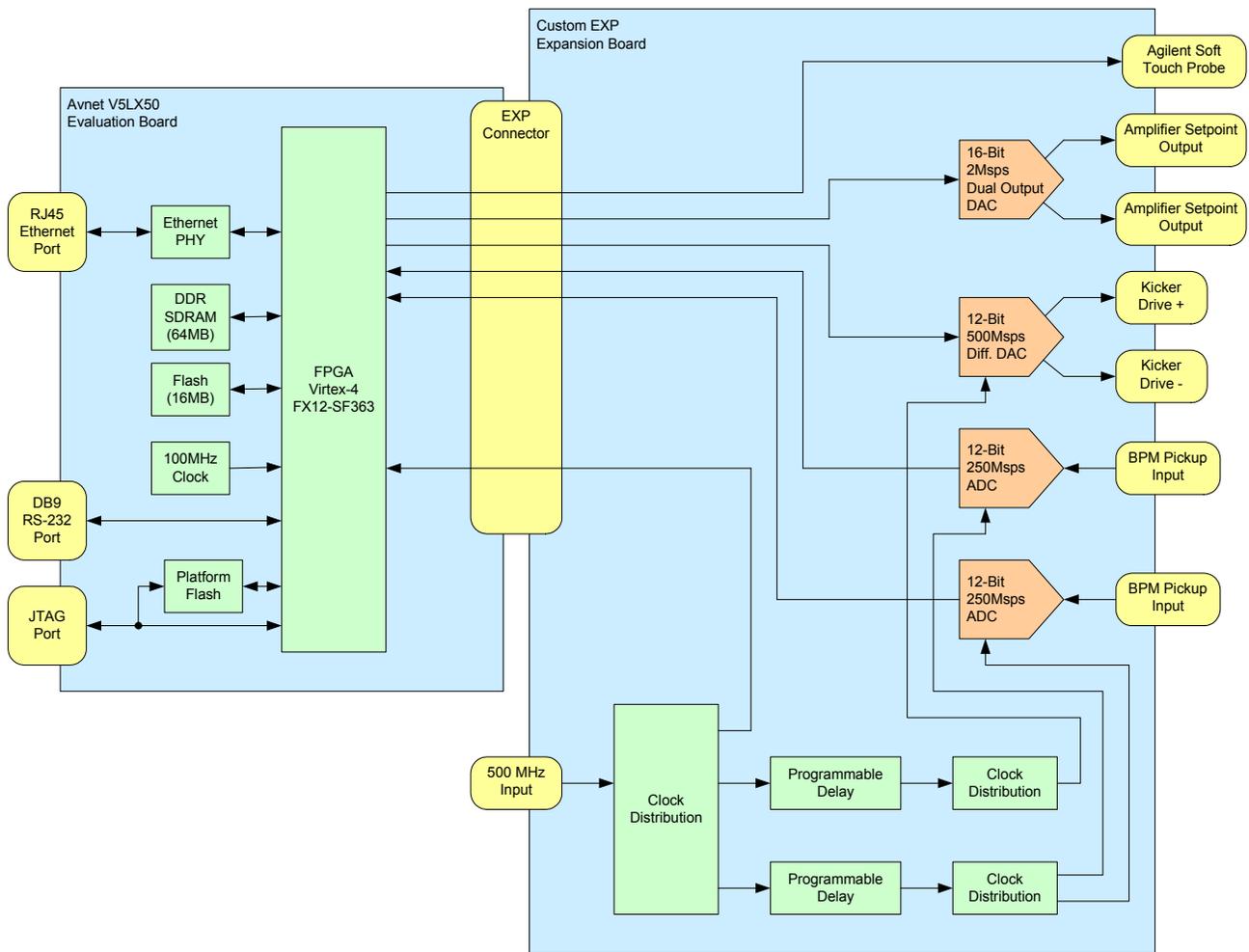


Figure 2: ALS Transverse Feedback Hardware Block Diagram.

FIRMWARE

The FPGA firmware consists of an embedded processor, standard peripheral interfaces, and custom cores for EXP board interfaces and feedback logic. A block diagram of the TFB firmware is shown in Figure 3. The PEP-II TFB design contained Virtex-2Pro series FPGAs with embedded PowerPC hard core processors running the control system interface software [2]. Since the Virtex-5 LX series FPGA on this board does not have an embedded PowerPC, the MicroBlaze soft core processor will be used. The processor runs the control system interface software, which initially will be a simple TCP interpreter based on an Avnet design example. Eventually, this interface could be replaced with an EPICS channel access server running on a version of the Linux operating system (OS). More details regarding the use of embedded processors in FPGA-based systems can be found elsewhere [5].

Several peripheral interface cores included in the development kit design templates are used in this design including an Ethernet controller (EMAC), Flash Memory controller, UART, Agilent Soft Touch Probe interface, Block RAM Controller, and SDRAM Multi-Port Memory

Controller (MPMC2). These cores are developed by Xilinx and are pre-configured for the development kit hardware. The EMAC is used by the system software to communicate with the control system network. The Flash

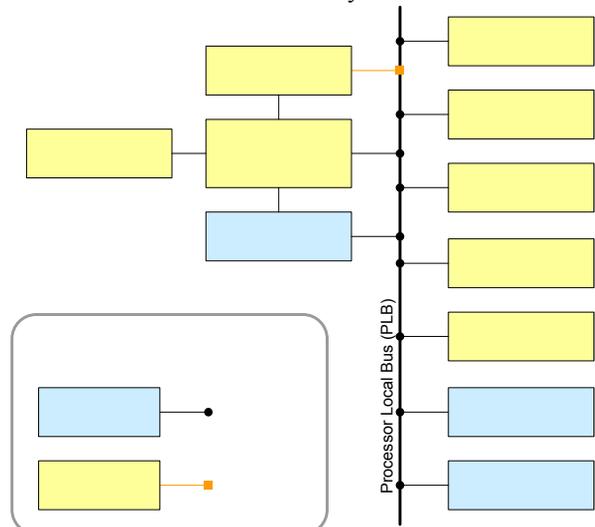


Figure 3: ALS Transverse Feedback Firmware Block Diagram.

Feedback and instabilities

can be used to store the OS or an OS bootloader application depending on the size. The UART and Soft Touch Probe can be used for status and debugging.

The Block RAM contains initial boot code for the processor. This code typically boots the OS or OS bootloader from the Flash. The MPMC2 allows simultaneous access to the SDRAM from multiple sources. The SDRAM stores all OS and program code that is accessed by the processor. It also stores bunch data written by the feedback core for diagnostic purposes.

The firmware also contains several custom cores. The feedback core provides access to the high-speed ADCs and DACs and implements the filter and delay logic for feedback. This core can write the ADC data to the SDRAM through a dedicated port in the MPMC2 core. Another core provides an interface to the lower performance DAC that controls the kicker amplifier gains. A third custom core controls the programmable delay chips to tune the ADC and DAC clock edges.

FUTURE CONSIDERATIONS

There are several aspects of bunch-by-bunch feedback systems that can be improved over the capabilities of the current generation of systems. One obvious limitation is the sampling speed of the ADCs. 12-bit 250Msps ADCs are near the edge of current performance limitations, but it is likely that there will be a 12-bit 500Msps part suitable for use in feedback systems in the next few years. While there is always a push for higher resolution parts, there is no proof of any performance advantage of 12-bit over 8-bit bunch-by-bunch feedback systems. We plan to run a side-by-side comparison of these systems to see if there is any performance advantage at the ALS.

Similarly, current FPGAs are incapable of single channel processing at 500MHz. The fastest FPGA speed grades boast routing designs running up to 550MHz, but with minimal design complexity the maximum routed performance decreases dramatically. With our new system using a Virtex-5 at the slowest speed grade, we are able to comfortably route complex designs at 250MHz. At the present rate of development, the performance of these devices will allow routing complex designs at 500MHz in the next few years as well.

With both ADCs and FPGAs running at 500MHz, systems will be capable of single channel feedback through the entire digital system. This is important because there are limitations to the current multi-channel sampling and processing designs. First, these designs cannot provide full resolution for particle accelerators with odd harmonic numbers due to errors in matching the multiple channels. With an odd harmonic number and a two channel sampling system like presented here, each bunch is sampled by the opposite ADC on each consecutive turn. Therefore gain and offset differences between the channels and clock jitter and mismatch can all affect the resolution of the sampled bunch data. This is

not an issue for accelerators like the ALS with even harmonic numbers because each bunch is sampled by the same ADC on every turn (i.e. ADC0 samples even bunches and ADC1 samples odd bunches). However, for absolute bunch amplitude measurements, it is an issue for even harmonic number accelerators as well.

Improvements can also be made in the logic design of existing systems. One feature that we may add to the ALS system is the ability to provide a separate gain for each bunch. A table of gain values would be loaded into FPGA memory with a value for each bunch. This could be used for kick out or grow-damp studies of individual or arbitrary patterns of bunches.

An extension of this concept is to add bunch cleaning capability to the feedback system. The new ALS FPGA-based bunch cleaning hardware uses the same FPGA-DAC architecture as the ALS TFB system [6]. The bunch cleaning is currently connected to a spare set of kickers. Using the TFB electronics to run both the feedback and bunch cleaning algorithms by combining the logic into a single FPGA would require only a single electronic system and only one kicker.

CONCLUSION

Design of FPGA-based feedback electronics is not a new concept, but using only two 12-bit data converters to generate bunch-by-bunch feedback at 500MHz has not previously been achieved. This provides tremendous improvement over the existing analog system used at the ALS. Storage of bunch-by-bunch 12-bit data allows for advanced diagnostics and post-mortem analysis. The embedded Microblaze processor provides control system network accessibility to set points and diagnostic data. The electronics have been built and are being qualified with the plan to commission the system by the end of this calendar year.

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