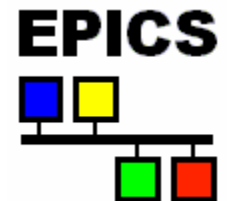


Overview of the NSLS-II Control System

Nikolay Malitsky

*on behalf of
NSLS-II Control Group*



Acknowledgments

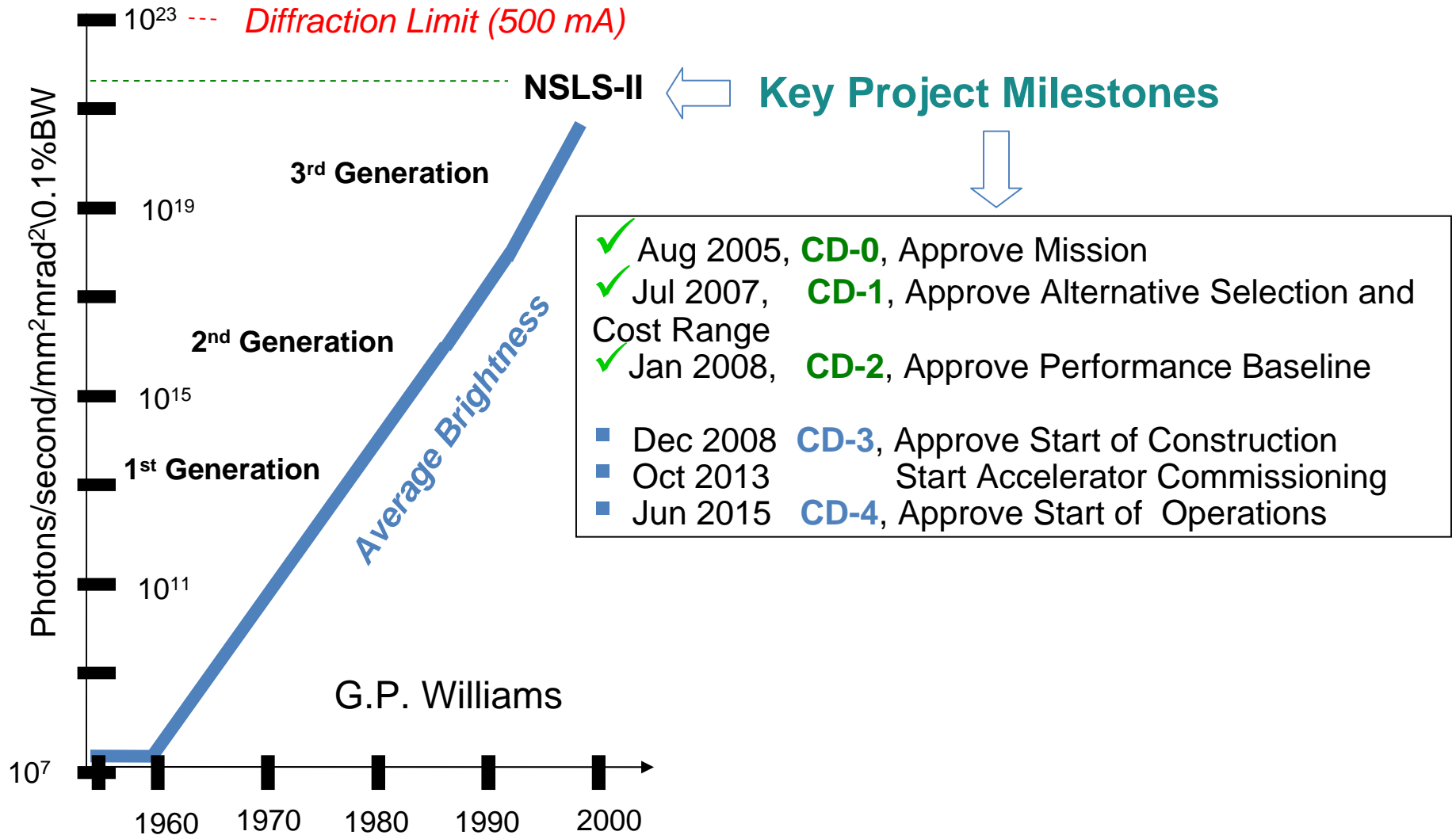
Control: B. Dalesio, G. Carcassi, D. Dohan, J. Shah, G. Shen, Y. Tian, Z. Yin

AP: J. Bengtsson, T. Shaftan

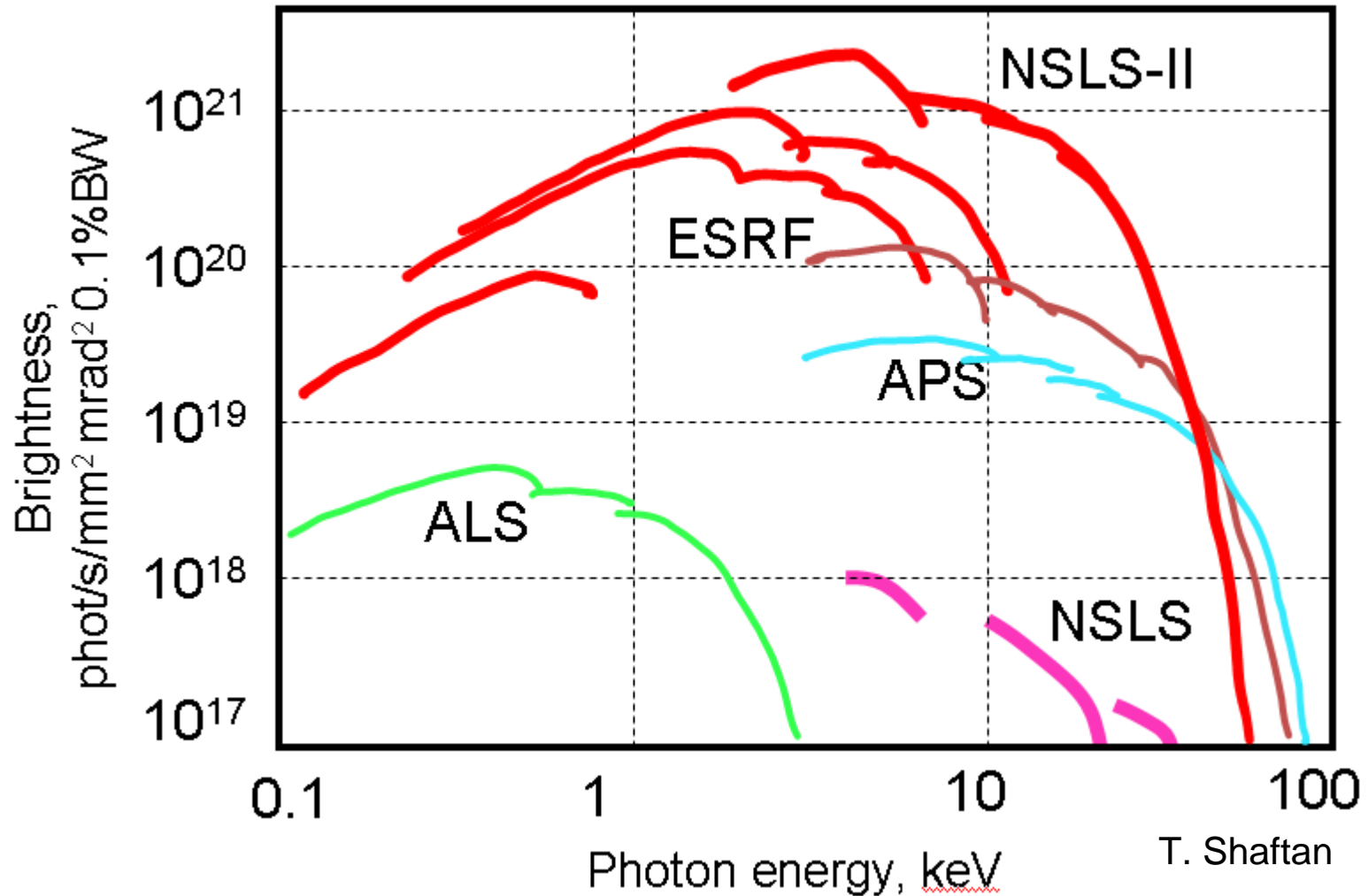
Outline

- **Overview of the NSLS-II Project**
- **Control System**
 - Scope
 - Requirements
 - Standards
 - Infrastructure
- **Areas For Technical Development**
 - Embedded Device Control
 - IRMIS: Integrated Relational Model of Installed Systems
 - High Level Applications
- **Concluding Remarks**

Evolution of average brightness



NSLS-II vs Synchrotron Light Sources



NSLS-II Design Features

Design Parameters

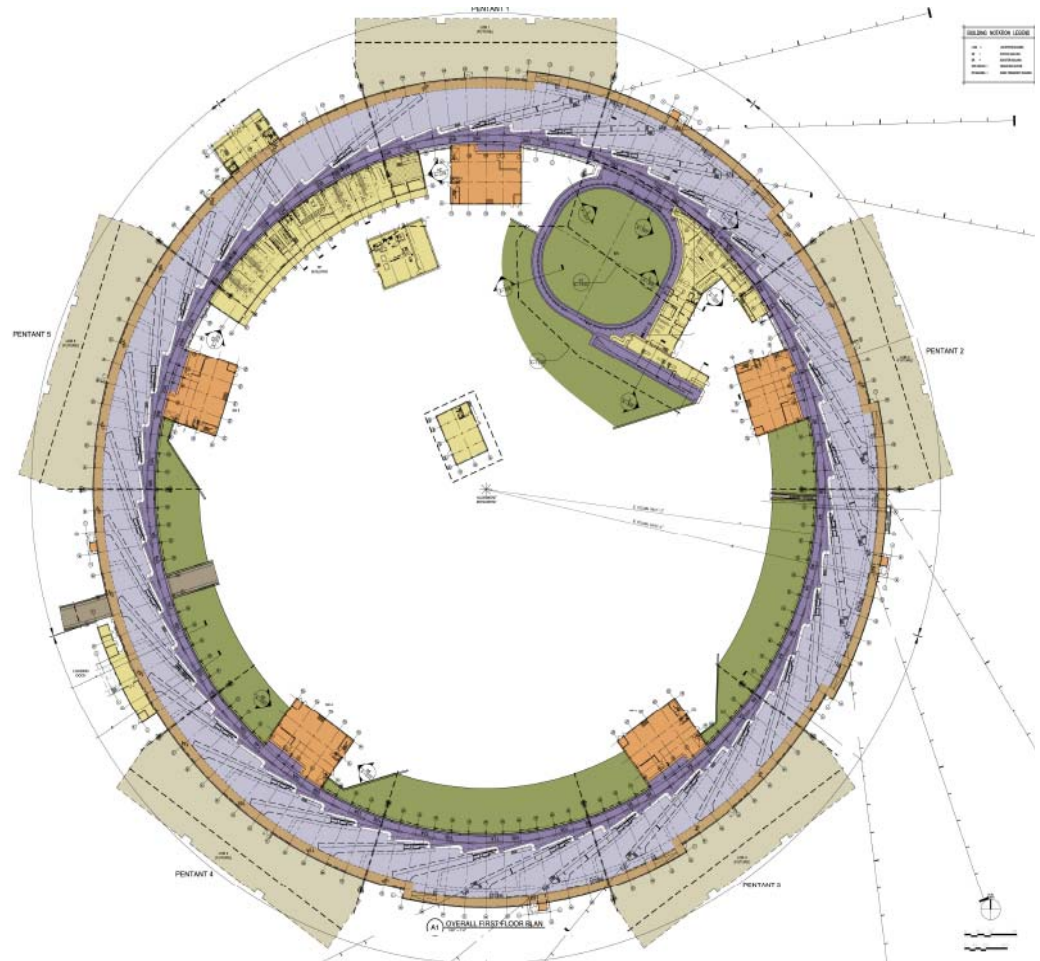
- 3 GeV, 500 mA, top-off injection
- Circumference 791.5 m
- 30 cell, Double Bend Achromat
 - 15 high- β straights (9.3 m)
 - 15 low- β straights (6.6 m)

Novel design features:

- Damping wigglers
- Soft bend magnets
- Three pole wigglers
- Large gap IR dipoles
- Elliptically polarizing undulators

Ultra-low emittance

- $\epsilon_x, \epsilon_y = 0.6, 0.008$ nm-rad
- Diffraction limited in vertical at 12 keV
- Small beam size: $\sigma_y = 2.6$ μm , $\sigma_x = 28$ μm , $\sigma'_y = 3.2$ μrad , $\sigma'_x = 19$ μrad

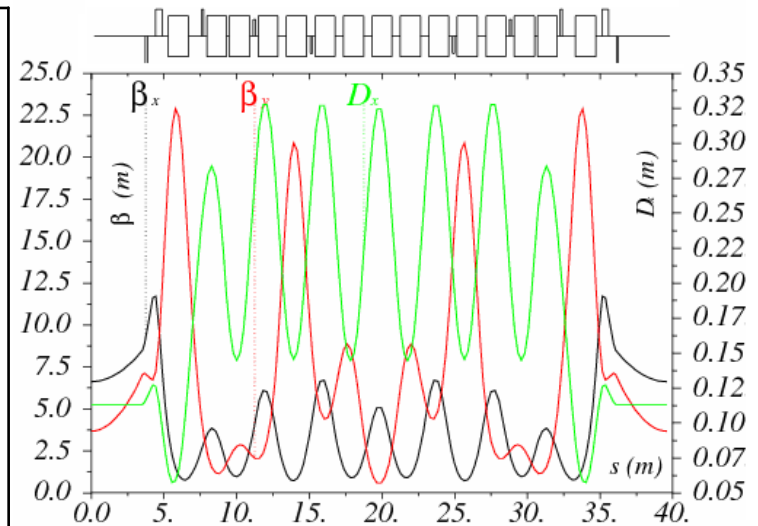


S. Dierker, F. Willeke

Injection Systems

Booster:

Injection Energy	0.2 GeV
Extraction Energy	3.0 GeV
Circumference	154 m
Emittance	30 nm-rad
Cycle Frequency	1Hz
RF frequency	500 MHz
Charge	10-15nC @ 30 mA
Tunes: x, y	10.25, 4.2



Designed after ASP Booster

T.Shaftan, W.Guo, Y.Li, B.Nash

Close to NSLS-II requirements:

Linac:

Energy	0.2 GeV
Frequency	S-Band
Charge	15 nC/pulse
$\Delta E/E$	< 1%

ASP (ACCEL):

3 GHz, 100 MeV, 4/0.25 nC/pulse

■ SOLEIL (THALES):

3 GHz, 100 MeV, 10/0.5 nC/pulse

Scope of the Control System

The control system integrates all subsystems:

- Power supply
- RF
- Timing
- Vacuum
- Diagnostics
- Insertion devices
- Beam lines
- Facility
- Equipment protection and personal safety

Control System Requirements – 1 of 2

- Bunch Length 1-40 psecs
- 2.6 usec ring revolution
- Top off every 1 minute
- Top off bunch train 140-300 nsec
- Top off damping time 10-50 msecs (no extraction)

- Manual control of orbit trims, quadrupoles, sextupoles, and insertion devices are asynchronous
- ~10 Hz write/read is suitable for “turning knobs” for a power supply
- 5 Hz updates to operators of up to 1000 chosen parameters
- Archive up to 6000 parameters at a rate of 2 Hz continually

- Must scale to support 150,000 physical I/O connections and 400,000 computed variables
- 99.99% availability 24/7

Control System Requirements – 2 of 2

- Transient Recording
 - Take coherent turn by turn orbit data for up to 800 channels
1024 turns
 - Latch the last 10 seconds of data from all parameters in the storage ring
 - Beam line needs 1 msec archiving over 1 minute for temperatures and positions
- Provide data for all control aspects
- 5 KHz RF Feedback on beam phase
- 10 kHz orbit feedback, (100 usec loop time)
 - 300 BPMs (10 per cell)
 - 2 * 120 Corrector PS in 30 I/O Controllers (IOC)
- 20 msec equipment protection mitigation
- 1 Hz model based control
- 10 kHz power supply read backs triggered from timing system

Open-Source Control System Standards

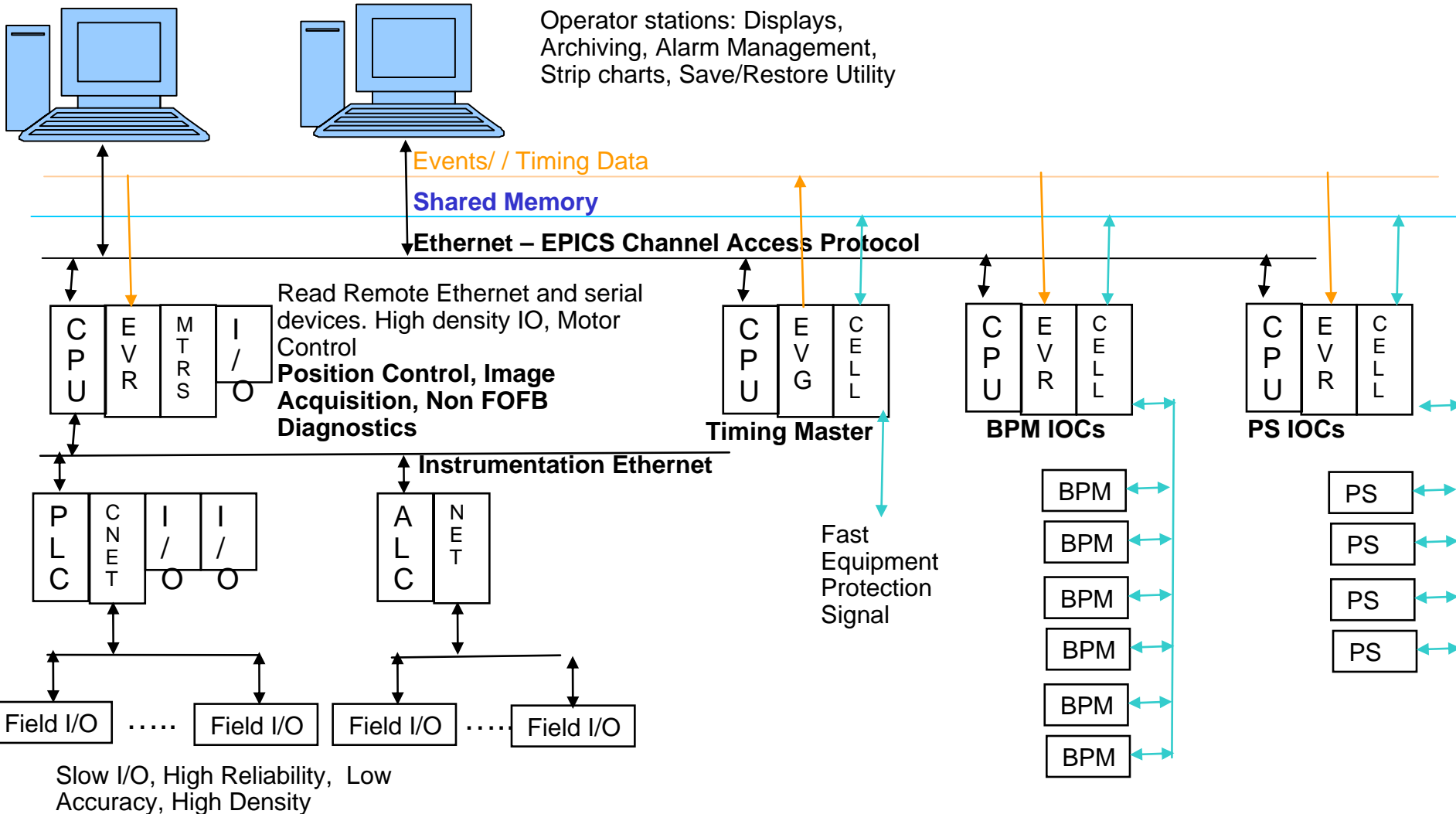
EPICS (Experimental Physics and Industrial Control System) Collaboration:

- Began in 1989 between LANL/GTA & ANL/APS (B. Dalesio & M. Kraimer)
- Over 100 independent projects in North America, Europe and Asia
- Applications in particle physics, astronomy, and industrial control
- Independent development, co-development and incremental development by the numerous distributed groups of developers
- Large biannual collaboration meetings to report new work, discuss future directions, explore new applications, and explore new requirements for existing codes

RTEMS (Real-Time Executive for Multiprocessor Systems) Operating System:

- Free open-source code for OS, support components, tests, documentation, development environment
- Standard compliant
- Highly portable across CPU architectures, many Board Support Packages (BSP) available
- Several successful accelerator control projects: LCLS, Spear, CLS, ...

Control System Infrastructure



Vacuum, PPS, MPS, Non FOFB
PS, Cryo., Facility control

Russian PAC, 28.09 – 03.10, 2008

Areas For Technical Development

- **Embedded Controllers** need an open standard for high speed, deterministic functions. Work with other labs and board manufacturers to develop one.
- **Relational Databases support data management** through the life of a project. Development of adequate tools to enter and report this data is required early.
- **High Level Applications** currently tie together functions through data or file structures. To make the components of High Level Applications modular and distributed, a client/server architecture is needed.

Embedded Device Control – 1 of 2

+T0

+ - Settling time on BPMs

+0.0 usecs - BPM to Compute Controller

$$384 \text{ bits} = 64 \text{ bits} * 6 \text{ BPMs}$$

$$4.9 \text{ usecs} = 384 \text{ bits over } 100 \text{ MBit enet}$$

+4.9 usecs - Compute Controllers to each other

$$10,290 \text{ bits} = 30 \text{ nodes} * 384 \text{ bits}$$

$$10.5 \text{ usecs} = 10,290 \text{ bits over } 2 \text{ GB enet}$$

+15.4 usecs – Compute local matrix

0 usecs

+ 15.4 usecs - Communicate t Power Supply Controllers

$$24 = 4 \text{ PS} * 4 \text{ bytes each}$$

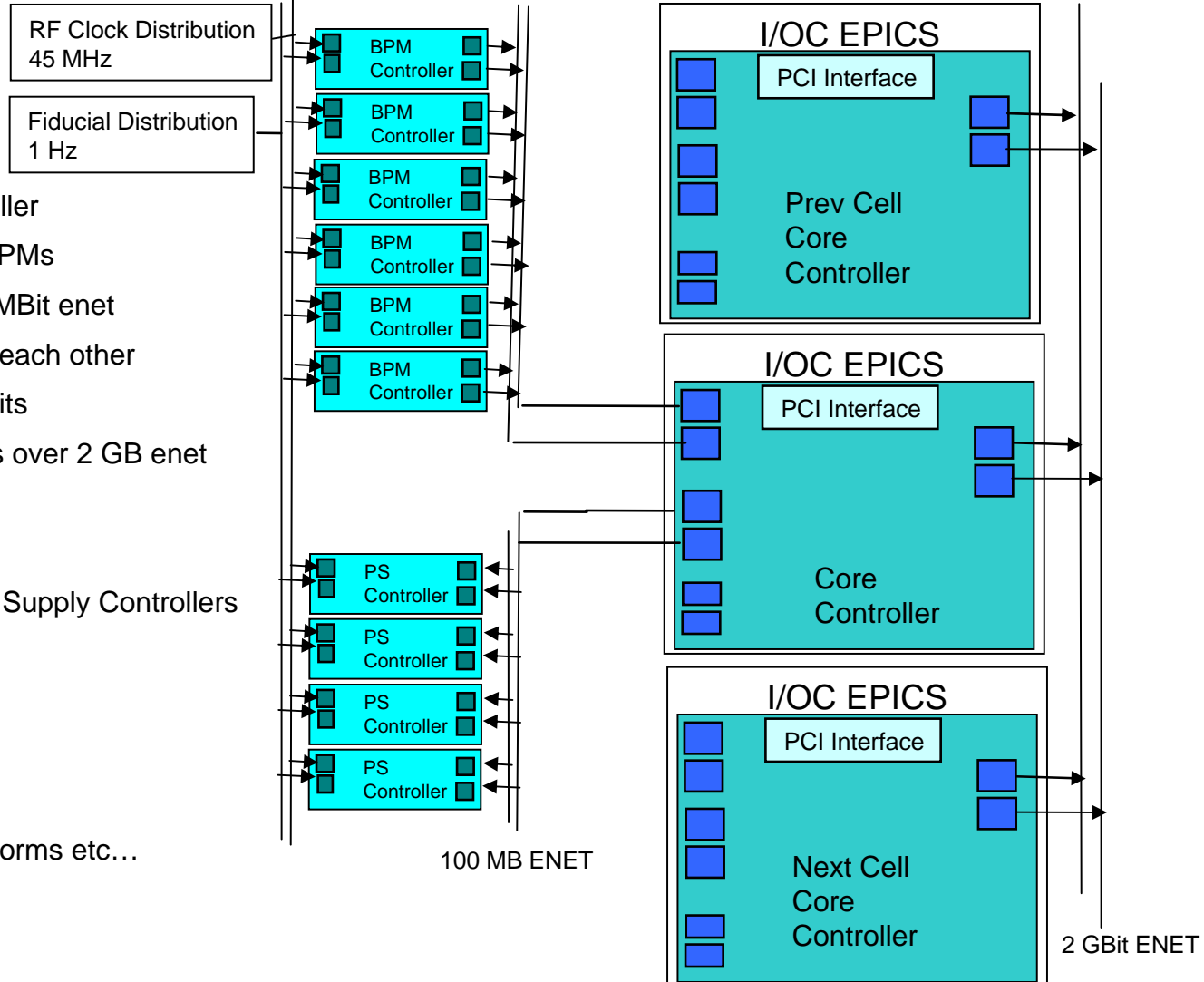
3.5 usecs

+18.9 usecs – loop complete

settling time for magnets

communicate diagnostic waveforms etc...

+200 usecs – start again



Embedded Device Control – 2 of 2

- **FY 08**

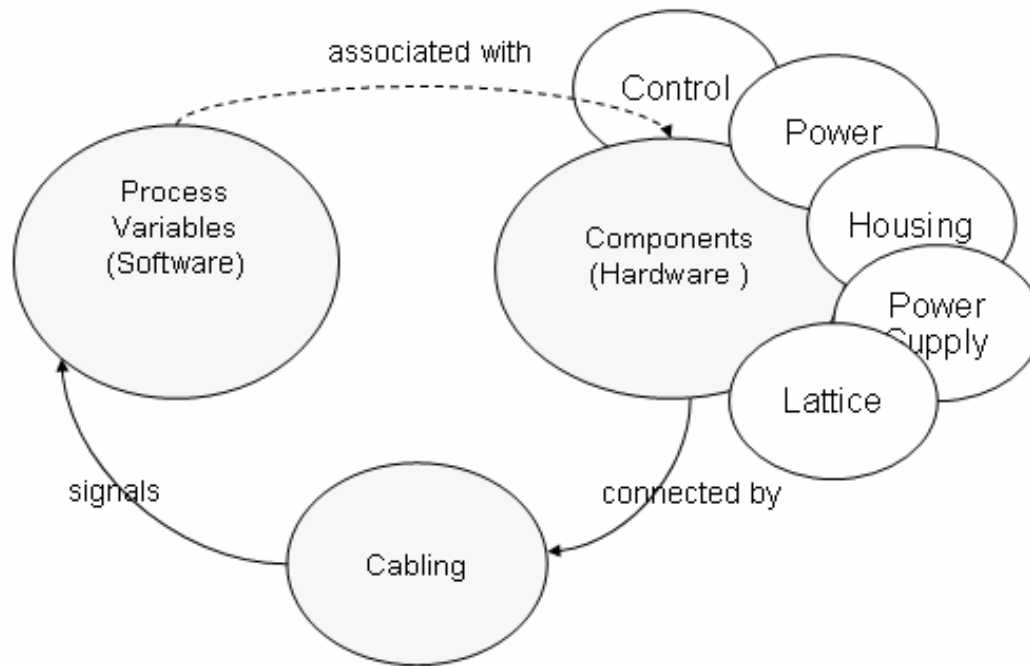
- Purchase order in place with LBL (Alex Ratti and Larry Doolittle)
- Develop a prototype cell controller:
 - Redundant 2 Gbit communication paths for peer to peer communication
 - RF timing signals
 - Verify communication and timing jitter meet requirements
- Develop the interface from the cell controller to a processor for integration into EPICS (PCI Express)

- **FY 09**

- Develop the inexpensive device controller with redundant 100 MBit controllers
- Develop the 100 Mbit receive and transmit circuits for the Cell Controllers
- Begin integration of these device controllers
 - Libera
 - Power supply control
 - LLRF control

IRMIS – 1 of 4

IRMIS: Integrated Relational Model of Installed Systems



IRMIS – 2 of 4

The IRMIS RDB effort began at the APS. After several iterations and meetings with other laboratories, the emphasis shifted to a global perspective in developing the schema and support applications.

IRMIS is a collaborative effort involving SNS, Triumf, SLAC, CLS, SLS, ...

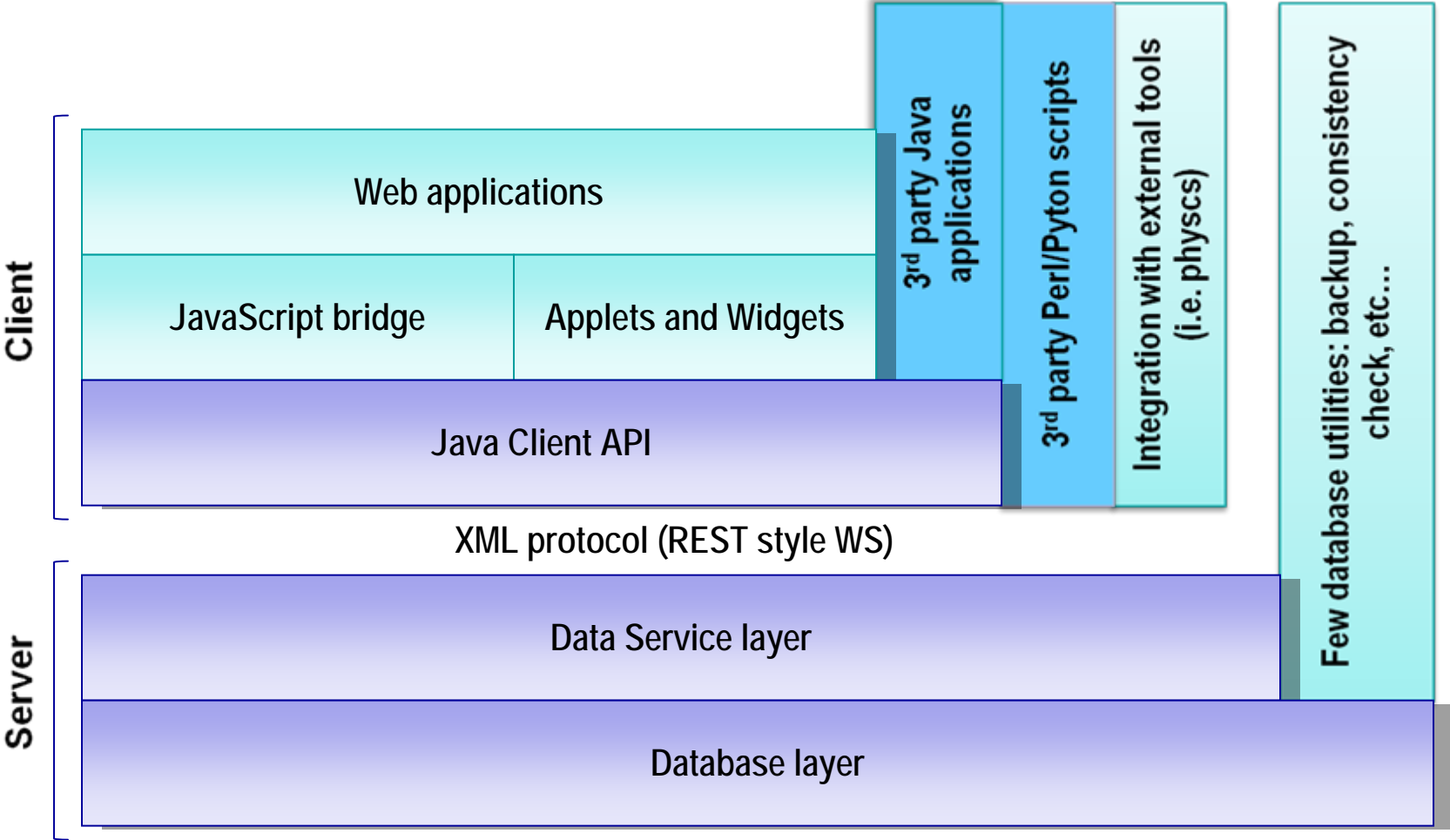
- IRMIS Inaugural Meeting, APS, March 2005
- IRMIS Collaboration Meeting, APS, May 2006

www.aps.anl.gov/epics/irmis

- IRMIS meetings are usually held in collaboration with EPICS meetings.

The present BNL work extends this collaborative effort.

IRMIS – 3 of 4



IRMIS – 4 of 4

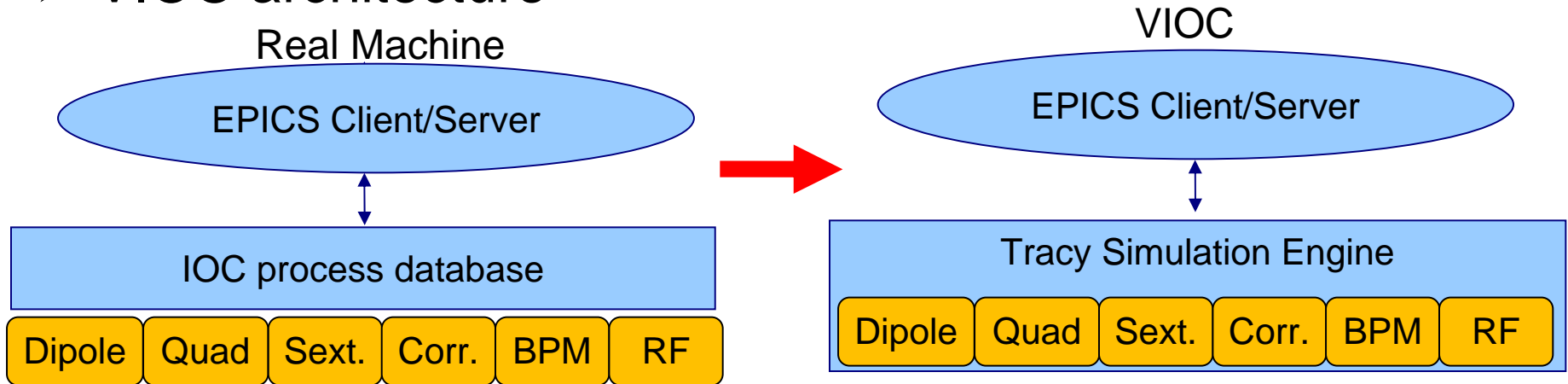
The screenshot displays the IRMIS Component Browser application. The browser's address bar shows the URL "IRMIS Component Browser". The main interface is titled "Component Browser" and features the IRMIS logo in the top right corner.

The interface is divided into several sections:

- Find component...:** A search bar at the top left.
- Control, Housing, Power:** Three tabs for navigating between different component categories. The "Control" tab is currently selected.
- Component Tree:** A hierarchical list of components. Under the "Control" tab, the tree shows a "VME Chassis-Mupac" folder containing several sub-folders, including "EVR100 0" which is highlighted.
- Control:** A panel showing the selected component's location within the hierarchy: "Network" > "MVME 167-xxx DBL iocrf5mon" > "VME Chassis-Mupac" > "EVR100 0".
- Housing:** A panel showing the component's physical location: "Site" > "Building 420" > "Room A014 A014" > "Rack 01 01" > "VME Chassis-Mupac" > "EVR100 6".
- Power:** A panel showing the component's power supply path: "SG-R1" > "Breaker CB-R13" > "Panel TDP-R2 TDP-R2" > "AC Circuit (120V) 31,33,35" > "AC Panel TRPC-R1 TRPC-R1" > "AC Circuit (120V) 20" > "120VAC Power Strip" > "VME Power Supp" > "VME Chassis-Mupac" > "EVR100 -".
- Component detail:** A panel showing the specific ports of the selected "EVR100" component: "Ports" > "DATA RECEIVE(Fiber Optic:FO-ST-F)", "DATA XMIT(Fiber Optic:FO-ST-F)", "OUT(Lemo:Lemo2-F)", "CLOCK IN(Lemo:Lemo1-F)", "CLOCK OUT(Lemo:Lemo1-F)", and "VME P2(Miscellaneous:DIN-96-M (a b c))".
- Diagram:** A small schematic diagram showing the "EVR100" component connected to a "VME Chassis-Mupac" component.

Virtual IOC – 1 of 2

➤ VIOC architecture

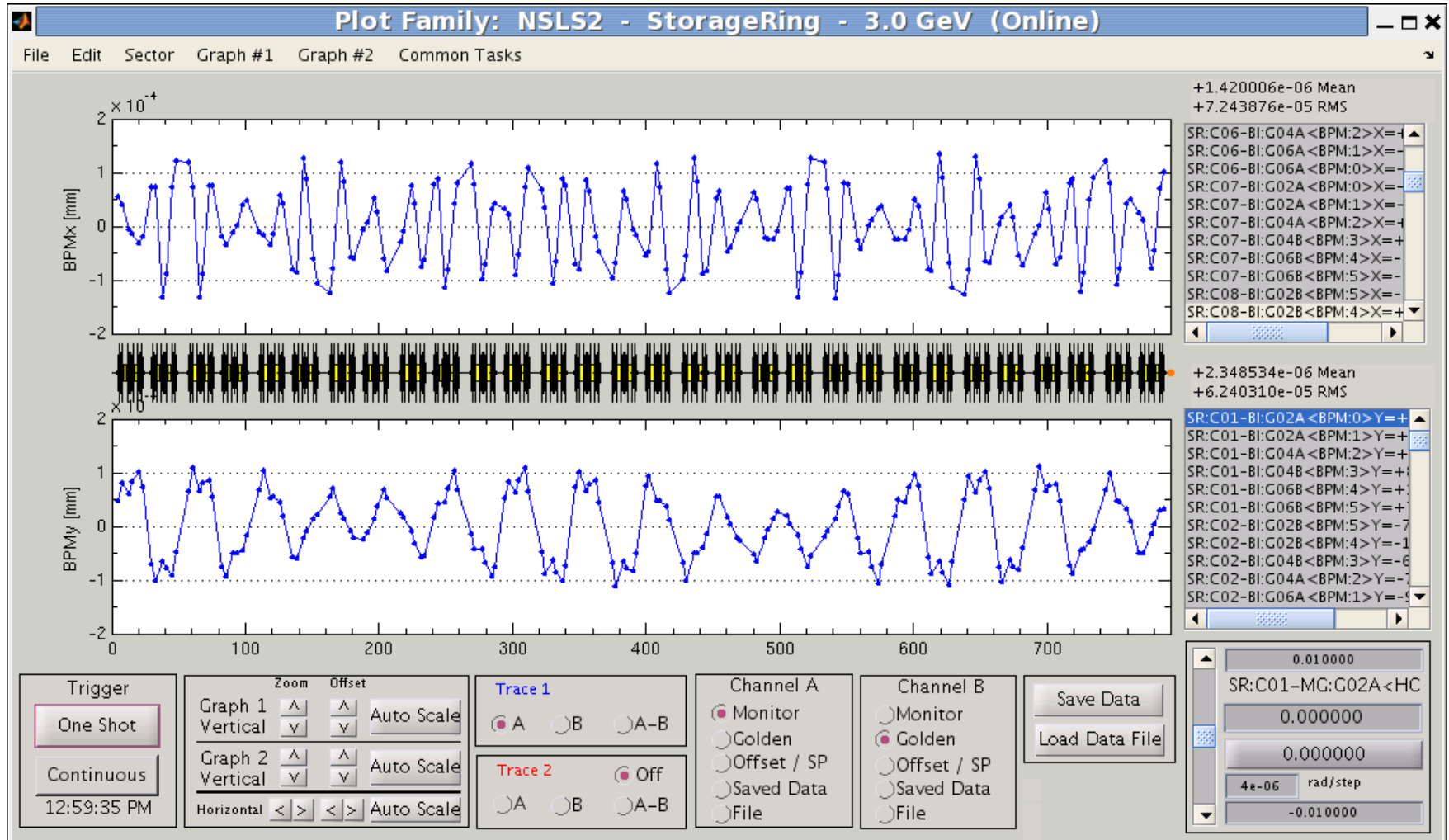


➤ Tracy simulation engine

Version	Track	Repetition	Lattice(30 Cells) (Idea, no error)	Support function	
				Set	read
3.5	linear	0.5Hz	CD3-Jun20	Magnets, & RF	Magnets, RF, & BPM

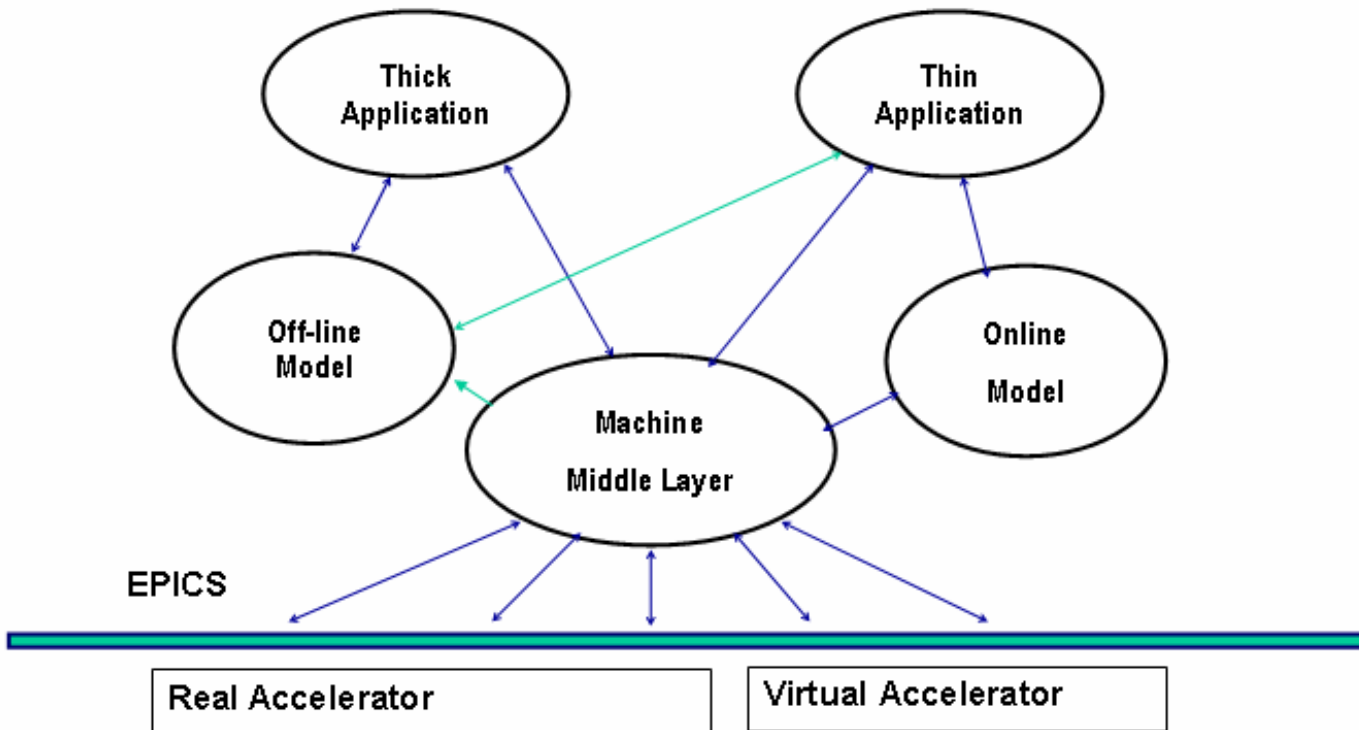
Virtual IOC – 2 of 2

Closed Orbit from VIOC:



High Level Application Environment – 1 of 3

Rationale: Open environment based on the **standard publish/subscribe specification** addressing the different types of the accelerator high level architectures and applications



High Level Application Environment – 2 of 3

Standard Publish/Subscribe Specifications

Middleware	Language	Data Type	Data Content Filtering	QoS	Complexity	Year
CORBA Event Service	C++, Java, ...	Generic and typed events	no	no	hard	1997
CORBA Notification Service	C++, Java, ...	Structured events	yes	yes	hard	~2000
Java Messaging Service (JMS)	Java	five types: text, map, bytes, stream, object messages	filters are message properties	no	easy	~2000
High Level Application (HLA)	C++, Java, ...	Sequence of octets	no	yes	TBD	~2000
Data Distribution Service (DDS)	C++, Java, ...	User-specific data types	yes	yes	easy	2004

High Level Application Environment – 3 of 3

- DDS/DCPS specification addresses the different types of the high level accelerator architectures and applications
- Functionality of two major DDS products has been evaluated:
 - OpenSplice offers an immediate commercial solution
 - openDDS is a free open source software that implements core DDS services. But it has to be extended with the content filtered topic and Java support
- In one year we plan to build the alpha/beta version of the DDS-based accelerator high level architecture and deploy the composite full-scale application providing the comparison of design and operational optics extracted from turn-by-turn data of a virtual accelerator.

Concluding Remarks

- 50% of Control System Design is completed
- Hardware standardization is being aggressively pursued with PLCs, processors, and crates being evaluated.
- All areas of development are making good progress.
- All subsystems should be prototyped in FY09, early FY10 time frame.