

Control System for NSLS Booster Power Supply Upgrade II*

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Summary

The booster at the NSLS is being upgraded from 0.75 to 2 pulses per second by means of the installation of new dipole, quadrupole, and sextupole power supplies. Here we outline the design of the power supply control system.

INTRODUCTION

Due to the complex nature of the control functions required in these power supplies(1), it was decided early on that the control system would be based on digital signal processing. Since this would produce a system configuration which would be difficult to debug using normal techniques, a design for test philosophy was adopted at the outset. This paper outlines the global design of the control system, and how the test facilities are implemented.

SYSTEM DESIGN

The control system consists of a VMEbus crate which holds the signal processing elements, and one VME crate which holds the gate drivers. The processor crate is equipped with two P1 and one P2 backplanes. The gate driver crate is not provided with either bus, but is wire wrapped. The two crates are connected together by means of a 61 conductor cable. Fig.1 shows the arrangement of circuit packs in the processor crate and the bussing scheme.

The first four slots are reserved for the NSLS control system interface. A remote ramp generator crate receives compressed ramp files, and a local processor converts this to sampled data points which are transferred by means of an optical fiber bus extender to the ramp memory located in the ramp generator. During power supply ramping, this data is read cyclically, and transferred over the VSBbus for processing in the servo. It will be noted that the ramp generator serves as the communication link between the two systems. The ramp generator contains a 2K x 16 page of dual port ram.

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The NSLS control system is able to turn the power supply on or off, and is able to control the ramps by writing into this memory page. The power supply controller passes status information by means of the same memory.

The power supply interlock and status is controlled by means of a PLC. This communicates with the processor on the ramp generator by means of an RS-232 link. The PLC in addition to its interlock functions, monitors the temperature of each transformer in the power supply by means of platinum RTD's buried in the windings. This temperature data is made available to the NSLS control system to allow for fault prediction.

DESIGN FOR TEST

The previous article (2) describes how use is made of the JTAG IEEE 1149.1 test bus for downloading and debugging the processor module. This approach was not used on the application modules. Instead, the more direct means communicating over the VMEbus is used. Each application module has two bus accesses. Real time data is passed over the internal P3 bus, while test data is passed over the VMEbus. Registers which are associated with test functions only appear only on the VMEbus, while data registers appear on both. In this way, for development purposes, the device may be used for real time applications over the VMEbus, and test programs may be run on the host processor and communicate with the module directly, bypassing the necessity of first downloading to a DSP, and then communicating over the internal bus. Since a VME slave may be constructed using six 300 mil DIPs, this is a simple and economical approach.

CIRCUIT PACK TESTING

In order to demonstrate the application of the design for test philosophy, we may consider the trigger generator.

The function of the trigger generator is to provide the 32 gate drive pulse trains required to trigger the thyristors in the power supply(3). This function is accomplished by means of a state machine consisting a number of counters, look-up tables, and decoding logic, driven by a 5.89 MHz clock. The primary test functions provided were the facility to disable the real-time clock, and substitute a clock which is generated

under program control, and the provision of read ports for the values contained in the various entities comprising the state machine. The module is placed in the test mode by setting a bit in the mode control register. Setting a bit in the diagnostic control register disables the real-time clock, while setting an additional bit enables the test simulation clock. Additional control bits allow counters and registers to be reset or loaded with defined values. The default values on power up are for normal operating mode. Debugging during the design process was accomplished by writing a C program which ran on the host PC, and which used function keys to define load/reset functions. Registers were displayed on the terminal in various colors, and in patterns which clearly showed the interrelations. The clock was incremented either by defining the number of pulses, or by single-stepping. In this way, the state machine was initialized to a known state, then single stepped to verify that subsequent states were as predicted. This feature proved its worth by allowing an obscure error in a look-up table to be quickly identified and corrected.

For production and subsequent equipment maintenance, a program will be written which will step through a defined sequence, and compare inputs to outputs. In this way it will be possible to diagnose the majority of errors quickly, and without resorting to test equipment. This may be done without removing the circuit pack from the control bin by simply taking the system off-line, and loading the test program to the host.

SYSTEM TESTING

A failure mode which can cause damage to the power supply during operation is the misfiring of one or more thyristors. This may be caused by insufficient or complete loss of gate drive. This failure will produce high output ripple, and in the case of the dipole supply, will bring the 10 KW filter damping resistor to red heat in very short order. Although the filter current is monitored by an over-current relay, a backup is provided by measuring the gate current and drive voltage in each thyristor, to determine if it falls within prescribed limits. This allows a soft failure to be tracked and corrected before it becomes a hard failure.

This diagnostic capability is achieved by providing a current transformer in each gate drive channel. A multiplexer in the gate driver circuit pack selects the appropriate channel, and transmits the analog signal to the gate driver controller. An A/D converter digitizes the voltage and stores the result in a memory. This memory is read over the VMEbus interface by the host.

In this way, the host may continually monitor the gate drive parameters. The voltage waveform is also made available on a BNC connector so that it may be monitored on an oscilloscope. During commissioning, a test routine allows the selection of thyristors under operator control.

CONCLUSION

The implementation of a control system based on digital signal processing techniques involved a substantial degree of effort. However, it was anticipated that results would be obtained which could not be achieved with an analog system. This has proven to be the case. Initial testing of a prototype of the feed-forward portion of the servo on the old booster dipole power supply (2,4), resulted in a factor of 20 decrease in acquisition time and a factor of 5 increase in tracking accuracy. The feed-forward system is representative of many of the control functions which must be executed in this type of system. Transfer functions of arbitrary complexity may be implemented by cascading simple routines. Many of our filters have been realized by cascading IIR filter sections such as that shown in Fig. 2

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