LOW LEVEL RF CONTROL SYSTEM OF J-PARC SYNCHROTRONS

Fumihiko Tamura*, Alexander Schnase, Masahiro Nomura, Masanobu Yamamoto
JAERI, Tokai-mura, Ibaraki-ken, Japan 319-1195
Masahito Yoshii, Shozo Anami, Eizi Ezura, Keigo Hara, Chihiro Ohmori, Akira Takagi
KEK, Tsukuba, Ibaraki-ken, Japan 305-0801

Abstract

We present the concept and the design of the low level RF (LLRF) control system of the J-PARC synchrotrons. The J-PARC synchrotrons are the rapid cycling 3-GeV synchrotron (RCS) and the 50-GeV main ring (MR) which require very precise and stable LLRF control systems to accelerate the ultra-high proton beam current. The LLRF system of the synchrotron is a full-digital system based on direct digital synthesis (DDS). The functions of the system are (1) the multi-harmonic RF generation for the acceleration and the longitudinal bunch shaping, (2) the feedbacks for stabilizing the beam, (3) the feedforward for compensating the heavy beam loading, and (4) other miscellaneous functions such as the synchronization and chopper timing. The LLRF system of the RCS is now under construction. We present the details of the system. Also, we show preliminary results of performance tests of the control modules.

INTRODUCTION

J-PARC [1, 2] is a project of high-intensity proton accelerator complex which consists of 400 MeV linac, 3-GeV Rapid cycling synchrotron (RCS), and 50-GeV synchrotron (MR). We discuss the concept and the design the low level RF (LLRF) control systems of the synchrotrons. To accelerate the ultra-high intensity proton beam, the LLRF control systems of the J-PARC synchrotrons must be very stable and precise.

The RF parameters of the synchrotrons are listed in Table 1. Magnetic Alloy (MA) loaded cavities are used to achieve high accelerating voltages. The MA cavities of the J-PARC have low Q-values and require no tuning loop. Thus, employing the MA cavities makes the LLRF system more simple.

The Q-value of the RCS cavity is chosen as 2. A single cavity is driven by the superposition of multi-harmonic RF signals; the fundamental ($h = 2$) signal is for the acceleration of the beam and the second harmonic ($h = 4$) is for the bunch shape control by modifying the RF bucket.

The system is a full-digital system based on direct digital synthesis (DDS). We discuss on the LLRF blocks in the following section.

The LLRF system of the RCS is now under construction and we mainly discuss on the details of the RCS LLRF system. However, the basic concepts of the MR LLRF system is similar to the RCS one. Preliminary tests of the LLRF modules have been performed and the results are also shown in the following section.

parameter	RCS	MR
circumference	348.3 m	1567.9 m
energy	0.181–3 GeV	3–50 GeV
Accel. freq.	0.94–1.67 MHz	1.67–1.72 MHz
harmonic number	2	9
max RF-voltage	450 kV	280 KV
repetition period	40 msec	3.64 sec
duty (power)	30%	60%
No. of cavities	12	6
Q-value	2	10–20
No. of gaps	3 per cavity	3 per cavity
average power	120 kW/cavity	240 KW/cavity

Table 1: Parameters of the J-PARC synchrotron RF

LLRF CONTROL BLOCKS

The block diagram of the LLRF system is shown in Figure 1. The LLRF control system consists of the following blocks.

- the multi-harmonic RF generation for the acceleration and the longitudinal bunch shaping
- the feedbacks for stabilizing the beam
- the beam feedforward for compensating the heavy beam loading
- other miscellaneous functions such as the synchronization and chopper timing.

The multi-harmonic RF signals are generated for driving the cavities and for the reference of the RF signal detection (I/Q modulation etc.). A schematic of the DDS is shown in Figure 2. The pattern generator gives a phase-increment at each clock cycle, and the phase accumulator generates a saw-tooth phase signal at the beam revolution frequency. Finally, the phase signal is converted into sine-wave by coordinate transformer. By basic arithmetic operation, higher harmonic phase signals are generated. The DDS can generate the multi-harmonic signals without PLL and the fundamental and the higher harmonic signals are easily synchronized.

These functions are realized in the modules named "SPG (main synthesizer)" and "RFG (RF generation board)" in

* ftamura@linac.tokai.jaeri.go.jp

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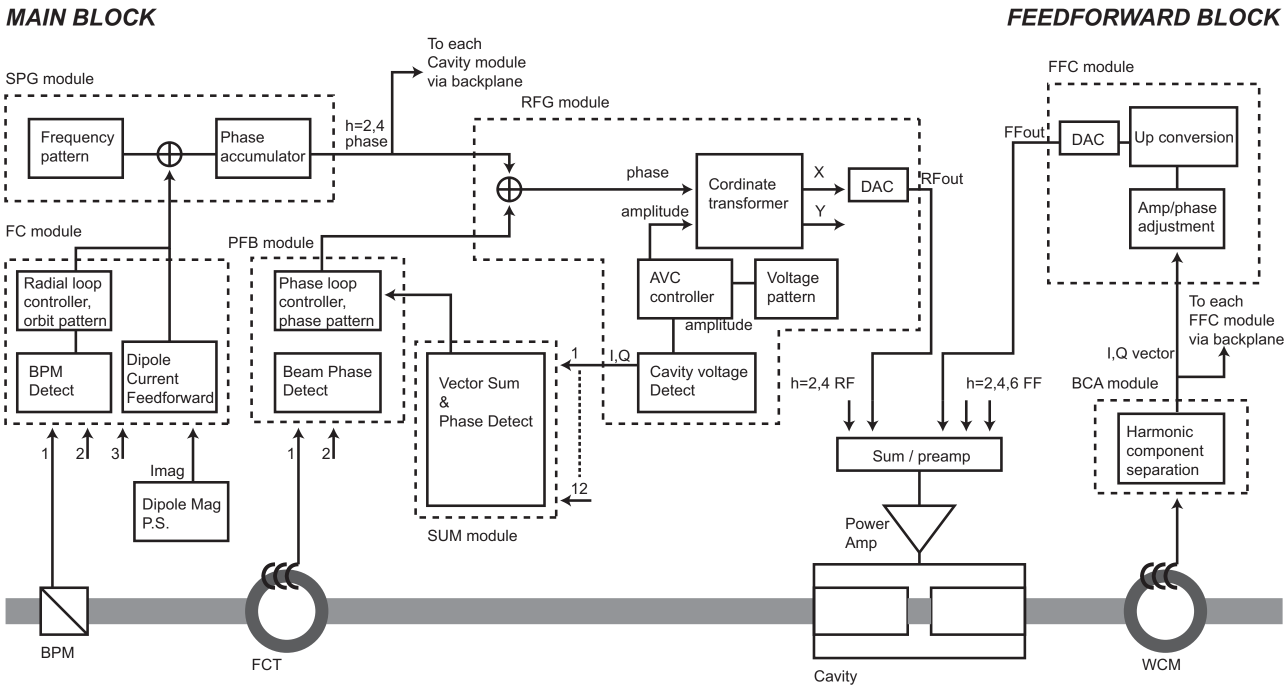

Figure 1: Block diagram of RCS LLRF system

Figure 1.

The feedback loops of the J-PARC RF are common ones. Each RF cavity has the auto voltage control (AVC) to follow the programmed voltages of both $h = 2$ and $h = 4$. The radial loop controls the RF frequency referring the beam orbit. Three beam position monitors (BPM) are used and the signals from the BPMs are averaged with proper weights. The phase loop is for damping the synchrotron oscillations. The phase loop compares the beam phase picked up by fast current transformers (FCT) and the vector-sum of the RF voltage of the twelve cavities. The details and the stability of the loops are discussed in the presentation of the this conference [3].

In Figure 1 the RFG board has the AVC function, and the "PFB (phase feedback)" and "FC (frequency control)" boards are for the phase feedback and the radial loop, respectively.

Since the beam current is fairly high, the beam loading effects should be considered carefully [4]. In the J-PARC RCS, the beam feedforward method is employed for the beam loading compensation [5, 6].

The RF compensation signal is generated so that the final amplifier generates a current which cancels the wake voltage. Since the wake voltage consists of not only the fundamental accelerating RF component ($h = 2$), but also the other harmonics ($h = 4, 6$). Each harmonic component must be adjusted in amplitude and phase because of the frequency response of the RF system.

The BCA (beam current analysis) module properly selects the harmonic component of the beam signals picked up by the wall current monitor (WCM). The I/Q vectors of the seleted harmonics are sent to the individual FFC (feedforward cavity driver) modules. Proper RF signals are generated by the FFC.

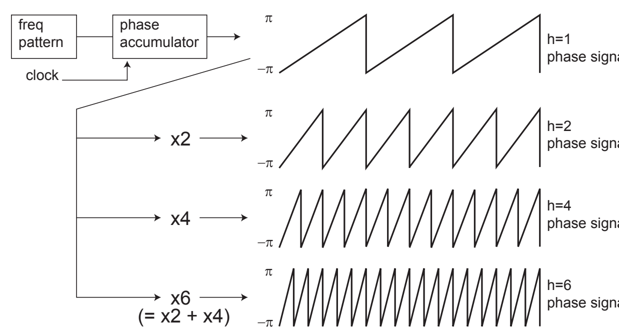

Figure 2: Direct Digital Synthesis (DDS)

The other miscellaneous functions are also necessary to receive and send the beam to the other facilities in the J-PARC. The timing of the beam chopper in the linac is generated by the RCS RF system. Also, the synchronization of the beam in the RCS to the MR or the neutron choppers is important function. The synchronization system is now under designing.

We are building these LLRF modules/blocks with FPGAs. The high-performance arithmetic functions of FPGA is especially important for the realization of FIR filters which is necessary for the RF signal detection. Also, the re-programmable feature makes the debugging more efficiently. Figure 3 shows the RFG board and two VertexII-pro FPGAs are used on the board.

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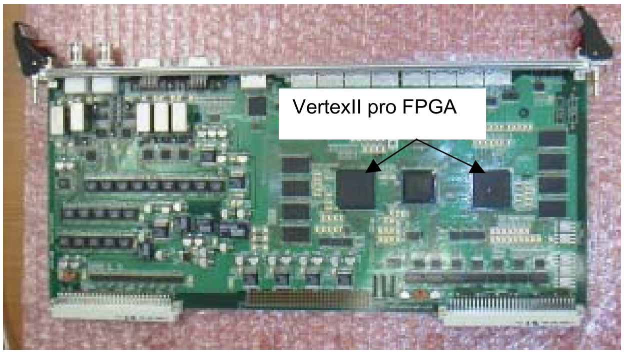

Figure 3: RFG (RF generation) board

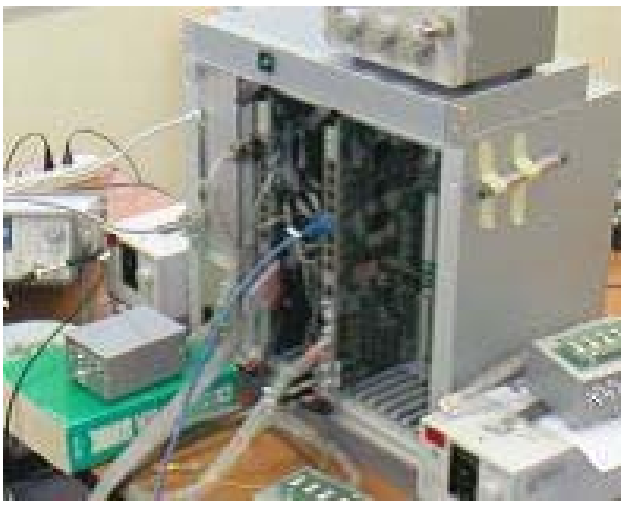

Figure 4: 9U VME chassis, SPG and RFG boards, under testing

AVC PERFORMANCE

By combining SPG and RFG boards, we have performed preliminary tests of AVC loops. In the test the low-level RF output is connected to the cavity voltage input with an external variable attenuator. The RF frequency was set to 1 MHz. The AVC has a PID controller with the gains of X_p, X_i, X_d for the proportional, integral and differential part, respectively.

Figure 5 shows the step responses of the error signals from the AVC controller with the stable condition. With a condition of $X_p = 1$, $X_i = 0.2$, $X_d = 0$, the error signal went to zero in 50 μsec without any ringing.

The details of the test are described in [3]. Tests in more realistic situation are to be done.

SUMMARY

We summarize the presentation as follows.

- MA-loaded RF cavities are employed in the RF systems of the J-PARC RCS and MR.
- The DDS-based full-digital LLRF control system is designed to accelerate the ultra-high proton beam current. The multi-harmonic RF signal is generated without PLLs.
- The common feedback loops are used; AVC, phase loop and radial loop.
- We employ the beam feedforward method for compensating the heavy beam loading.
- The RCS LLRF system is now under construction. Preliminary tests of the AVC have been performed.

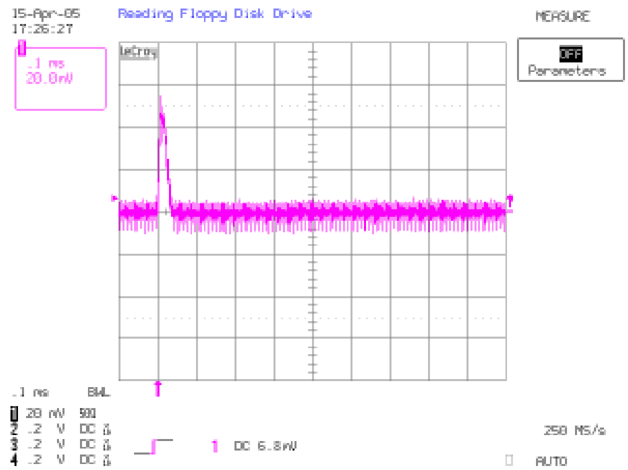

Figure 5: A stable condition: $X_p = 1$, $X_i = 0.2$,$X_d = 0$. The error signal shows no ringing.

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