MEASUREMENTS ON A 12.5 kV PROTOTYPE INDUCTIVE ADDER FOR THE CLIC DR EXTRACTION KICKERS

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Abstract

The CLIC study is investigating the technical feasibility of an electron-positron collider with high luminosity and a nominal centre-of-mass energy of 3 TeV. The pre-damping rings and damping rings (DRs) will produce ultra-low emittance beam with high bunch charge. To avoid beam emittance increase, the DR kicker systems must provide extremely stable field pulses during injection and extraction of bunches. The DR extraction kicker system consists of a stripline kicker and two pulse modulators. The current specifications for the modulators call for pulses with 160 ns or 900 ns flat-top duration of ±12.5 kV and 305 A, with ripple of not more than ±0.02% (±2.5 V). An inductive adder is a very promising approach to meeting the specifications because analogue modulation methods can be applied to adjust the output waveform. Recently, the first full-scale, 20-layer, 12.5 kV prototype inductive adder has been assembled at CERN and testing has commenced. The goal is to tailor the output waveform of the prototype to the waveform required for the DR extraction stripline kicker. The results of the initial tests and measurements are presented.

INTRODUCTION

The Compact Linear Collider (CLIC) would be a high-energy electron-positron collider [1]. It could provide very clean experimental environments and steady production of all particles within the accessible TeV energy range. To achieve high luminosity at the interaction point, it is essential that the beams have very low transverse emittance: the Pre-Damping Ring (PDR) and Damping Ring (DR) damp the beam emittance to extremely low values in all three planes.

Stripline kickers are required to inject beam into and extract beam from the PDRs and DRs [2]. Jitter in the magnitude of the kick waveform causes beam jitter at the interaction point [3]. Hence, in particular, the DR extraction kicker must have a very small magnitude of jitter: the 1 GHz specifications call for a 12.5 kV pulse of 160 ns duration flat-top, with a combined ripple and droop of not more than ±0.02 % [1]. The 2 GHz specifications call for a burst of two 160 ns duration pulses with 580 ns between the end of the flat-top of the first pulse and the beginning of the flat-top of the second pulse, which can also be fulfilled with a single 900 ns, continuous, flat-top pulse: the requirements for the voltage and stability during two 160 ns flat-top sections are the same as for 1 GHz design, i.e. ±0.02 % [1]. The flat-top repeatability requirements are also extremely tight, ±0.01 %, for both RF system designs [1].

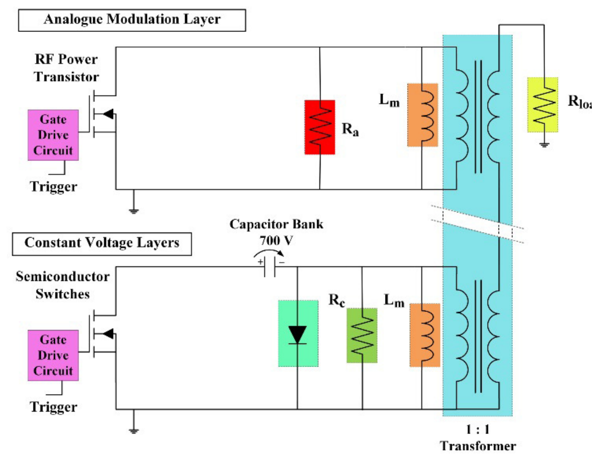

Figure 1: Schematic of an inductive adder with a single constant voltage layer with core loss resistance R_c and magnetizing inductance L_m, and with an analogue modulation layer with modulation resistance R_a, magnetizing inductance L_m and an RF power transistor.

THE INDUCTIVE ADDER

A review of literature of existing pulse generators has been carried out and an inductive adder (Fig. 1) has been selected as the most promising means of achieving the specifications for the DR kickers [4]. The inductive adder is a solid-state modulator, which can provide relatively short and precise pulses. With a careful design of the adder, it may be possible to directly meet the ripple and droop requirements of the PDR kicker and analogue modulation may provide a means to meet the demanding specifications for the DR kicker [5, 6]. The reasoning for choosing the main components of the inductive adder has been given in [6]. Two 5-layer prototype inductive adders have been assembled at CERN. The design parameters and the initial results for these pulse modulators were presented in [7] and [8]. The prototype inductive adders have been equipped with an analogue modulation layer, which can be used to compensate the droop and ripple of the output waveform. Operation of the passive and active modulation layers has been verified with measurements and the results have been presented in detail in [9-11]. Evaluation of magnetic cores for the full-scale, 12.5 kV, 250 A, prototype inductive adder was presented in [12]. Three recent papers [12-14] presented initial measurements on the first five layers of the full-scale prototype inductive adder and this paper is a continuation of that study. The detailed electrical design of the full-scale prototype inductive adder was presented in [13].

SPECIFICATIONS FOR THE 12.5 KV PROTOTYPE INDUCTIVE ADDER

Table 1 shows the specifications for the 12.5 kV prototype inductive adder for the CLIC DR. In the CLIC DR kicker system, the inductive adder generates pulses for a stripline kicker, which has an average odd-mode impedance of 40.5 Ω during a pulse [2]. The striplines may be terminated with their odd-mode characteristic impedance and therefore the nominal output current of the inductive adder, at 12.5 kV, would be 309 A. The full-scale prototype inductive adder has been designed to supply pulses with up to 900 ns flat-top duration. The specification for the maximum allowed total pulse duration, including rise and fall time and flat-top, is 2.2 μs [1]. However, to limit stress on the kicker system, the desired rise and fall times are in the range of 100 ns. The required pulse flat-top stability of ±0.02 %, i.e. ±2.5 V in absolute numbers for ±12.5 kV operation, defines the allowance for the combined droop and ripple for a single pulse. The pulse flat-top repeatability defines the allowed difference of any consecutive pulses and it is specified to be ±0.01%, which corresponds to ±1.25 V, for ±12.5 kV operation.

Recent simulation studies of the CLIC DR extraction kicker striplines have shown that, in order to achieve the required stability for the total of the deflecting magnetic and electric fields, the waveform for the kicker should be a "controlled decay waveform", as shown in [15], instead of a perfect "flat-top" pulse. The flat-top stability and repeatability requirements for the output pulse of an inductive adder remain unchanged, however the shape of the output waveform must now be compared to a simulated, optimum, pulse waveform instead of a flat-top pulse.

Table 1: Specifications for the 12.5 kV Inductive Adder for CLIC DR Extraction Kicker Inductive Adder

Output Voltage	12.5 kV
Nominal output impedance	50 Ω
Output current	309 A
Flat-top duration	160 ǀ 900 ns
Desired pulse rise/fall times	100 ns
Flat-top stability	±0.02 %
Flat-top repeatability	±0.01 %

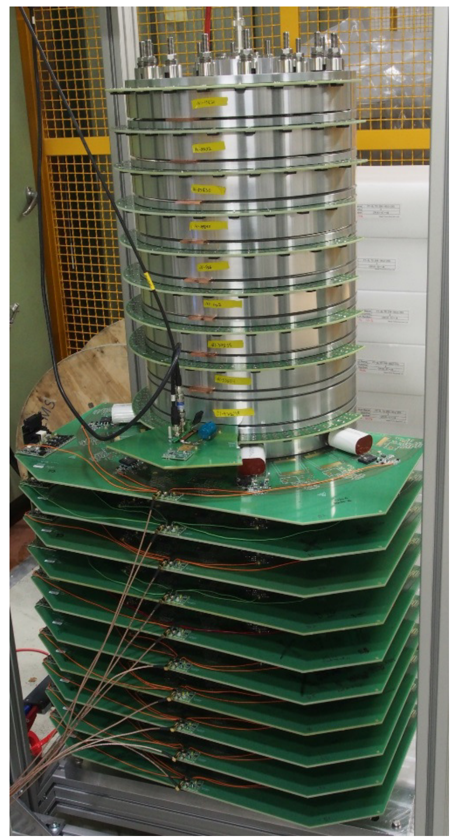

Figure 2: Prototype inductive adder with 10 constant voltage layers and 1 analogue modulation layer (the topmost PCB).

MEASUREMENTS ON THE FULL-SCALE PROTOTYPE WITH 10+1 LAYERS

Measurement Set-up

Measurements shown in this paper were carried out with a prototype inductive adder with 10 constant voltage layers and a single analogue modulation layer installed, and space for further nine constant voltage layers (Fig. 2). The primary circuit of each constant voltage layer consisted of a single printed circuit board (PCB) with four current branches powered. Each current branch consisted of either a single NWL T00216, 12 μF, [16] or a Leclanché PPM-4 170-23.0, 12 μF [17], pulse capacitor, and an APT12057LFLL [18] MOSFET. Each cell of the inductive adder was equipped with two Finemet FT-3L type magnetic cores [12, 19]. The nominal maximum output voltage of the set-up was 6.8 kV, corresponding to approximately 700 V per layer with 10 constant voltage layers. The output waveform was recorded with a Rohde & Schwarz RTO1004 oscilloscope [20], which has a specified resolution of 14 effective bits in the required bandwidth, 100 MHz. The primary circuit of the analogue modulation layer consisted of a 2.4 Ω resistor in parallel with a radio-frequency power MOSFET, type ARF463AP1G [18].

Measurements on a Flat-top Pulse

The goal of the measurements shown in this paper was to verify that the controlled decay waveform, required for the CLIC DR extraction kickers, can be generated by the prototype inductive adder. However, the starting point was a flat-top pulse (Fig. 3), generated by applying active analogue modulation. In this measurement, at 6.345 kV, the flat-top stability was ±0.02 % (±1.6 V) for the best 160 ns section during the flat-top and ±0.07 % (±4.6 V) for 900 ns duration. This fulfils the relative stability requirement for the 1 GHz specifications for the CLIC

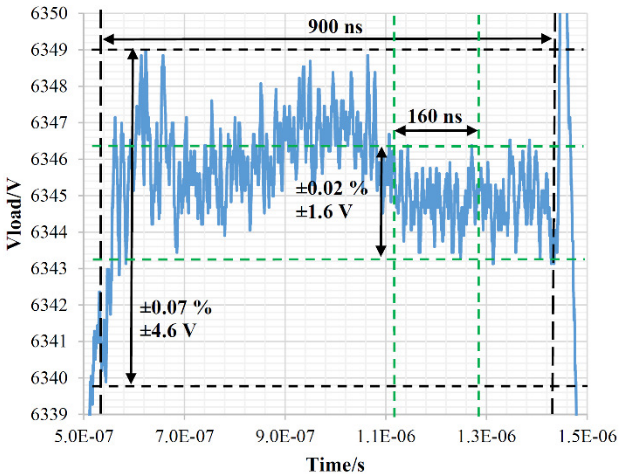

Figure 3: Measured flat-top waveform of the prototype inductive adder with 10 constant voltage layers and a single active analogue modulation layer.

DR extraction kicker system, i.e. ±0.02 % for 160 ns [1],at a half of the nominal voltage of the inductive adder.

The waveform in Fig. 3 is an average of 100 measured pulses, in order to improve the resolution of the measurement. In earlier measurements with a 5-layer prototype at CERN, presented in [12], ±0.01 % flat-top stability for 160 ns and ±0.04 % for 900 ns flat-top duration were measured at 2.4 kV: hence the measured flat-top stability was slightly better at lower output voltage. However, in the measurement shown in Fig. 3, the compensation waveform applied for the analogue modulation layer was a section of a sinewave, and found by manual tuning. Compensation could be improved further by iterations in the time domain or analytically in the frequency domain, by comparing Fast Fourier Transforms of the required waveform and the measured waveform. The steps for the frequency domain corrections have been described in detail in [14].

Measurements on a Controlled Decay Waveform

Figure 4 shows a simulated optimum controlled decay waveform (green) with error margins for stability, i.e. ±0.02 % (black and grey, dashed) and a measured waveform (blue). In addition, the maximum error between the measured and simulated optimum waveform, +0.1 %, is shown as an envelope curve (red, dashed). The measured load voltage in Fig. 4 is an average of 100 pulses. A point to note in Fig. 4 is that the simulated, optimum, waveform was normalised to have a maximum amplitude of 6.3 kV, which is a half of the required nominal output voltage: at this voltage, the modulation range of the analogue modulation layer of the prototype inductive adder is adequate to generate the required waveform. The main reason for the difference between the simulated and measured waveforms was a small error in the manually chosen control signal: the piece-wise linear control signal used in this measurement did not generate a perfectly matching waveform for the simulated decay waveform. However, this was not due to hardware limitation and, therefore, matching can be improved

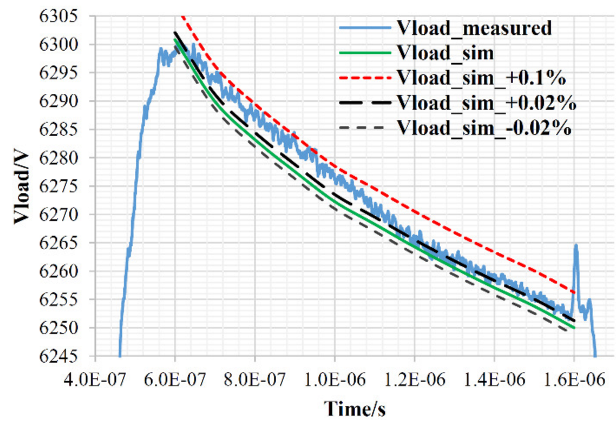

Figure 4: Simulated optimum waveform for CLIC DR extraction kicker (green) with ±0.02 % stability margins (black and grey, dashed), +0.1 % error envelope (red, dashed) and an average of 100 measured pulses (blue) of the prototype inductive adder with 10 constant voltage layers and a single active analogue modulation layer.

further, with the same means as described in the case of a flat-top pulse in the previous section.

CONCLUSION AND FUTURE WORK

This paper has presented initial measurements on the first 20-layer CLIC DR extraction kicker prototype inductive adder, with 10 constant voltage layers and an analogue modulation layer installed. Active analogue modulation was applied to the output pulses to generate a flat-top pulse and then subsequently to adjust the output waveform for the simulated optimum waveform required for the CLIC DR stripline kicker [15]. In the measurement shown in this paper, the maximum error between the simulated optimum decay waveform and measured waveform was +0.1 %. However, the matching can be improved further with the same hardware. Additional layers, up to a full complement of twenty, will be added to the inductive adder and measurements carried out at an output voltage of up to 12.5 kV.

In the near future, a second full-size 12.5 kV prototype inductive adder will be assembled: the final goal is to demonstrate the feasibility of the CLIC DR extraction kicker system with the required optimum controlled decay waveform with the required flat-top stability. In addition, an automated control system for compensation of the difference between the optimum decay waveform and the measured waveform of an inductive adder, based on frequency-domain analysis of the waveforms, is currently being designed. The prototype of the control system will be built with LabVIEW software package [21] and it will control existing hardware of the measurement set-up, i.e. a high-voltage power supply, low voltage power supplies and signal generators. Finally, the prototype inductive adders will be tested together with the CLIC DR prototype extraction stripline kicker [2] in an accelerator test facility.

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