DEVELOPMENT OF HIGH STABLE MAGNET POWER SUPPLY*

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Abstract

A high stable magnet power supply (MPS) was developed, which was a bipolar type with 200A of the output current at the 40V of output voltage. The MPS has been implemented by the digital signal processing technology using the DSP, FPGA, ADCs and so on. The output current stability of the MPS showed about 4 ppm peak-to-peak in a short term experiment at the 200A of its full output current. This paper shows the several design considerations being implemented to this high stable MPS. Some experimental data such as output stability, some waveforms and so on are given in this paper.

INTRODUCTION

The technologies of the magnet power supply (MPS) has been improving ceaselessly since the digital signal processing was introduced. The MPS using the analog technology had a good output stability less than 5 ppm shown in the SYSTEM 8000 from DANFYSIK [1]. The current stability of the MPS that was applied for the digital technology was not good as much as that of analog type at the beginning stage.

The better current stability of the MPS was continuously required by the accelerator physicists in order to get high quality of the electron or the particle beam. And it was getting popular in the world when the therapy accelerator machines (TAM), proton or heavy ion, were introduced to treat the various cancers. The high stable MPS was also essential in the TAM. The current stability of the MPS for the TAM was required to be ~ ppm. But it is not easy to develop a good stable MPS at the high output current higher than 100A.

In this paper, the MPS that showed the high stability at the 200A of output current with the magnet load was introduced. Some design schemes was described. The results of the experiments such as short term stability were showed.

SYSTEM CONFIGURATIONS

The designed MPS was the 200 A of output current and showed less than 4 ppm-pp at its full current output. The AC input stage was consisted of transformer and input LC filter. The transformer has a Wye configuration for primary and two secondary configurations of a Wye and Delta. Each winding of the secondary turns outputted 25 V. And they were connected in series to get 50 V after diodes rectifier. The diodes for the rectifier were assembled on an aluminium plate which was acted as a heat sink with cooling water.

The input LC filter configured with an inductor of 1 mH, which was common, and two capacitor banks of 48000 μF (12000μF x 4) for each converter module as shown in the Figure 1. The DSP & FPGA board generated eight PWM signals for two converter modules. The switching frequency for each converter module was 20 KHz thus it resulted in 40 KHz together by the bi-phase PWM signals. The output filters were implemented within the each converter module.

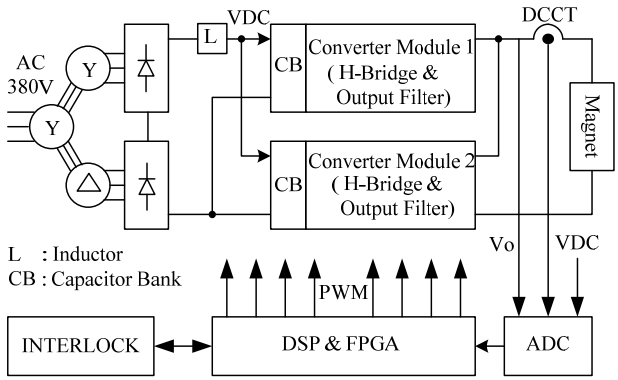

Figure 1: The block diagram of the designed MPS.

The Figure 2 showed two power converter modules. The PWM interface board was shown at the front part of the module. The IGBTs were assembled on the heat sink plate of water cooled near to the PWM interface board. The output filters were fabricated with four inductors and two capacitor boards next to IGBT plate. Finally, cooling fans for filters were mounted on the side wall of the module.

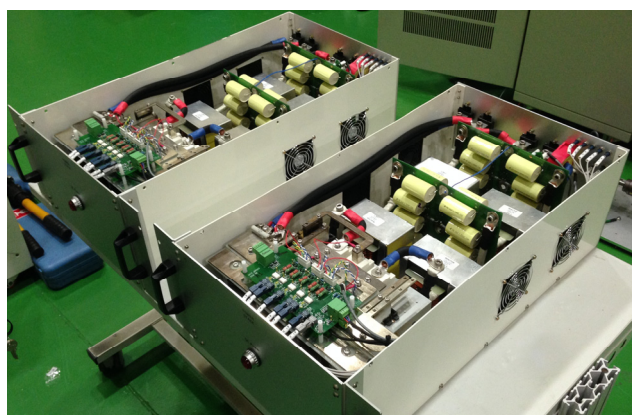

Figure 2: Power converter modules including output filters.

Figure 3 showed the new designed DSP board. The DSP daughter board was the commercial one which assembled a DSP TMS320F28335 from TI Co. The DSP daughter board makes easy in design and assembly. And it also benefits in developing stage when the DSP module was a failure and it was needed to be changed with the

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other one. Thus it saved the cost and time during the development. The FPGA SPARTA-3, right next to DSP, from Xilinx Co. was assembled next to DSP module in the DSP board.

The DSP communicated to the FPGA by the McBSP mainly and some extra GPIO signals. The FPGA generated the SPI interface signals for the each ADC chip. The FPGA performed the over-sampling process for the ADC data stream of the output current and voltage, respectively. It increased the extra resolution in number of bits from 12 to about 18. By virtue of this oversampling scheme, the MPS got the high stability of about ±1 ppm as shown in Figure 8. The FPGA also generated the interlock signals for output over current and voltage after calculated the average values during the given time interval.

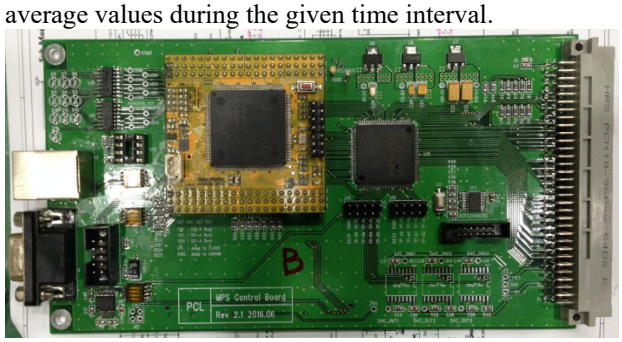

Figure 3: Assembled DSP and FPGA board.

The performance test of the ADC AD977 was carried out to confirm its accuracy. The Figure 4 was showed the signals stored by an oscilloscope during the AD977 test [2]. The input terminals of the ADC was connected by three alkaline batteries made up to 4.5V. The start conversion signal, SPI clocks and serial data frame were shown in the Figure 4. The conversion error was equivalent to about 4 bits which were shown from the lowest waveform in the Figure 4. Thus the equivalent noise voltage was about 2.4 mV at the 5 V reference input and its effective bit reduced to twelve. This was not enough for a high stable MPS of ~ppm performance.

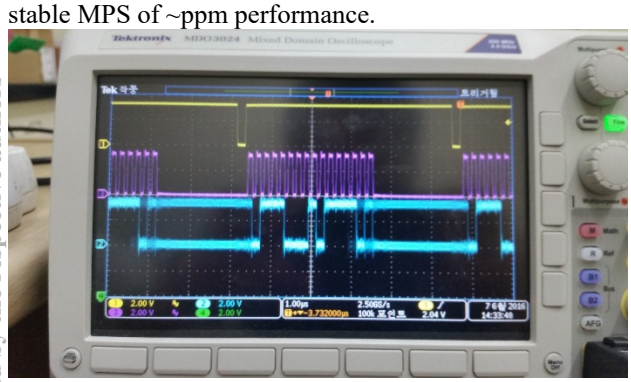

Figure 4: Conversion error of the AD977 ADC. Upper: start of conversion signal, middle: data clock, and lower: converter serial output signal.

Thus it is required to apply the oversampling techniques to increase the effective ADC bit. When oversampling was implemented, the signal-to-noise ratio was improved as the equation (1) [3].

$$SNR_{max}[dB] \cong 6.02N + 1.76 + 10log_{10}(k) \quad (1)$$

Where N is the ADC resolution and k is oversampling factor. The Figure 5 shows the concept of the oversampling scheme by sampling, average and decimation. Thus it improved the resolution of the ADC by w-bit [4].

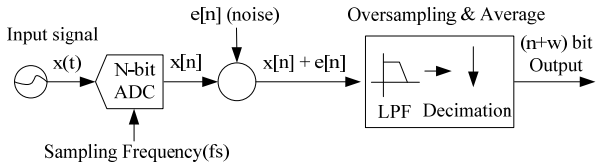

Figure 5: Oversampling and averaging process to increase effective bits.

The oversampling effects tested with the ADC AD977 were shown in the Table 1. The equivalent output noise was reduced as K values were increased from 32 to 4096

Table 1: Output Noise Value as K Value Increased

K value	32	64	128	256	512
Output [μV]	150	130	100	80	60
K value	1024	2048	4096	Remark	
Output [μV]	40	30	20		

The Figure 6 showed the data of the table 1. It appeared a little non-linearity that was caused by the reading error of a human. But it kept the trend of the effects by increasing the K value.

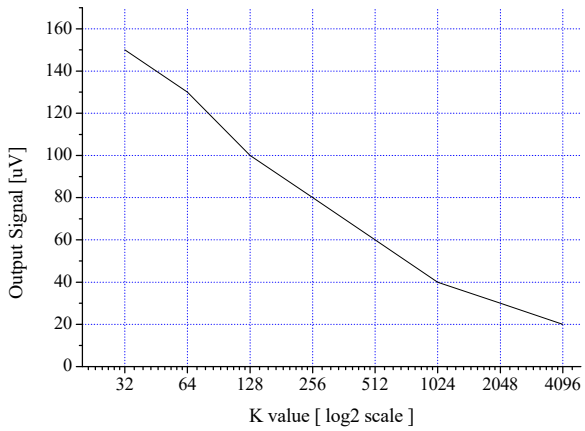

Figure 6: The effect of increase oh K value.

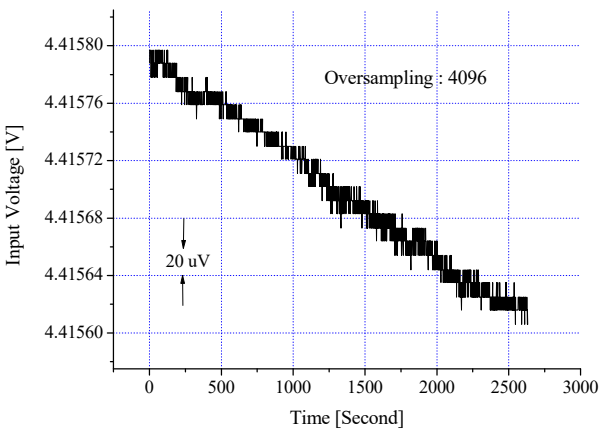

Figure 7 : ADC data after oversampling process with k of 4096.

The Figure 7 showed the ADC data after over-sampling process with the K value of 4096 at 4.5 V input by the three serialized batteries of 1.5V. The data after processing was about 20 μV, which was equivalent to 4 ppm at the 5 V of the reference voltage. The sampled ADC data were decreased slightly by the time because batteries continuously discharged through the equivalent input impedance of the ADC circuits. If the other voltage source was inputted, then this phenomenon won't appear, but ADC data would be showed large fluctuation.

EXPERIMENTAL RESULTS

An external DCCT of a ULTRASTAB 867-400I from DANFYSIK was set up to measure the output current stability precisely. This was completely isolated from the MPS not to interfere each other. There is another DCCT for the feedback control for the MPS. This is the same model as the external DCCT. The DVM HP3458A was used to convert the output current to digital with the burden resistors. The load was a dipole magnet of 166 mH and 109 mΩ, respectively. The current capability of tested magnet has 300 A with water cooling.

And the other instruments were included in this experiments such as temperature sensors, oscilloscope, current probe etc.

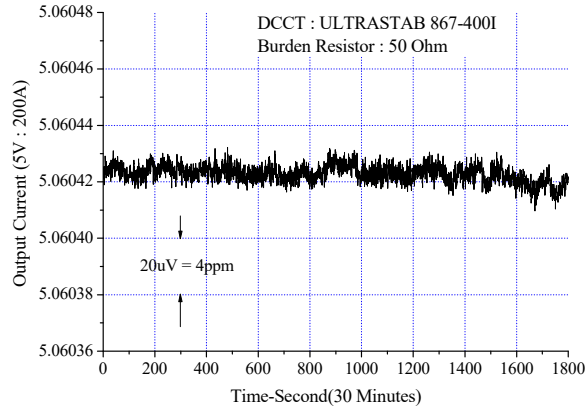

Figure 8: Measured output current stability for short term, 30 minute.

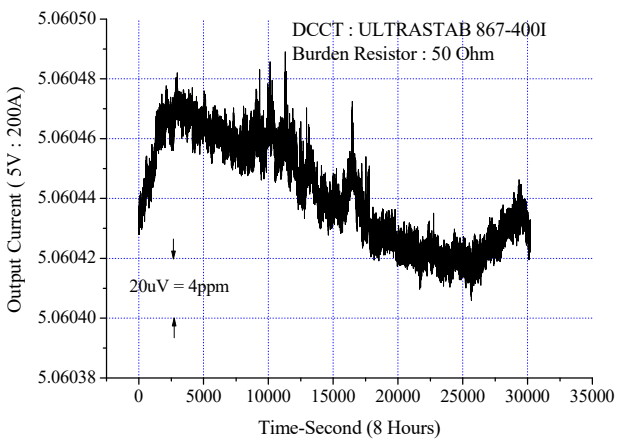

Figure 9: Measured long term current stability for 8 hours.

Short term stability of the MPS was measured for 30 minutes. It showed the less than 4 ppm-pp at its full output current of 200 A as shown in the Figure 8. It also showed the same stability at the -200 A current. But the instantaneous current stability was about 2 ppm-pp.

Long term stability for eight hours was also measured as shown in the Figure 9. It showed less than 20 ppm-pp. If temperature variation of the test were considered, the stability could be reduced to 10 ppm-pp.

The measured step responses were shown in the Figure 10: a) the violet: was the link DC voltage; b) the cyan was full output current of 200A; and c) the blue was output current of a single power converter module. The test showed no overshot at the output. The full link voltage was applied to the load magnet to minimize the rising time.

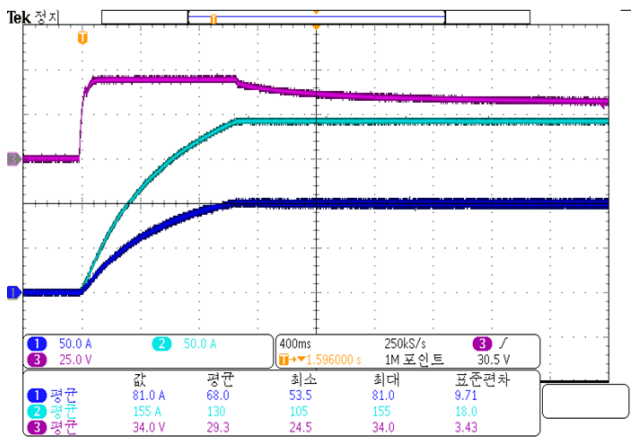

Figure 10: The output responses of the step input from 0 to 200 A.

CONCLUSIONS

The very high stable MPS was designed and assembled. Some experiments were carried out to confirm how high the output stability could be archived in the application of switching method. The short term stability for 30 minutes was less than 4 ppm-pp at the 200A of output. The long term stability was also very good, which was less than 20 ppm-pp for eight hours. The step response of the power supply showed no overshoot from 0 to 200A of the full output capability.

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