OPTIMISATION OF A HIGH-RESOLUTION, LOW-LATENCY STRIPLINE BEAM POSITION MONITOR SYSTEM FOR USE IN INTRA-TRAIN FEEDBACK

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Abstract

A high-resolution, low-latency beam position monitor (BPM) system has been developed for use in feedback systems at particle accelerators and beamlines that operate with trains of particle bunches with bunch separations as low as several tens of nanoseconds, such as future linear electron-positron colliders and free-electron lasers. The system was tested with electron beams in the extraction line of the Accelerator Test Facility at the High Energy Accelerator Research Organization (KEK) in Japan. The fast analogue front-end signal processor is based on a single-stage RF down-mixer, with a measured latency of 15.6 ± 0.1 ns. The processor has been optimised, doubling the maximum operating beam intensity up to 1.6 nC, and the signal processing in the custom digital acquisition board has been upgraded in order to improve the resolution beyond the 300 nm level measured previously. The latest results, demonstrating a position resolution of order 150 nm with single-pass beam, will be presented.

INTRODUCTION

The designs for the International Linear Collider (ILC) [1] and the Compact Linear Collider (CLIC) [2] require beams stable at the nanometre level at the interaction point (IP). In support of this, the goal of the ATF2 collaboration based at KEK, Japan is to achieve position stability at the IP of approximately 2 nm. To this end, the Feedback On Nanosecond Timescales (FONT) project [3] operates a position and angle feedback system in the extraction line of the Accelerator Test Facility (ATF2) [4] (Fig. 1). In order to achieve the required level of position stability at the IP, the FONT feedback system needs to stabilise the beam to below 1 μm at the entrance to the final focus system; this requires a BPM processing scheme capable of delivering position signals accurate to the sub-micron level on a timescale of the order of 10 ns.

The FONT beam position monitoring system makes use of three 12 cm stripline BPMs (P1, P2 and P3), which are located in the diagnostics section of the ATF2 extraction line, and a witness stripline BPM (MFB1FF) located ~30 m downstream. A further triplet of cavity BPMs (IPA, IPB and IPC) is located around the ATF IP (Fig. 2); the details of this cavity BPM system are described in [6].

The stripline BPMs are connected to specially developed analogue processing electronics [7] in order to deliver appropriate position signals to a custom digital board [8] that digitises the signals and returns the sampled data to a computer where they are logged. In 2015, the BPM system achieved a resolution of ~300 nm at a bunch intensity of ~0.5 × 10^{10} electrons/bunch [7]. This paper presents the improvements made to the BPM processor and the digital board in order to increase the maximum operating bunch intensity and improve the BPM resolution.

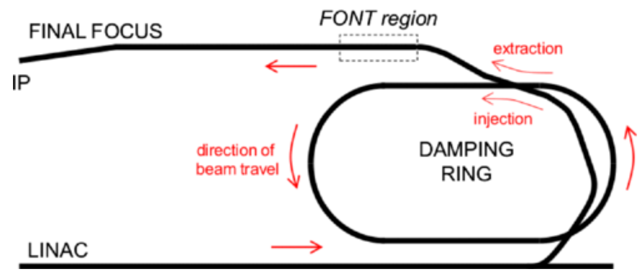

Figure 1: Layout of the ATF, showing the locations of the ATF2 extraction line and the FONT position and angle feedback system system.

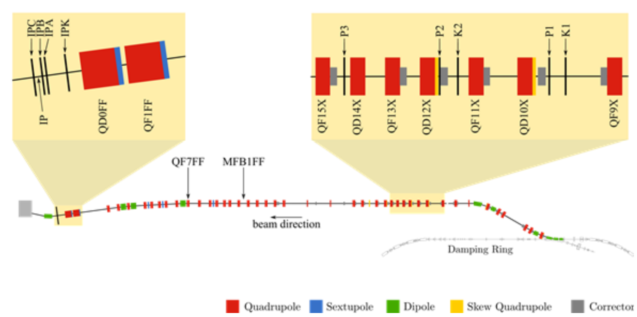

Figure 2: Layout [5] of the ATF2 extraction and final focus beamline with the FONT regions zoomed in.

BPM PROCESSOR DESIGN

A schematic of the processor module is shown in Fig. 3. The operation is as follows: the top (V_T) and bottom (V_B) stripline BPM signals are subtracted using a 180° hybrid to form a difference (Δ) signal and are added using a resistive coupler to form a sum signal. The resulting signals are then band-pass filtered and down-mixed with a 714 MHz local oscillator (LO) signal phase-locked to the beam before being low-pass filtered and amplified using 16 dB low-noise amplifiers. The hybrid, filters, and mixer were selected to have latencies of the order of a few nanoseconds in order to yield a total processor latency of 10 ns [7].

The phasing of the LO signal with respect to the beam signal is maintained using an adjustable phase shifter on the LO input to the processor. In the sum channel, a 90°

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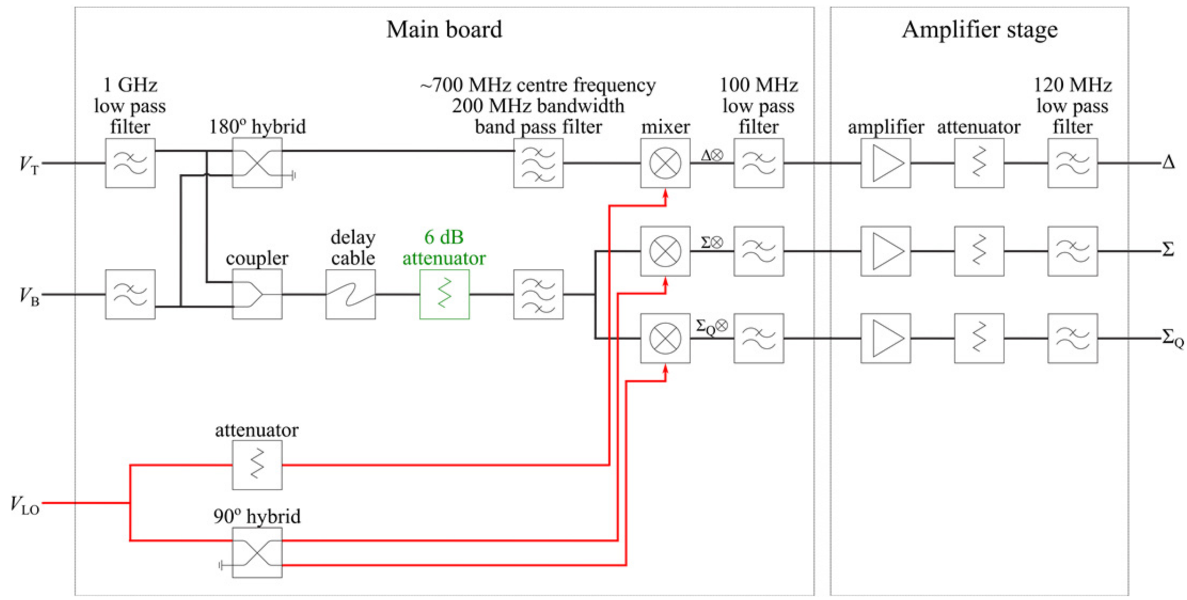

Figure 3: Schematic diagram illustrating the structure of the analogue processor, with the LO signal distribution in red and the additional 6 dB attenuator in green.

hybrid is used to downmix the raw sum signal with two orthogonal phases of the LO, producing an in-phase sum signal (Σ) and quadrature-phase sum signal (Σ_Q). The phase of the difference channel is accurately matched to that of the in-phase sum signal via a custom loopback cable in the sum channel. Hence the optimal phasing of both the Δ and Σ signals is achieved by minimising the Σ_Q signal.

The three output signals (Δ, Σ and Σ_Q) are digitized using analogue-to-digital converters (ADCs) on the FONT5A digital board, capable of converting at up to 400 MHz with 14-bit resolution. Low-noise amplifiers, with a gain of 16 dB, built into the processor modules are used to boost the input levels to just above the digitiser noise floor, and hence maximise the dynamic range of the measurement system. The ADCs, and sampling logic of the FONT5A board's Field Programmable Gate Array (FPGA), are clocked in a system-synchronous mode at 357 MHz, this being a convenient frequency derived from the machine RF. The ADC clock may be delayed in increments of 70 ps to allow sampling at the exact time the bunch arrives. There are nine ADCs in total and so a single board is able to fully record the data from three BPMs.

In the 'difference-over-sum' processing scheme, the Δ signal is proportional to the product of the beam offset and the bunch charge, whilst the Σ signal is proportional to the bunch charge alone [7]. Thus, the beam offset y is proportional to Δ/Σ.

SYSTEM IMPROVEMENTS

The maximum operating bunch charge is set by the saturation threshold of the mixer for the Σ signal. The Δ signals are typically small as the BPM movers can be used to set $y \approx 0$. In order to increase the maximum operating charge from $\sim 0.5 \times 10^{10}$ to $\sim 1.0 \times 10^{10}$ electrons/bunch, without reducing the sensitivity of the Δ signal, a 6 dB attenuator was placed before the Σ mixer (Fig. 3).

In addition, originally, a phase-locked loop (PLL) was used as a timing jitter filter on the incoming 357 MHz FPGA clock [8]. It was found that a combination of removing the PLL and introducing 360 ± 5 MHz band pass filters on the ADC sampling clock reduced the ADC sampling jitter.

BPM RESOLUTION

The BPM resolution was determined for the system comprising P1, P2 and P3 (Fig. 4). The previous best resolution of ~ 300 nm at $\sim 0.5 \times 10^{10}$ electrons/bunch has been reduced to a resolution of 157 ± 8 nm at $\sim 0.8 \times 10^{10}$ electrons/bunch.

FEEDBACK PERFORMACE

Two stripline BPMs (P2 and P3) have been used to drive a pair of kickers (K1 and K2) local to the BPMs (Fig. 5) and nominally orthogonal in betatron phase, to form a two-phase closed-loop feedback system to stabilise the position and angle of the beam at the entrance to the final focus [9].

For these demonstrations, a beam consisting of two bunches separated by 182 ns was used. The feedback tests therefore involve measuring the vertical position of bunch one and correcting the vertical position of bunch two. The system was typically operated in an 'interleaved' mode, whereby the feedback correction was toggled on and off on alternate machine pulses; the feedback 'off' pulses thereby provide a continual 'pedestal' measure of the uncorrected beam position. The feedback correction of the beam was witnessed at MFB1FF and at IPC. In the

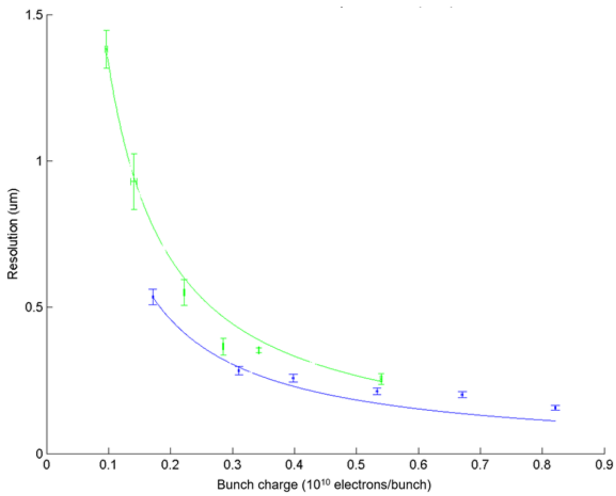

Figure 4: BPM resolution versus bunch charge q. Previous results are shown in green [7]; new results are shown in blue. The lines show the expected $1/q$ scaling taking the lowest-charge point in each case.

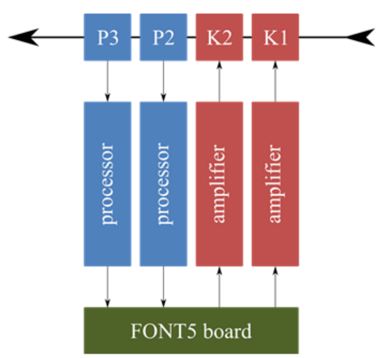

Figure 5: Block diagram of the feedback system.

configuration used, the beam waist is located downstream of IPC.

The result of the feedback operation as measured at P2, P3, MFB1FF and IPC is shown in Fig. 6. The position jitter is reduced by a factor ~3 at P2, and by a factor ~6 at P3. As a result of having approximately the same betatron phase as P2, a factor ~3 reduction in jitter is also observed at MFB1FF and IPC.

The bunch 2 position versus bunch 1 position for this data set is shown Fig. 7. The feedback removes the correlated component between the bunches, reducing the bunch-to-bunch position correlation from nearly 100 % to approximately zero.

The results at P2 and P3 have been propagated using vertical position and angle (y, y') transfer matrices through the ATF2 line to the beam waist in the IP region, assuming no jitter sources between P2 and the IP. A 0.19 mm difference in the longitudinal location of the waist is observed depending on whether the feedback is on or off. In this model, the jitter on waist is 6.1 ± 0.4 nm with the feedback off. The feedback stabilises the jitter on waist to 1.3 ± 0.1 nm, meeting the ATF beam stability goal.

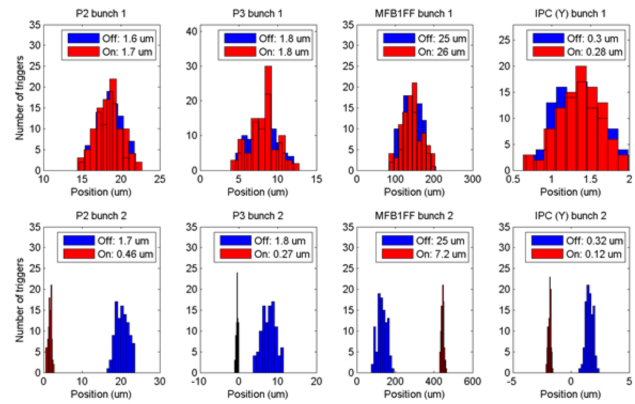

Figure 6: Distribution of the vertical position of bunches 1 and 2 in P2, P3, MFB1FF and IPC with (red) and without (blue) application of the feedback correction. Values of the position jitter are quoted for each BPM.

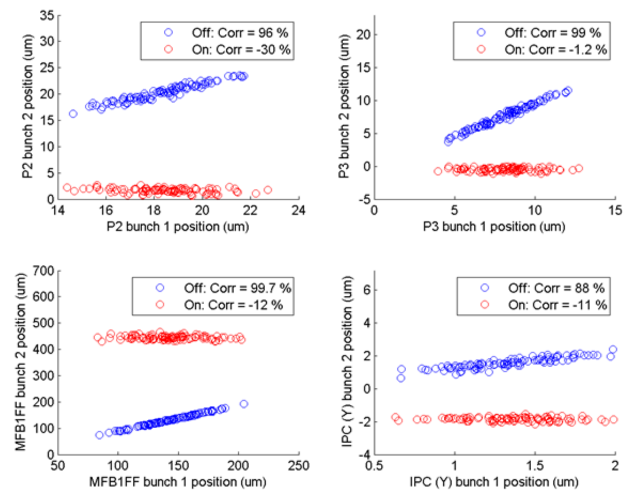

Figure 7: Bunch 2 position vs. bunch 1 position in P2, P3, MFB1FF and IPC with (red) and without (blue) application of the feedback correction. Values of the bunch-to-bunch position correlation are quoted for each BPM.

CONCLUSIONS

A stripline BPM system has been developed and optimised in the ATF2 extraction line, achieving a resolution of 157 ± 8 nm at a bunch charge of $\sim 0.8 \times 10^{10}$ electrons/bunch. Two such stripline BPMs have been used, together with two kickers, to operate a coupled-loop feedback system that can stabilise both the position and angle of the beam. Vertical beam stabilisation has been achieved to below the 300 nm level locally at one of the feedback BPMs, and the propagation of the correction has been confirmed using witness stripline and cavity BPMs downstream. Propagation of the results using a linear transfer model shows that the feedback stabilises the beam jitter to 1.3 ± 0.1 nm at the beam waist of the ATF2 final focus system, meeting the ATF beam stability goal.

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