DESIGN OF NEW SPECTRUM DATA ACQUISITION SYSTEM *

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Abstract

To solve the problem of spectrum acquisition in LIBS (Laser-Induced Breakdown Spectroscopy), a real-time data acquisition system was designed based on PSoC (Programmable System-On-Chip). First, the linear array CCD with electronic shutter function TCD1304DG has been used as detector .And then, the AD7621, a 16-bit analog-to-digital converter, was used to convert signal from the AFE (Analog Front End). After that, a high-integrated, low-power PSoC5LP was used as core controller, it works to complete the driver and data communication, including CCD, ADC, FIFO, the USB interface, etc. At last, a WIFI module has been added to the system for the convenience of users as well as follow-up research. The result through board-level testing indicates that the system in the spectrum acquisition is stable and accurate, and the indicators meet the LIBS project requirements.

INTRODUCTION

LIBS has become a very popular analytical method in the last decade in view of some of its unique features such as applicability to any type of sample , practically no sample preparation, remote sensing capability, and speed of analysis. The Laser-Induced Breakdown Spectroscopy system is shown in Fig. 1[1-3].

Under these circumstances, people put forward on higher requirements on the collection speed, accuracy, and stability of the spectral acquisition system [4]. The Charge-Coupled Device, CCD, also known as an image sensor, has been applied in astronomy, imaging, medicine and other fields. Design of the CCD imaging circuit mainly focus on the amplification of the output analog signal, and the A / D conversion. This involves a lot of knowledge of analog and digital mixing. PSoC can solve this problem very well.

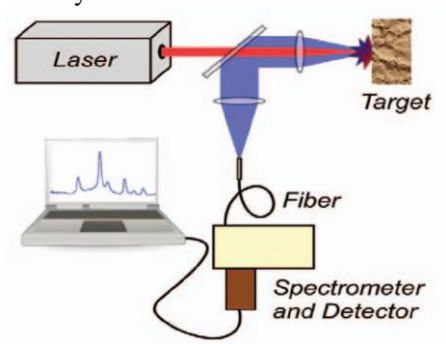

Figure 1: Structure of LIBS system .

INTRODUCTION TO PSOC-5LP

PSoC-5LP is a true programmable embedded system-on-chip, integrating configurable analog and digital peripherals, memory, and a microcontroller on a single chip. The PSoC-5LP architecture boosts performance through: 1.32-bit ARM Cortex-M3 core plus DMA controller and digital filter processor, at up to 80 MHz. 2. Ultra low power with industry's widest voltage range. 3. Programmable digital and analog peripherals enable custom functions. 4. Flexible routing of any analog or digital peripheral function to any pin.

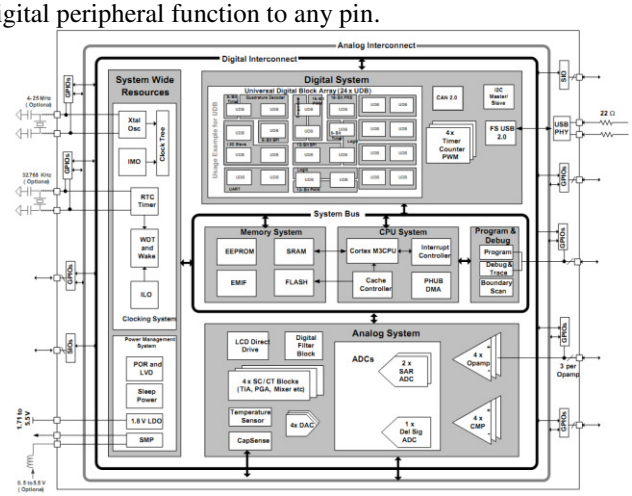

Figure 2: Simplified diagram of PSoC-5LP .

Figure 2 shows the diagram of the PsoC-5LP. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications[5].

SYSTEM OVERALL FRAMEWORK AND DEVICE SELECTION

In our design, the PSOC is the core control module, using its timer to generate the drive timing of CCD. The analog signal output by the CCD is very weak and contains noise, so we need to add some pre-amplification circuit and noise cancellation circuit. After the optimization, the electrical signal can be directly into our A/D converter for sampling. Data obtained from the ADC are not necessary to upload through the CPU, DMA can handle that. USB provides the interface for system and PC communication so that we can see the spectral data on the screen. Figure 3 shows the system framework.

* Supported by the National Key Scientific Instrument and Equipment Development Projects (No.2014YQ120351).

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ISBN 978-3-95450-182-3

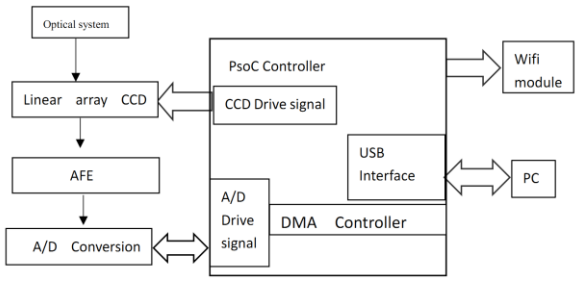


Figure 3: System overall framework.

The TCD1304DG is a high sensitive and low dark current 3648 −elements linear image sensor[6]. The sensor can be used for POS scanner. Electronic shutter function can keep always output voltage constant that vary with intensity of lights. Register imbalance is defined as follows:

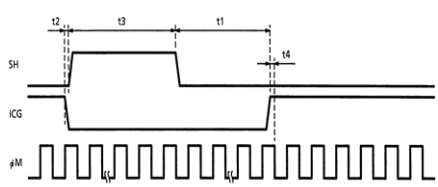
$$RI = \frac{\sum_{n=1}^{3647} \left| x^{n} - x^{n+1} \right|}{3647 \cdot \bar{x}} \times 100\% \qquad (1)$$

Where x^{n} and x^{n+1} are signal outputs of each pixel. $\bar{x}$ is average of total signal outputs. Table 1 shows the characteristic parameters of the CCD.

Table 1: Characteristic parameter of TCD1304

Voltage	Pixel Number	Spectral range	Master Clock Frequency	Data Rate
0.3~7V	3648	200-1100nm	2MHz	0.5MHz

Since we want the integration time to be adjustable, we need to use PSoC to control the timing. According to the timing diagram provided in the device manual, we divide the 80MHz system clock into different frequency by the PWM function from the PsoC. The period of the transfer gate pulse SH is the optical integration time of the linear array CCD. When the clearing gate pulse ICG from low to high, the image signal will output driven by the main clock φM. The reference value for delay is shown in Figure 4:



CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
ICG Pulse DELAY	t1	1000	5000	—	ns
Pulse Timing of ICG and S H	t2	100	500	1000	ns
SH Pulse Width	t3	1000	—	—	ns
Pulse Timing of ICG and φ M	t4	0	20	*	ns

Figure 4: Timing requirements of TCD1304 ·

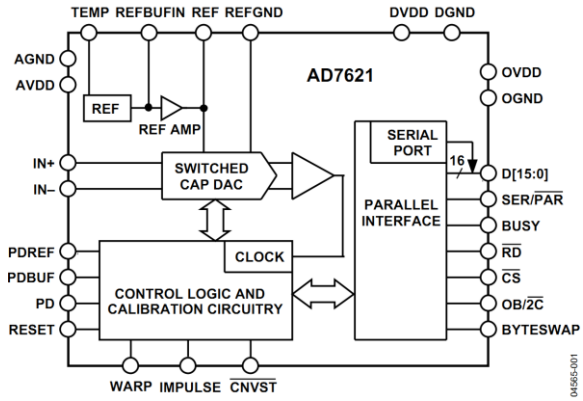


Figure 5: Framework of AD7621.

The AD7621 is a 16-bit, 3 MSPS, charge redistribution SAR, fully differential analog-to-digital converter (ADC) that operates from a single 2.5 V power supply. It contains a high speed 16-bit sampling ADC, an internal conversion clock, an internal reference (and buffer), error correction circuits, and both serial and parallel system interface ports. It features two very high sampling rate modes (wideband warp and warp), a fast mode (normal) for asynchronous rate applications, and a reduced power mode (impulse) for low power applications where the power is scaled with the throughput. Because there is no programmable gain and DAC inside the AD7621, we need to configure the external DAC to adjust the OS signal. We chose LTC2641,and let the difference input to ADC. The analog input of AD7621 is a true differential structure. By using this differential input, small signals common to both inputs are rejected. It's function diagram is shown in Fig.6.

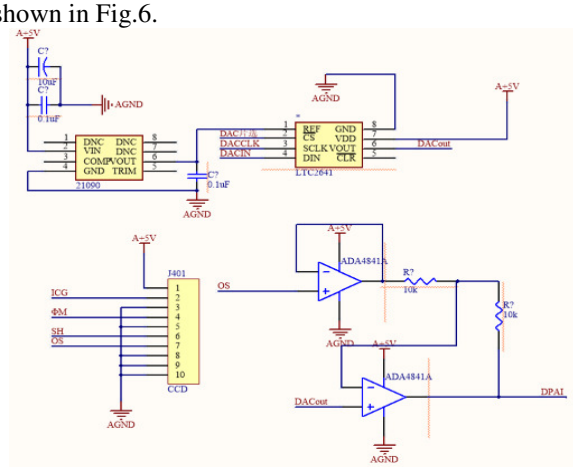


Figure 6: Differential input using DAC.

Power module is also need to carefully consider in our system. USB is a 5V input, but the voltage is not very well and the output power is not enough. So we use an external 5V power supply to drive CCD and WIFI module specifically. First we use the SX1308 to raise the input voltage, and then use a low dropout linear regulator LT1962 to stabilize the output voltage at 5V.

DATA TRANSMISSION

The DMA controller (DMAC) in PsoC-5LP can transfer data from a source to a destination with no CPU intervention. This allows the CPU to handle other tasks while the DMA does data transfers, thereby achieving a 'multiprocessing' environment. The PsoC DMAC is highly flexible – it can seamlessly transfer data between memory and on chip peripherals including ADCs, DACs, Filter, USB, UART, and SPI. There are 24 independent DMA channels.

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins. In order to process the imaging, we must transfer the data collected in real time to the host computer. After a frame of data collection of CCD, write data to the FIFO in the USB. The software part is not much to say.

We designed and made the PCB board, welded electronic chips and components and eventually made the actual circuit board, shown in Fig. 7.

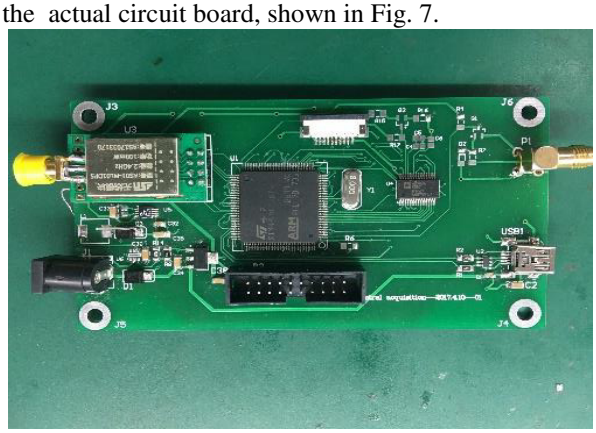


Figure 7: Actual circuit board.

TEST RESULTS

Test results will be affected by many factors. In order to verify the ability of the circuit system to adapt in different environments, we test the reliability of the system. The drive pulse is the most critical signal. Fig.8 shows the SH and ICG timing relationships that we produced.

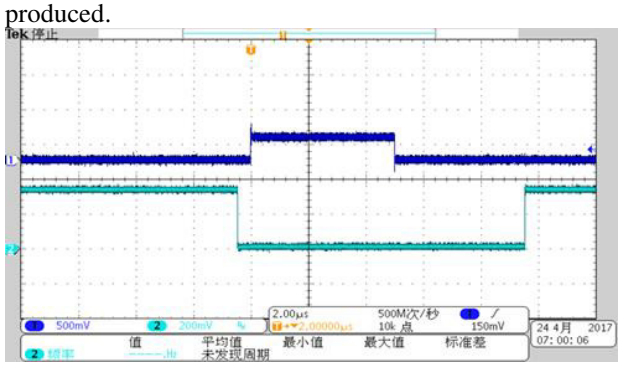


Figure 8: Timing relationships between SH and ICG.

The result shows that SH rising edge and ICG falling edge have a 500ns delay. And the cycle reached 7.388ms, achieved requirements of a long time exposure. The high duration of SH selects a value of 5000ns. ICG's low duration then lasts to a typical value of 10us. The result through board-level testing indicates that the system in the spectrum acquisition is stable and accurate, and the indicators meet the LIBS project requirements.

CONCLUSION

In this paper, a new spectral data acquisition system based on PSoC and linear array CCD is designed. And to achieve a low power consumption, portable, high integration characteristics. The design of the pre-processing circuit optimizes the signal noise. 80MHz operating frequency can solve the 20ns delay requirements. The differential circuit also improves the system's anti-jamming capability. The addition of the WIFI module provides the basis for subsequent work. So it has a certain practical value and industrial application prospects.

REFERENCES

[1] J. B. Sirven, B. Bousquet, L. Canioni, L. Sarger, S. Tellier,M. Potin-Gautier, and I. Le-Hecho, Anal. Bioanal. Chem.,2006, 385(2): 256.

[2] F. H. Kortanbruck, R. Noll, P. Wintjens, H. Falk, and C.Becker, Spectrochim. Acta B, 2001, 56: 933.

[3] Song, K.; Lee, Y.I.; Sneddon, J. Application of laser-induced break down spectrometry. Appl. Spectrosc. Rev. 1997, 32 (3), 183 – 235.

[4] LI Gang, WANG Yan, LIN Ling, et al. Life Science Instruments, 2004, 2(5):33.

[5] S.Goldman, P. L. White, and N.C Anheier. Planar waveguide spectrometer. SPIE Optoelectron Devices and Appl, 1990, 1338: 64-68.

[6] Toshiba Corporation. TCD1304DG Datasheet. http://www.spectronicdevices.com/pdf/TCD1304DG.pdf

ISBN 978-3-95450-182-3