TIMING SYSTEM AT ESS

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Abstract

The European Spallation Source (ESS) is a research facility being built in Lund (Sweden) that will produce neutrons by the spallation process. It uses the Micro-Research Finland (MRF) Timing System, which provides a complete event-based timing distribution system. The timing signal generation consists of a basic topology: an Event Generator (EVG), an optical distribution layer (fan-out modules) and an array of Event Receivers (EVRs).
The timing system will provide clock synchronization and timing services to devices with real time requirements. Its main purposes are event generation and distribution, time stamping and synchronous data transmission.
The event clock frequency will be 88.0525 MHz, divided down from the bunch frequency of 352.21 MHz. An integer number of ticks of this clock will define the beam macropulse full length, around 2.86 ms, with a repetition rate of 14 Hz. ESS will be the first facility to deploy large amounts of uTCA EVRs, and is planning to take advantage of the features provided by the uTCA standard, like trigger and clock distribution over the backplane. These EVRs are already being deployed in some systems and test stands.

INTRODUCTION

ESS [1] will be the leading facility in Europe in neutron science. It works by colliding proton beam pulses with a tungsten target to produce neutrons by the spallation process, which are led through beamlines to the scientific instruments. In normal operation the proton beam pulses, up to 2.86 ms long, are generated with a frequency of 14 Hz. The timing system allows the synchronisation of the distributed control system and the components of the facility with the beam operating cycle [2]. In order to achieve that, the timing system broadcasts trigger events, time stamps, beam-related parameter and clock signals across the facility with a deterministic latency.

TIMING SYSTEM FUNCTIONS

- Trigger event distribution: Trigger events define the accelerator sequence timeline. EVRs act based on these triggers, by driving outputs high and low, or triggering them with user-defined width, delay and polarity.
- Data distribution: Beam-related information for each pulse is broadcasted before the actual pulse is emitted. Devices can prepare for each individual pulse, and even raise a flag if they are not ready for it.
- Timestamping: A timestamping mechanism distributes a common "wall-clock" time to the whole facility. This time is used for timestamping events and actions, and is derived from GPS. It is incremented internally but periodically re-synchronised with GPS to avoid drifting too far away from the GPS-defined time.
- Distribution of clock signals: Up to 8 RF-synchronous clock signals can be distributed globally or created for an individual EVR. They are sampled at half the event clock frequency.
- Delay compensation: An active delay compensation mechanism provides stability against long term drifts caused mainly by thermal changes.

IMPLEMENTATION

The ESS timing system is event based, with an EVG at the top of a tree-like structure also comprising EVRs and fan-out modules (FOUT). The EVG generates a bitstream containing timing events, data and synchronous clocks that is sent over an optical link to the FOUTs. They multiply the bitstream and send it to other FOUTs and EVRs. The EVRs receive the events, data and clocks, decode them and perform the necessary actions. The EVG derives the event and data frames frequency (of approximately 88 MHz) from the RF master oscillator. Figure 1 shows the timing distribution system.

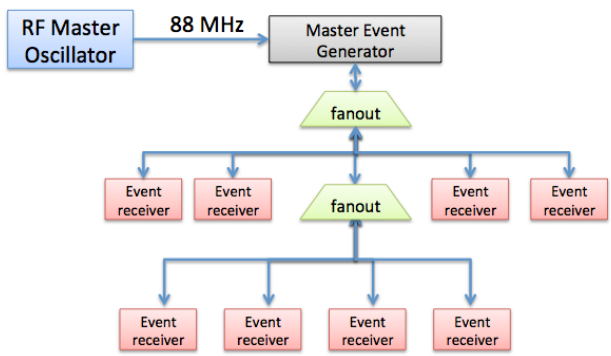

Figure 1: Timing distribution structure.

The EVG has event two sequencers that transmit sequences of events stored in memory in the form of lists of event-mask-timestamp triplet. The timestamp is stored in event clock ticks since the start of the sequence. At any time one of the sequencers is in use while the other one can be manipulated.
The EVG has multiplexed counters used to trigger the sequencers and to send periodic events at an (almost)

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ISBN 978-3-95450-182-3

arbitrary frequency to the array of EVRs. The EVG uses special events to send and synchronize the timestamp across the facility.
In each event clock cycle the EVG sends an event and, either a frame of a data block, or a distributed bus with 8 simultaneous clock signals (they are intercalated every other cycle). The data is stored in the memory of the EVG and broadcasted to the EVRs. The distributed bus is sampled with half the event clock frequency of approximately 88 MHz. Figure 2 shows the structure of the event clock cycles in the timing system bit stream.

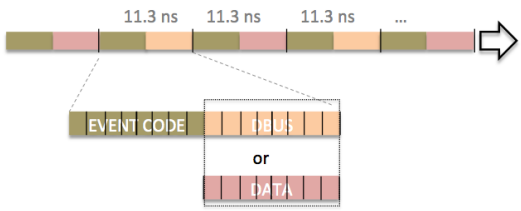

Figure 2: Frame structure of the timing system bit stream.

The EVRs main purpose is generating output triggers based on the timing events, distributed bus signals or internal prescalers. Delay, width and polarity of the trigger is controlled by software. Special outputs provide low jitter signals that can be used for clock generation or arbitrary pattern generation (following certain rules).
The EVRs receive the timestamp from the EVG and allow attaching a timestamp, synchronized with the rest of the facility, to the collected data and performed actions. In between timestamp events received from the EVG, the EVR keeps track of the time internally.
EVRs have a 2 kB memory area reserved for data buffer reception from the EVG, which is accessible in the EPICS IOC (more about this in the *EPICS INTEGRATION* section). The EVRs can also create interrupts used by the CPU to trigger EPICS records to process, and with recent firmware updates they have also limited EVG functionality.

Currently ESS uses EVRs in MTCA.4 and PCIe form factors,and EVG and FOUT in the VME form factor. The VME-EVM-300 board version provided by Micro-Research Finland (MRF) [3] acts as EVG and FOUT, while the MTCA-EVR-300 and PCIe-EVR-300DC versions are used as EVRs.

MACHINE TIMELINE AND BEAM PARAMETERS

The frequency of operation of the ESS machine is 14 Hz, with some systems, such as the target wheel and RF systems, requiring constant operation at this frequency. Each machine cycle of 71.4 ms encompasses events used for things such as triggering RF systems, beam diagnostic devices and extracting beam from the proton source. Figure 3 shows a preliminary machine timeline.

For the correct operation of the machine, some parameters of the proton beam need to be known by some devices before the arrival of the beam. This information is transmitted across the facility by the timing system. The parameters for a specific beam cycle are broadcasted during the previous cycle, so that all the control system devices have time to perform the necessary actions. Table 1 shows a preliminary list of the data to the broadcasted. Exact layout of the data is yet to be defined.

Table 1: Preliminary list of beam data distributed my the timing system.

Data item	Unit	Format
Beam repetition rate	Hz	Integer (1-14)
Beam present	-	Boolean (0-no, 1-yes)
Accelerator mode	-	Enumerated integer
Beam envelope mode	-	Enumerated integer
Pulse length	ms	Float
Proton energy	MeV	Float
Raster pattern	-	Enumerated integer
Target segment	-	Integer

TECHNICAL DETAILS AND REQUIREMENTS

ESS generates proton beam pulses with a frequency of 14 Hz, and a maximum length of 2.86 ms. The ESS RF master clock, running at 352.21 MHz, is used used to generate the timing event clock with a frequency of 88.0525 MHz or around 11.357 ns period (the 4^{th} subharmonic of the RF master clock), so all operations of the timing system are phase-synchronous to the RF master clock. The timing event clock (6289464 ticks) is used to generate the 14 Hz beam frequency.

The following list summarises some of the requirements for the ESS timing system:

- The jitter of clock distributed by the timing system must not exceed 1 ns.
- It must be possible to configure timing receivers to generate actions on received timing events, with phase misalignment not greater than one timing clock period between two timing receivers.
- Granularity of time-stamps should be one timing clock period.
- Timing events, sequences, timestamping, alignment, etc. must be defined relatively to a 14 Hz repetition rate.

ISBN 978-3-95450-182-3

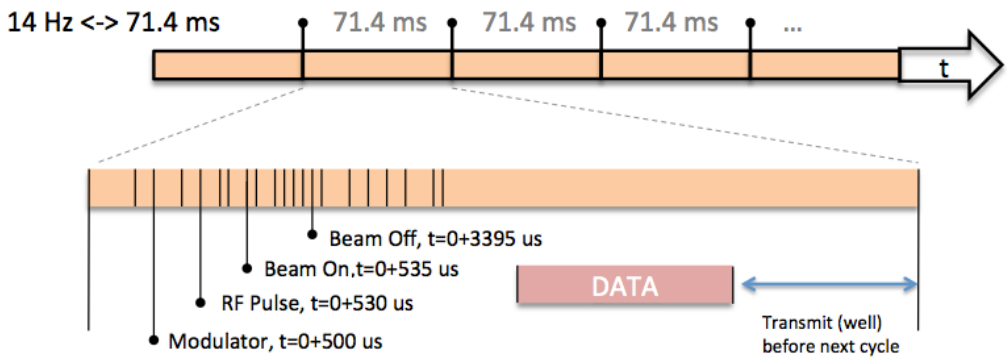

Figure 3: Machine timeline (conceptual).

- The EVG must transmit data over the real-time timing system network to EVRs without compromising determinism of timing sequence generation.
- Granularity for setting delay and width parameters of responses generated on hardware output interfaces must be configurable in steps of one timing clock period.
- EVR must only allow action configuration to specific timing events during its boot-up procedure where indicated timing events in the provided configuration must and cannot be changed during run-time.
- EVRs must be able to use and re-configure the hardware delay-width configuration for every trigger line if it changes during operation without compromising any currently generated actions.
- EVRs must switch to local clock source as a fallback in case of losing the signal from EVG.

EPICS INTEGRATION

ESS uses the Experimental Physics and Industrial Control System (EPICS) [4], which is a software environment used to create distributed soft real-time control systems for scientific instruments such as a particle accelerators, telescopes and other large scientific experiments. EPICS uses Input/Output Controllers (IOCs) for interfacing the real world. The configuration of the timing system components is done using EPICS variables, such as how EVRs respond to event codes, handling the data distribution or making the global timestamp available.

The EPICS integration is realised by the *mrfioc2* driver, developed and widely used by the EPICS community, and which provides access to the whole functionality of the EVG and EVR modules.

CONCLUSION

This paper describes briefly the ESS timing system, including the implementation, functionalities and some technical details. All the details of the final design are not yet defined, but rather a glimpse of the system is described.

REFERENCES

[1] European Spallation Source ERIC website, `http://europeanspallationsource.se`

[2] T. Korhonen *et al.*, "Status of the European Spallation Source Control System", in *Proc. 15th Int. Conf. on Accelerator and Large Experimental Physics Control Systems (ICALEPCS'15)*, Melbourne, Australia, Oct. 2015, paper FRB3O02, pp. 1177–1181, `http://jacow.org/icalepcs2015/papers/frb3o02.pdf`, `doi:10.18429/JACoW-ICALEPCS2015-FRB3O02`, 2015.

[3] Micro-Research Finland website, `http://www.mrf.fi`

[4] Experimental Physcics and Industrial Control System website, `http://www.aps.anl.gov/epics/`