DIGITAL LOW LEVEL RF CONTROL SYSTEM FOR THE TAIWAN PHOTON SOURCE

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Abstract

The Taiwan Photon Source (TPS) is a 3 GeV, 500 mA, 499.65 MHz, 3rd generation synchrotron light source at NSRRC. To achieve the requirements of system flexibility, fault diagnosis, precise control and high noise reduction, a digital low level RF (DLLRF) control system based on Field Programmable Gate Array (FPGA) was developed. The communication interface is based on Raspberry Pi. The feedback loop performance of the control system was tested on the booster of the Taiwan Photon Source (TPS) with 950 kV gap voltage.

INTRODUCTION

After completion of the TPS commissioning in 2016, the beam lines are open for user operation with 300 mA beam current at 3 GeV while the final goal is to provide 500 mA beam current. The original LLRF system at TPS may become unstable by the Robinson instability while operating under heavy beam loading, which is one of the most critical issue to maximize the mean time between failures of the SRF [1]. Especially, cross-talk between RF components is an unavoidable problem. The anti-noise capability of the LLRF system is the key and plays an important role for improving the stability of the SRF. The LLRF control system for the TPS is still based on an analog system [2] and there is room to improve the 60Hz noise and its harmonics by developing a DLLRF system.

The LLRF system at NSRRC contains a cavity phase loop, a cavity amplitude loop, a klystron phase loop, and a tuner loop to control the SRF cavities [2]. In this article, an alternative DLLRF system is discussed which integrates the functions of cavity phase loop, klystron phase loop, and cavity amplitude loop into a FPGA control core. The noise suppression capability was tested at the TPS booster and compared with the current analog system.

DLLRF ARCHITECTURE

Process Flow of the DLLRF

The schematic of the DLLRF controller is shown in Fig. 1 where the master clock in the Front End creates a 550 MHz local signal (Lo) for the Up/Down converter of the controller and an 80 MHz LVTTL signal to be the working clock for the FPGA. The master clock connects with the DLLRF controller as an IQ sampling reference. The cavity (P_t) and master signals are down converted to IF band (50 MHz) by mixing a 500 MHz RF signal with a 550 MHz Lo signal. Then, these IF band signals are digitised by an ADC with a 40 MHz clock generated by a FPGA PLL from the 80 MHz working clock. After data processing by the FPGA functions, a signal for cavity control (Ptx) is generated by a DAC with the 80 MHz working clock and then up converted to a 500 MHz RF signal. The principle of data sampling and data output follows the study reported by H. Ma et al. in 2009 [3].
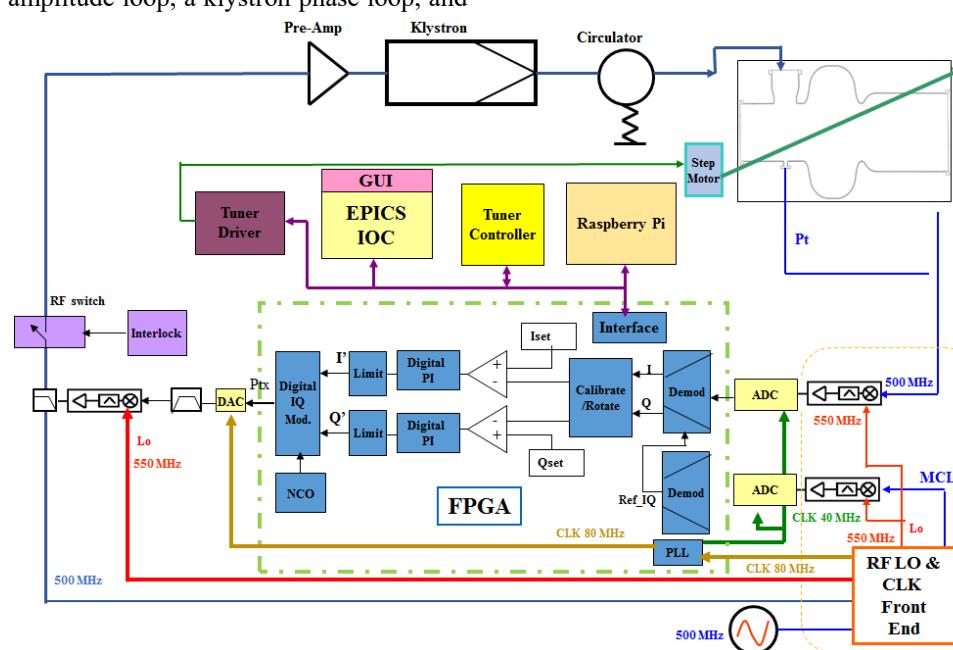
Figure 1: Schematic of the DLLRF controller..

Functions of the DLLRF

The DLLRF functions are controlled by machine status modes including Off Mode, Tune Mode, and Operational Mode. Off Mode means the drive power to the RF transmitter (I_{out}=0 and Q_{out}=0) is turned off. In the Tune Mode a limited drive power is provided for the tuner to lock on to the resonance frequency. I_{out} and Q_{out} are directly set up by the Raspberry Pi [4]. In the Operational Mode the RF system is ready for high power and for beam current. The feedback by the PI controller is turned on to determine I_{out} and Q_{out} and to keep I_{ro} and Q_{ro} the same as I_{set} and Q_{set}. When applied to the booster, the operational electric field may not be a continuing wave but rather a ramping wave for which a ramping Table is prepared. The flow chart of the machine state is shown in the upper right corner of Fig. 2. The Reset and Off Mode command invoke the state Off Mode. There is a 30 sec lock time for the tuner to lock to the frequency when the state changes from Off Mode to Tune Mode. The state only can go into Operational Mode from the Tune Mode. The detailed algorithm for the machine state is shown in Fig. 3.
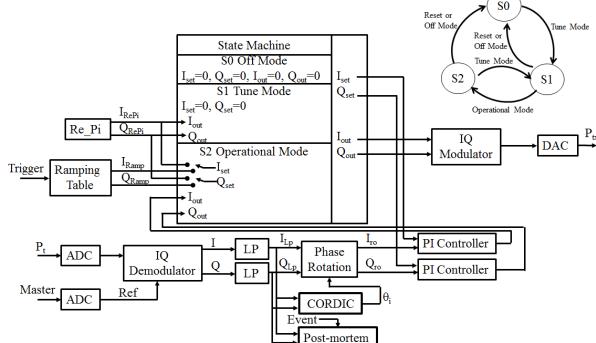
Figure 2: Function block scheme for the FPGA core and flow chart for the machine status.

The function block of the FPGA core is represented in Fig. 2. The Pt signal is demodulated in terms of I and Q defined by Eq. (1) [5].

$$I = \frac{2}{N}\sum_{i=0}^{N-1} y_i \sin(i \cdot \Delta\varphi), Q = \frac{2}{N}\sum_{i=0}^{N-1} y_i \cos(i \cdot \Delta\varphi) \quad (1)$$

where $f_s = \frac{N}{M} f_{IF}$, $\Delta\varphi = 2\pi\frac{M}{N}$, and I is an integer. In the case described here, N=4, M=5, f_s =40 MHz and f_{IF}=50 MHz while the sampling signal is listed as Q, I, -Q, -I, Q, I, …-I. LP is a FIR low pass filter to eliminate noise caused by fluctuations of the ADC and sampling clock. After filtering, the ILP and QLP are split into three parts including Phase Rotation, CORDIC, and Post-mortem. The Post-mortem function is used to record 1000 data of I_{ro}/Q_{ro} before and 3096 data after an event. This is useful for system diagnosis and observing the performance of the PI controller [4]. Phase Rotation is used to calibrate the angle error due to the whole system delay. The Calibrating angle (θ_i) is evaluated by CORDIC which works once at the first Tune Mode from a reset situation and then keeps the θ_i value, as shown in Fig. 3. After calibrating, the I_{ro}/Q_{ro} signal is fed to the PI controller and compared with the set points I_{set}/Q_{set} for feedback before

it is transmitted to the machine status. According to the operation mode, the machine state generates signals I_{out} and Q_{out} for the IQ Modulator, where the I/Q data are covered to amplitude signals by Eq. (2).

$$y = I_{out} \times \sin\omega t + Q_{out} \times \cos\omega t \quad (2)$$

where y is the amplitude signal for the klystron. The sine and cosine signals are perfectly synchronized and generated by a numerically controlled oscillator (NCO). The frequency of the NCO is chosen to be the same as the carrier (50 MHz). The amplitude signal processed by the IQ Modulator is still digital and needs to be transformed to analog form by a DAC. Finally, the analog amplitude signal (P_{tx}) is up converted to 500 MHz, and passes through a band pass filter to the klystron.
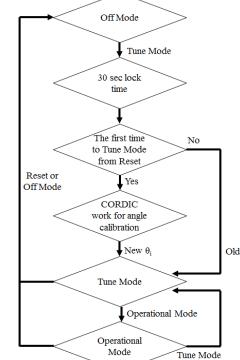

Figure 3: Algorithm for the machine state.

HARDWARE

The DLLRF control system includes a FPGA control core, a Raspberry Pi, an Up/Down converter, and a linear power source as shown in Fig. 4. The hardware of the FPGA control core consists of two kinds of commercially available cardboards. The Altera DE3-260 is a development platform carrying 260 k logic elements FPGA (Stratix III) while the DCC-HSMC is an AD/DA data conversion card based on the High Speed Mezzanine Card (HSMC). Both, ADC and DAC have 14-bit resolution and update rates are up to 150 MSPS for the ADC and 250 MSPS for the DAC. The DE3 can communicate with the DDC-HSMC and Raspberry Pi via a SFF connector and GPIO, respectively. The cavity RF signal is transformed form 500 MHz to 50 MHz by the Up/Down converter, digitised by the DDC-HSMC, processed by DE3, and then up converted back to 500 MHz for cavity control. The Raspberry Pi is used to create a graphical user interface written in Linux to control and monitor the DLLRF system [4].
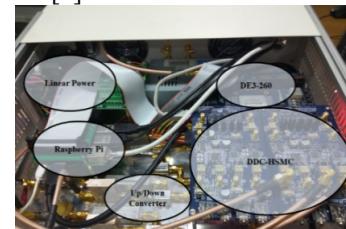

Figure 4: Physical assembly of the DLLRF control system.
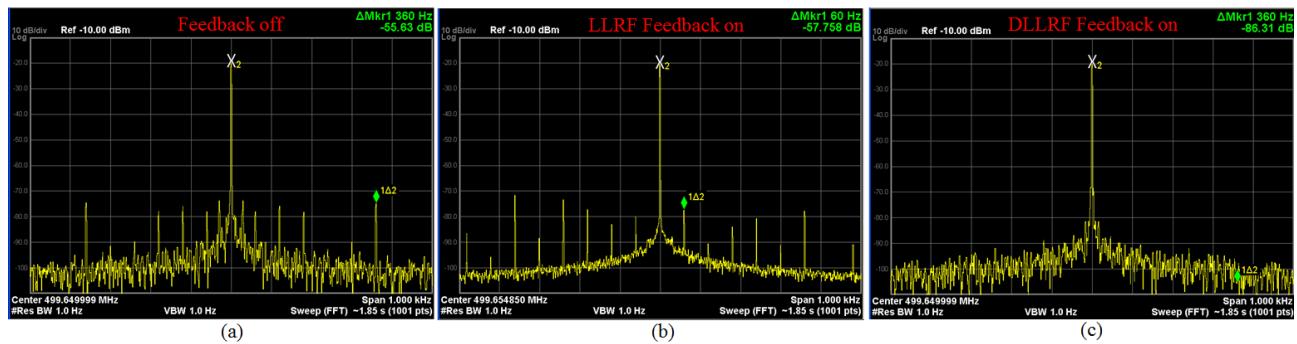
Figure 5: Cavity field spectra with (a) Feedback off, (b) LLRF Feedback on, and (c) DLLRF Feedback on.

RESULTS FROM TESTS IN THE TPS BOOSTER

The TPS booster includes a 500 MHz Petra Cavity with a 100 kW transmitter generating a cavity gap voltage of 950 kV. The DLLRF control system performance was tested there in January, 2017 and the testing results as measured by an Agilent Technologies EXA Signal Analyser are shown in Fig. 5. Figure 5(a) shows the cavity field spectrum when the feedback system is off and suffers from the interference with 60 Hz noise harmonics. The noise suppression capability of the original analog LLRF system at 60 Hz is insufficient as Fig. 5(b) shows. All analog components are driven by City Power, and it is difficult to get rid of the 60 Hz interference. In contrast, Fig. 5(c) exhibits almost perfect performance of the DLLRF system to depress the 60 Hz noise by over -70 dB compared with the central frequency

CONCLUSION

NSRRC developed a DLLRF control system and tested its performance at the TPS booster. The results show the DLLRF control system for the TPS to successfully supress the 60 Hz noise and its harmonics up to -70 dB compared with the central frequency. In addition, the digital system reduces the noise power by about 13 dB compared to the analog system.

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