DSP FRAME AND ALGORITHM OF LLRF OF IR-FEL*

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Abstract

Infrared Free Electron Laser (IR-FEL) use linear accelerator to accelerate electron to relative speed and then generate simulated radiation of infrared wavelength by periodic magnetic field of undulator. The amplitude and phase of microwave field need to be controlled precisely by low level RF control system (LLRF) to meet the high quality demand of electron from undulator. This paper mainly introduce the digital signal processing frame and feedback algorithm. Four times frequency sampling can realize IQ demodulation precisely and reduce DC offset, amplitude sampling error is less than 0.075% and phase sampling error is less than 0.1°. Pipeline CORDIC can calculate amplitude and phase by parallel processing and shift operation. Phase calculating accuracy reach 0.0005° when iteration count is 18. FIR filter is used to improve frequency selected performance. Feedback loop use digital PI controller to adjust system output.

DIGITAL SIGNAL PROCESSING FRAME

The LLRF system of IR-FEL has 8 channels input and 1 channel output. The SSA_IN signal is input for the controlled variable, the ACC_Refl is input for software interlock to protect power amplifier system which is the signal reflected from accelerating structure and other 6 input signals is used for monitoring the whole microwave system. The RF signal is controlled by feedback and feedforward algorithm and output for driving SSA [1].

Fig. 1 is the DSP frame of LLRF. Each input signal is sampled by ADC to generate I and Q digital signal. Amplitude and phase can be calculated from I and Q through CORDIC algorithm and storage in DDR3 which can be read by CPU through DMA (Direct Memory Access) but not need to interrupt FPGA.

In the feedback loop, digital I and Q signal need to be rotated by matrix to make sure the phase is in the range from -90° to +90° . The I_1/Q_1 signal is compared with the set value I_set/Q_set to generate the error variable I_E/Q_E and then the PI control algorithm can calculate the adjusting variable I_U/Q_U.

Feedforward module is used for reducing the feedback time and preventing greater adjusting vairable.VM Comp module is used for compensating the DC offset, the imbalance of amplitude and phase. VM module can modulate the analog I and Q signal with the reference signal [2].

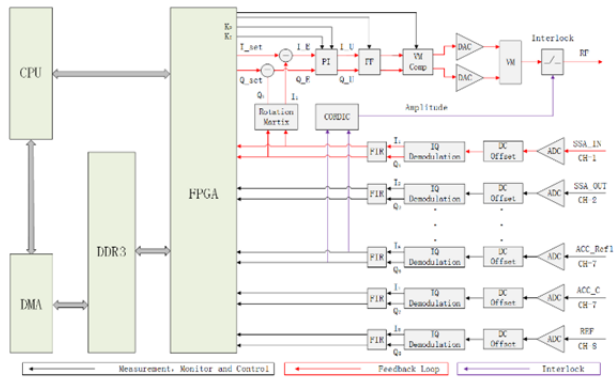

Figure 1: DSP Frame of LLRF of IR-FEL.

Interlock switch which is behind the VM module output is a kind of software interlock and it has advantages of set and recovery more easily and higher system integration. It is controlled by the amplitude of the signal reflected from the accelerating structure.

SAMPLING ALGORITHM

The target of LLRF is control the amplitude and phase of signal, but it will occupy huge hardware resource and lead to greater calculating delay if we control the amplitude and phase directly by digital device. IQ demodulation can generate the quadrature I and Q component of original signal which contain the information of amplitude and phase. The I/Q component can be adjusted by addition or subtraction easily.

Traditional IQ demodulation use analog device and have the problem of imbalance of amplitude and phase which is caused of DC offset and non-ideal quadrature. The IQ trace will be ellipse which deviate from original point but not perfect circle which is round at the original point [3].

We use 4 times frequency sampling algorithm to realize IQ modulation. The IF signal frequency is 26.44MHz and sampling frequency 105.76MHz which is need to be 4 times as sampled signal frequency precisely. Fig. 2 is the principle of 4 times frequency sampling.

$$
\begin{aligned}
S_S &= A\cos(\omega k T_S - \phi) \\
&= A\cos(\omega k \frac{4n+1}{4}T)\cos(\phi) + A\sin(\omega k \frac{4n+1}{4}T)\sin(\phi) \\
&= I\cos(\omega k \frac{4n+1}{4}T) + Q\sin(\omega k \frac{4n+1}{4}T) \\
&= I\cos(\omega k \frac{1}{4}T) + Q\sin(\omega k \frac{1}{4}T) \\
&= I\cos(\frac{\pi}{2}k) + Q\sin(\frac{\pi}{2}k) \\
&= I, Q, -I, -Q \quad (k = 0,1,2,3,.....)
\end{aligned}
\tag{2.1}
$$

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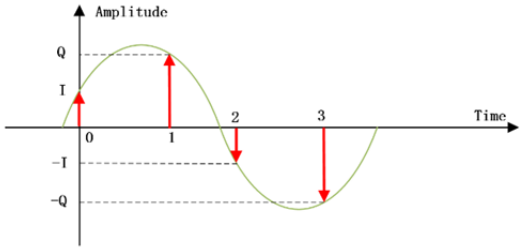


Figure 2: 4 times frequency sample.

See Fig. 3, I and Q signal will be output from one and the same ADC and can be separated by multiplexer.

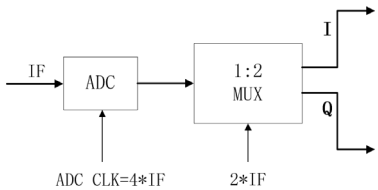


Figure 3: I and Q separate.

The RF board and ADC both have DC offset. This offset can be eliminated by the DC input on the RF board but it need to measure the offset in advance and can't be real time. A group of I, Q, -I and –Q data can generate I and Q data without offset.

$$\begin{cases} I_{DC} = \dfrac{S_S(4n+1)-S_S(4n+3)}{2} \\ Q_{DC} = \dfrac{S_S(4n+2)-S_S(4n+4)}{2} \end{cases} n = 0,1,2,3..... \quad (2.2)$$

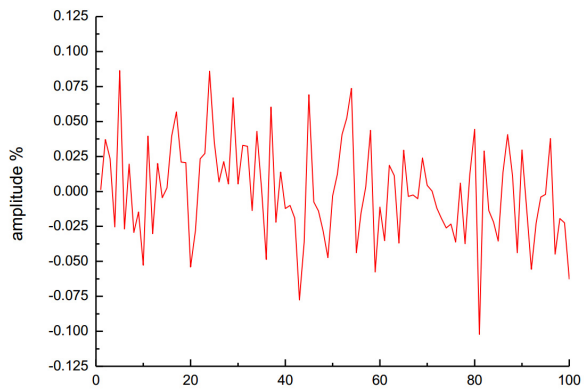


Figure 4: Error of amplitude sample.

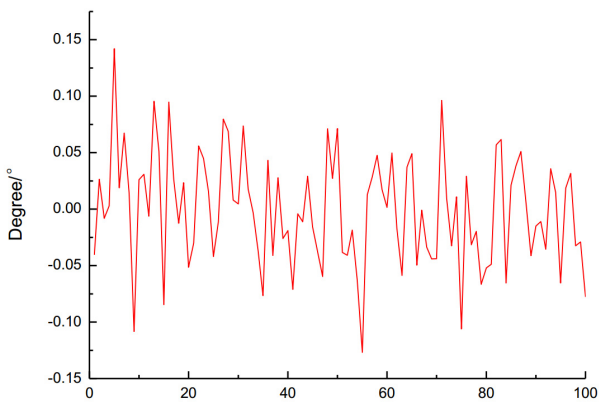


Figure 5: Error of phase sample.

Figure 4 and 5 is the offline measurement of ADC. The amplitude sampling error is almost in the range of ± 0.075% and the phase sampling error is almost in the range of ±0.1° .Considering the jitter of RF signal, the real errors will be less than above data.

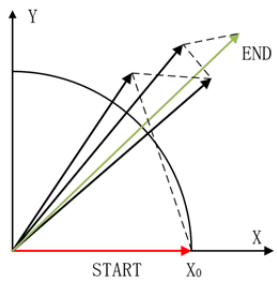
AMPLITUDE AND PHASE CALCULATION

Although the RF signal can be controlled by I and Q component, upper computer need to display the amplitude and phase, the adjusted target transmit from upper computer is also amplitude and phase. So FPGA need to realize the transition between I/Q and amplitude/phase which require calculating transcendental function. The traditional method is building a table of function value, but this method need huge memory space and calculating accuracy is low. CORDIC algorithm use iteration by rotating vector to calculate transcendental function. The d_i is defined as rotating direction and the Z_i is defined as degree accumulated value.

$$\begin{pmatrix} x_{i+1} \\ y_{i+1} \end{pmatrix} = \begin{pmatrix} 1 & -d_i 2^{-i} \\ d_i 2^{-i} & 1 \end{pmatrix} \begin{pmatrix} x_i \\ y_i \end{pmatrix} \quad (3.1)$$

$$Z_{i+1} = Z_i + d_i \theta_i \quad (3.2)$$

See Fig. 6 and 7, CORDIC have two work modes: rotating mode, convergence target is degree deviation being equal to zero; vector mode, convergence target is y component being equal to zero [4]. Table 1 is CORDIC function.



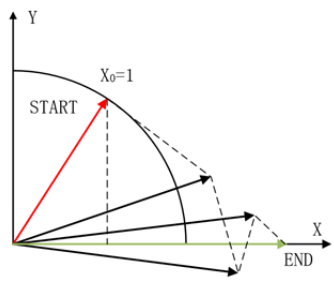


Figure 6: Rotating mode. Figure 7: Vector mode.

Table 1: CORDIC Function

	R=1.6468
$Z_i \to 0$	$\begin{cases} x_N = R(x_0 \cos Z_0 - y_0 \sin Z_0) \\ y_N = R(y_0 \cos Z_0 + x_0 \sin Z_0) \end{cases}$
$y_i \to 0$	$\begin{cases} x_N = R\sqrt{x_0^2 + y_0^2} \\ Z_N = Z_0 + \arctan(y_0 / x_0) \end{cases}$

We simulate the degree calculating error with different iteration count and shown by Fig. 8 and 9. Accuracy improvement is very small with iteration count improvement when the iteration count is more than 15. The degree calculating error is less than 0.05 % when the iteration count is 18.

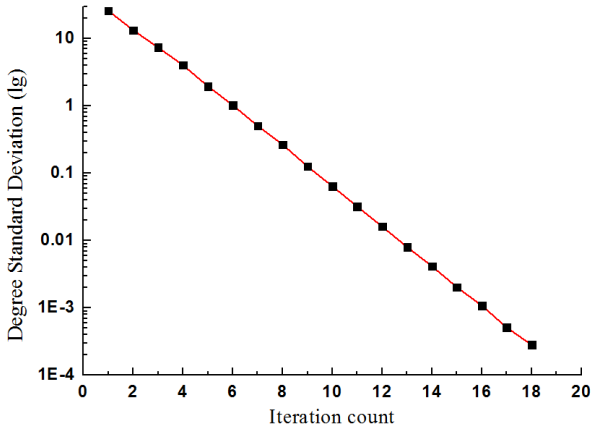


Figure 8: Degree SD (@ Iteration Count).

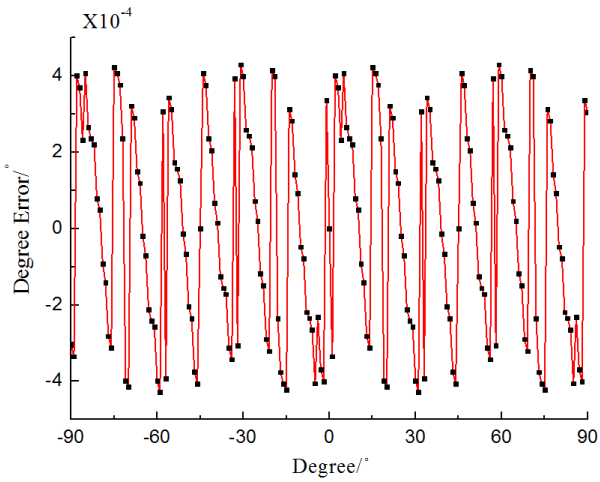


Figure 9: Degree error (iteration count is 18).

See Fig. 10, CORDIC can be realized by pipeline structure. Pipeline can improve calculating speed by parallel processing and use fixed depth shifter unit.

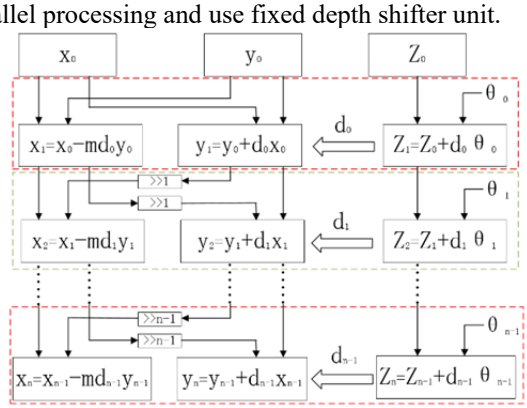


Figure 10: Pipeline CORDIC.

FIR FILTER

FIR filter can realize frequency selection through convolution. Symmetry and linear phase filter can reduce multiplication processing by half which define zeroth sampling point as impulse response center and make response function being pure real number or pure imaginary number. Fig. 11 is the structure of symmetry and linear phase filter.

$$y(n)=\sum_{k=0}^{(L-1)/2}\left[x(k)+x(L-1-k)\right]f(k) \qquad (4.1)$$

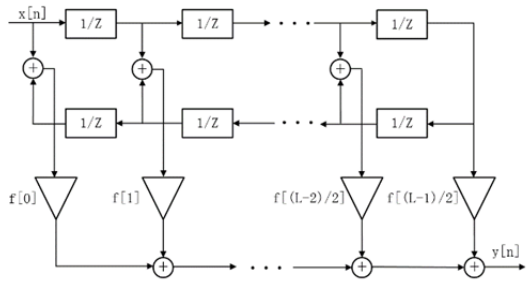


Figure 11: Symmetry and linear phase filter.

PI CONTROLLER

Feedback loop use proportion and integration controller to adjust output value. K_I and K_p coefficient are transmitted from upper computer to FPGA through PCIE [5]. See Fig. 12, delay module is used to synchronize the signal of proportion and integration link.

$$u(k)=K_p e(k)+K_I\sum_{k=0}^{n}e(k) \qquad (5.1)$$

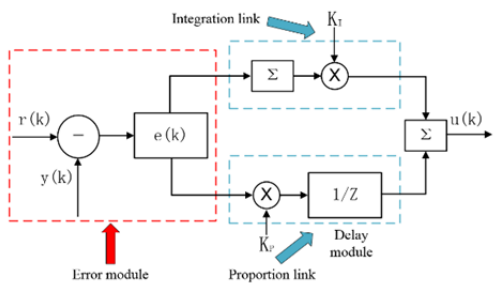


Figure 12: PI Controller.

CONCLUSION

This paper introduces the DSP frame and algorithm of LLRF of IR-FEL. Four times frequency sampling can realize IQ demodulation precisely and reduce DC offset. Pipeline CORDIC can calculate amplitude and phase by parallel and shift operation. FIR filter is used to improve frequency selected performance. Feedback loop use digital PI controller to adjust system output.

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