LOW LEVEL RF CONTROL SYSTEM ARCHITECTURE OF IR-FEL*

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Abstract

Infrared free electron laser (IR-FEL) is one type of laser driven by accelerator and generated by undulator. It is built by National Synchrotron Radiation Laboratory (NSRL). Compared to synchrotron radiation light source, it have much higher demand of beam quality. Low level RF control system (LLRF) need to reach higher controlled accuracy corresponded to the demand. Accelerating structure which contains one pre-buncher, one buncher and two accelerating tube can accelerate beam to 60MeV. Frequency distribution system use direct digital synthesizer technology to generate 5 signal of different frequency. LLRF system detect 8 channels signal, one for control loop, and the others for monitor and interlock. The hardware contain MTCA.4 architecture which is advanced in global; RF board for downconverter and IQ modulation output; DSP board for sampling, controller and transmission.

INTRODUCTION

Infrared free electron laser (IR-FEL) have the advantage of high power, high efficiency, high light, wavelength adjusting continuous, time and space coherence, and can be widely used in the science of biology, material, environment and so on. IR-FEL use LINAC to accelerate beam to relativity velocity and use period magnetic fields of undulator to generate coherent radiation. The undulator has high demand of the quality of electron beam such as energy of 60MeV, beam length of 5ps, energy dispersion of 120keV, horizontal emittance of 9.6 mm*mrad and vertical emittance of 9.8 mm*mrad. Microwave system which decide beam quality on greater extent can mainly divided into accelerating structure, power amplifier system, frequency distribution system and low level RF control system[1].

ACCELERATING STRUCTURE OF IR-FEL

The linear accelerator is used to accelerate electron to relativity power and modulate the energy and density of electron by radio field. Electron beam generated by electron gun have repetition frequency of 476/n MHz, electric charge quantity of 1.5nc and pulse length of 1ns. The LINAC can bunch beam to 1nC and 5~10ps and accelerate beam to 60MeV. See Fig. 1, accelerating structure of the LINAC is consisted of a pre-buncher, a buncher and two accelerating tube.

The pre-buncher is subharmonic cavity with material of stainless steel. Its design objective contains the RF frequency of 476MHz, the no load shunt impedance of 400~500kΩ, the no load Q of 2500~3500 and the cavity voltage of 45kV. The beam length can be compress from 1ns to 40ps with the cavity voltage of 40kV.

The buncher is travelling wave accelerating structure with work frequency of 2856MHz, constant gradient of 9MV/m and 2pi/3 mode which can compress beam to 5~10ps and accelerate electron to 3Mev. It totally have 11 cells which contain 4 phase velocity changed cells and 7 light velocity cells. The former have the phase velocity of 0.63, 0.80, 0.915 and 0.958 respectively[2].

The last accelerating structure is two accelerating tube with work frequency of 2856MHz, constant gradient of 25MV/m and 57 cells respectively. Each tube can accelerate electron beam current of 300mA to increase energy of 30Mev.

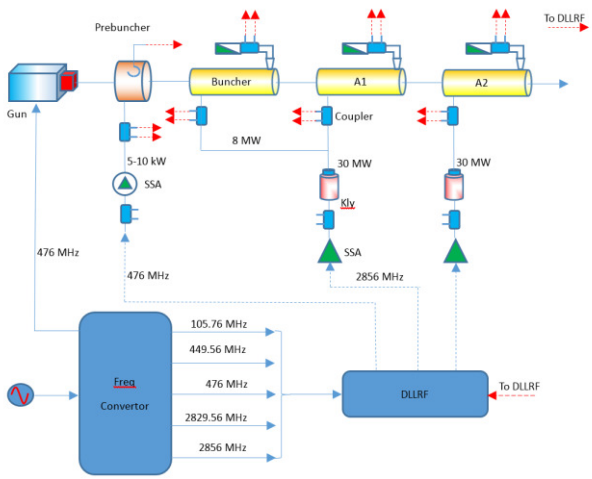

Figure 1: Structure of microwave system of IR-FEL.

Power amplification systems use pulse with 15us length and 0.1% flatness. The pre-buncher have input power of 5~10kW which can be driven by solid state amplifier through coaxial cable. The buncher have input power of 8MW. The first 30MW klystron can drive the buncher and the first accelerating tube and the second 30MW klystron can drive the second accelerating tube. Waveguide is used in S-band high power transmission.

FREQUENCY DISTRIBUTION SYSTEM

The frequency distribution system is used to generate 5 signal of different frequency to drive LLRF system and power amplifier system. Fig. 2 is the structure of frequency distribution system. Fig. 3 is the model of frequency distribution system. The input frequency is 476MHz from the master oscillator which is used to control the time series of whole accelerator. The output signal can be divided into 4 type, such as reference signal, local signal, clock signal and control signal. The reference

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frequency is 26.44MHz higher than local frequency. According to the driven amplifier, the reference frequency can be 476MHz or 2856MHz, the consistent local frequency will be 449.56MHz or 2829.56MHz. The clock frequency is always 105.76MHz. The control signal is 79.33MHz which is used to control the time serial of accelerator and laser. We don't inject control signal in the model of frequency distribution system.

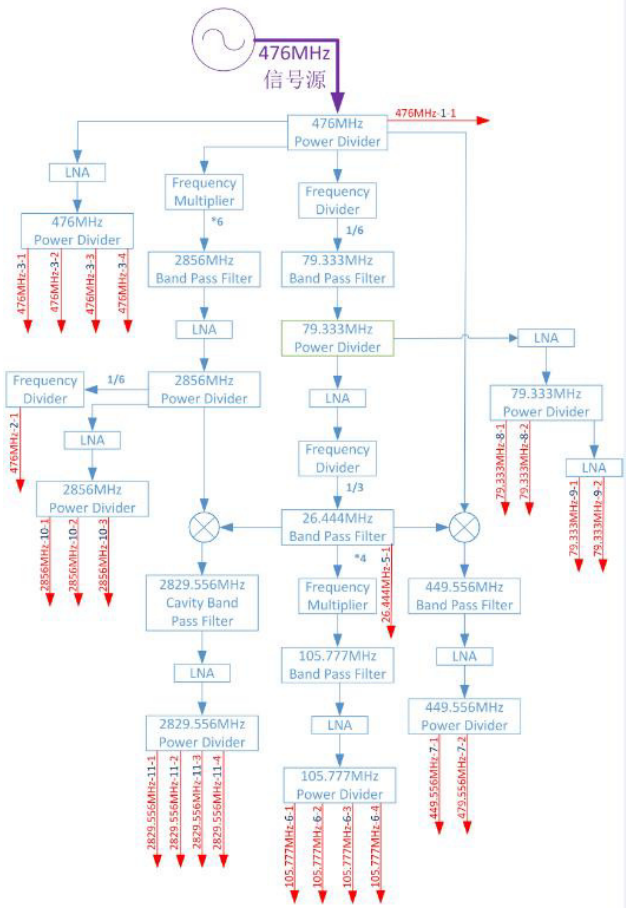

Figure 2: Structure of frequency distribution system.

Figure 3: Model of frequency distribution system.

The system uses direct digital synthesizer (DDS) technology and has operation bandwidth of 5MHz which can reduce the influence of master frequency shift [3] DDS uses frequency of the same reference signal source to calculate, so that it won't exit phase shift and accumulated shift [4]. The phase jitter addition is lower than 0.15° of 476MHz and 1° of 2856MHz. The suppression of harmonic wave is better than 50dBc and the suppression of noise wave is better than 65dBc. The stable of RF power is better than 0.2% and the isolation between input and output is better than 25dB.

We use spectrometer to test the system, test result is shown as Table 1. The SNR of REF2 and LO2 are not good enough to the demand of 80dBc. The reason should be the frequency multiplier has bigger additional noise.

Table 1: Noise of Frequency Distribution System

(MHz)	SNR	Noise Factor
Source@476	86.29dBc	/
CLK@105.77	83.83dBc	1.7620
REF1@476	82.30dBc	2.5061
LO1@449.56	85.34dBc	1.2445
REF2@2856	64.03dBc	168.2674
LO2@2829.56	67.32dBc	78.8860

SIGNAL TRANSMISSION OF LLRF

Because the pre-buncher, buncher, accelerating tube have smaller interval distance, their control system can be integrated. LLRF need to acquire 8 signal from the link of power amplifier. The signal transmission of LLRF is shown as Fig. 4.

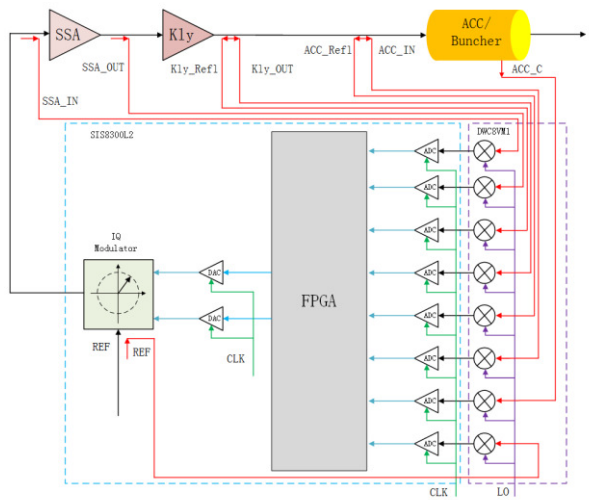

Figure 4: Signal transmission of LLRF.

SSA_IN signal is the input of solid state amplifier and is used for LLRF control signal. SSA_OUT signal is the output of SSA and is used to monitor the working position of SSA such as magnification, frequency and phase.

Kly_OUT signal is the output of klystron and is used to monitor the working position of klystron. Kly_Refl is the signal transmitted to klystron which reflected from accelerating structure. It is used to protect klystron, SSA_IN will be shut down when Kly_Refl is too high.

ACC_IN signal is the input of accelerating structure. SSA_IN will be adjusted when ACC_IN departure the set point. ACC_C signal is coupled from the accelerating structure and used to monitor the RF field in it. ACC_Refl signal is reflected from accelerating structure and also used to protect klystron which can prevent measured error of Kly_Refl. Kly_Refl and ACC_Refl are both safety interlocking signal.

REF signal is used to monitor the reference signal used in vector modulation of LLRF.

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HARDWARE OF LLRF

MTCA.4 system architecture is used in the LLRF of IR-FEL and have advantage of flexible backplane, better heat dispersion, reliability and compatibility. Fig. 5 is the real product of MTCA.4 system. RF board (model DWC8VM1, STRUCK) and DSP board (model SIS8300L2, STRUCK) carried on the system and connected each other through J30 and J31 port. VHDL code can be downloaded to DSP board through JTAG port or PCIE bus.

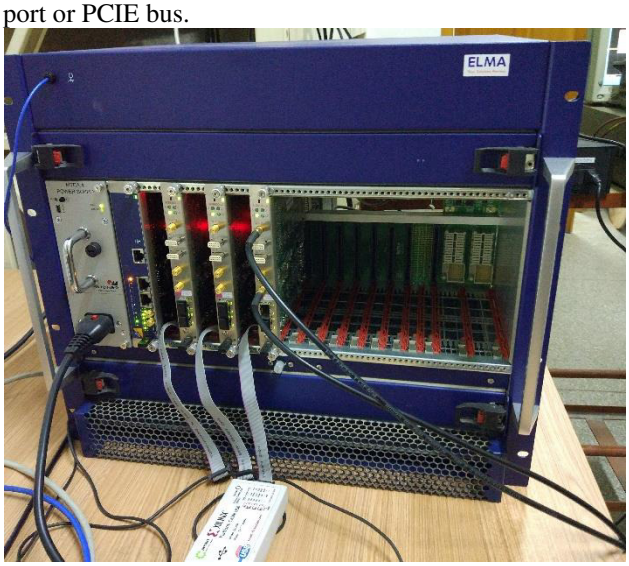

Figure 5: MTCA.4 system.

See Fig. 6, RF board is used to make down-convertor and IQ modulation. 8 paths of RF input signal mixed with LO signal to get IF signal which has the frequency of 26.44MHz. The programmable attenuator can be configured by user IIC to make ADC work in full scale. REF signal is used for IQ modulation in the Vector Modulator to modulate the I and Q signal of 26.44MHz and up-convertor to REF frequency. CLK signal can used for working clock of DSP board, but this may cause greater path delay and jitter.

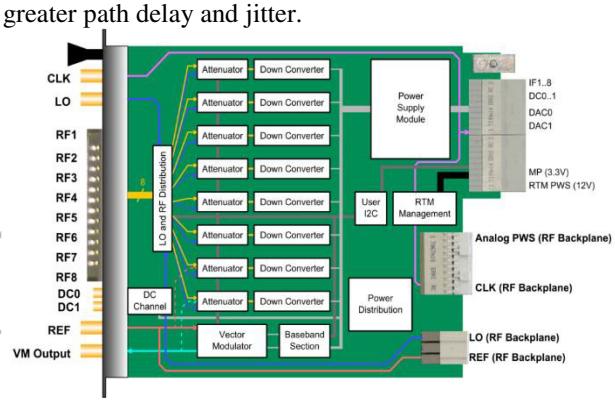

Figure 6: RF board.

Fig. 7 is the functional diagram of DSP board. DSP board uses Virtex-VI FPGA as its core processor. 5 dual channel ADC are used to sample 8 path RF analog signal. Each ADC uses 4 times frequency sampling to get I and Q component directly. Digital I/Q output from FPGA to DAC after control by algorithm. The two clock input on the DSP board respectively are SMA and Harlink port, both are low voltage difference signal. Harlink and SFP can also used for trigger signal input. SFP port use optical signal input and always used in long distance control system.

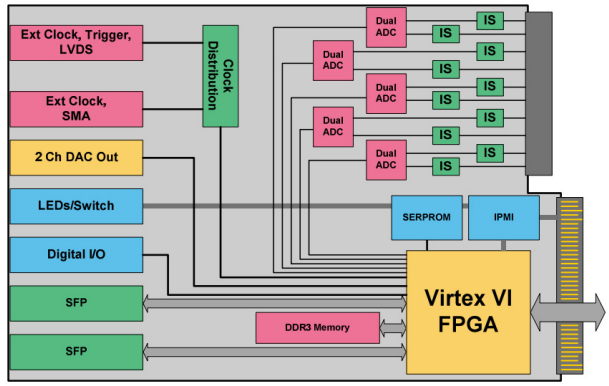

Figure 7: DSP board.

CONCLUSION

This paper introduce the frame of accelerating structure, frequency distribution system, signal transmission and hardware of LLRF. Accelerating structure which contains one pre-buncher (476MHz), one buncher (2856MHz) and two accelerating tube (2856MHz) can accelerate beam to 60Mev. Frequency distribution system use direct digital synthesizer technology to generate signal of 5 different frequency from the signal source of 476MHz. LLRF is based on the MTCA.4 architecture which is advanced in global. The hardware contain RF board and DSP board, the former is used for downconverter and vector modulation output, the latter is used for sampling, controller and data transmission.

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