DIGITAL PROCESSING ELECTRONICS FOR THE ELETTRA TRANSVERSE MULTI-BUNCH FEEDBACK SYSTEM

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Abstract

Coupled-bunch instabilities excited by RF cavity high order modes or resistive wall impedance can seriously limit the performance of third generation synchrotron light sources like ELETTRA. These instabilities can be cured by the use of active feedback systems. In the digital bunch-by-bunch approach adopted at ELETTRA, the position of the 432 bunches is sampled and corrected employing 500 Msample/s A/D and D/A converters. The correction values are computed by a multi-processor architecture made of state-of-the-art DSPs (Digital Signal Processors). A modular design allows to use commercial-off-the-shelf (COTS) components for the most critical parts of the system.

1 SYSTEM OVERVIEW

The basic principle of a bunch-by-bunch feedback is that each bunch is considered as an independent oscillator at the betatron frequency and the motion of each bunch is controlled individually. The task of the feedback system is to correct the trajectory of each bunch with a transverse electromagnetic field in order to add a damping term to its equation of motion. The strength of the correction kick for each bunch can be derived from the position error of the same bunch detected in another location of the ring.

Figure 1 shows the block diagram of the ELETTRA transverse multi-bunch feedback system [1].

The position of the 432 bunches is detected by the four buttons of a Beam Position Monitor followed by a "hybrid network" that produces the x, y and I signals. The wide-band signals are demodulated by the "RF front-end" giving a base-band 0÷250 MHz signal which represents the position error of the bunches passing through the BPM at the frequency of 500 MHz. This analog signal is sampled by a fast 500 Msample/s A/D converter. The samples are passed to a bank of DSPs (Digital Signal Processor) that calculate the corrections and these are converted to an analog signal by a D/A converter at 500 Msample/s. This signal represents the corrections that have to be applied to the electron bunches as they pass through the kicker. A RF power amplifier supplies the necessary power to drive the kicker.

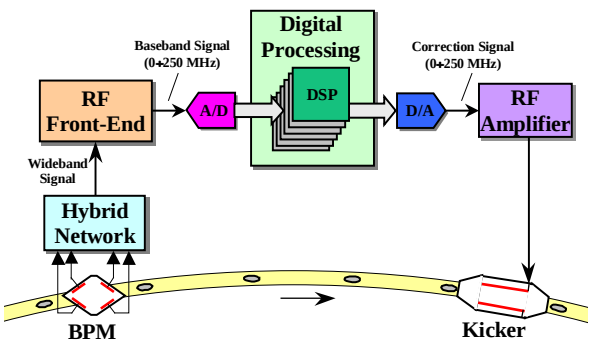

Figure 1: Block diagram of the Transverse Multi-Bunch Feedback System

2 PROCESSING ELECTRONICS ARCHITECTURE

After a thorough analysis of the computing power required to process in real-time this unprecedented amount of data (500 Msample/s), a parallel architecture made of a bank of DSPs has been adopted. The Texas Instruments TMS320C6201 fixed point DSP has been chosen. The choice of using a modular architecture based on VME boards interfaced through standard high-speed communication paths allows flexibility and upgradability.

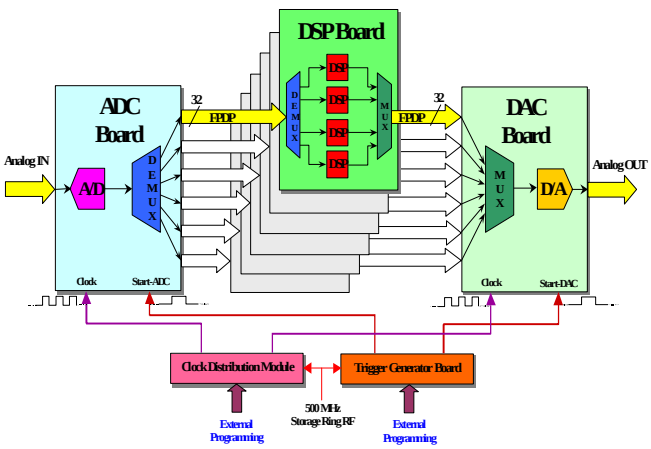

Figure 2: Block diagram of the processing electronics

The block diagram of the system is shown in figure 2.

The A/D Converter (ADC) VME board samples the analog signal at 500 Msample/s with 8-bit resolution. The first de-multiplexing of the data is performed on board into six 32-bit data paths which are individually connected to a FPDP (Front Panel Data Port) parallel

interface. Each FPDP is connected to a DSP board by means of an Interface Module that distributes the incoming data to its four DSPs. After processing, the data from the DSPs are multiplexed following a symmetric scheme and are converted to analog by the 8-bit D/A Converter (DAC) VME board. The whole process is synchronized by timing signals provided by the timing electronics.

The transverse feedback processing electronics will be made of two VME chassis: one for the horizontal and one for the vertical plane. Each of them will host one ADC board, one DAC board, six DSP boards equipped with the Interface Module, and one timing board. The VME bus will be used to initialize, control and monitor the system and to download the programs into the DSP boards.

The ADC board, DAC board and DSP boards are commercial-of-the-shelf components. The Interface Module and the timing electronics are in-house developments.

3 ADC AND DAC BOARDS

The ADC and DAC boards are respectively the ADC750 and DAC750 models from Celerity System Incorporated. These boards perform A/D and D/A conversions at up to 750 Msample/s with 8-bit resolution. For the Feedback System we operate them at the bunch crossing frequency, i.e. 500 Msample/s, using a clock derived from the main RF signal and connected to the external clock inputs.

The 8-bit data out of the A/D converter of the ADC board are first stacked in 32-bit words and then sequentially distributed to the six FPDP output ports. The six ports work at 20.8 MHz.

An external trigger signal (Start-ADC) provided by the timing electronics starts the conversion and the de-multiplexing process. Being the bunch number (432) divisible by 6 (number of FPDPs) times 4 (number of byte per FPDP word), each FPDP port always carries the samples relative to the same group of 72 bunches. This is the basic principle of the bunch-by-bunch feedback, where each group of bunches is processed always by the same DSP on the same DSP board.

In the DAC board the input data from the FPDP ports are treated in a complementary way with respect to the ADC board. The FPDP data are multiplexed into one 8-bit path and transformed to analog by the D/A converter. In addition, some data buffering is performed by the use of FIFOs to de-couple from possible variations in the processing chain delays.

An external trigger signal (Start-DAC) provided by the timing electronics starts the multiplexing and the conversion process. Start-DAC is generated with a programmable delay relative to the Start-ADC in order to make the correction kicks synchronous with the bunches passing through the kicker.

4 DSP BOARD AND INTERFACE MODULE

The DSP board adopted is the Pentek model 4290. Figure 3 shows the DSP board block diagram. The four TI-TMS320C6201 DSPs communicate with the mezzanine Interface Module via high-speed bi-directional FIFOs (BI-FIFO). The DSP use the BI-FIFO to acquire the bunch position samples and put the correction samples after processing.

Each of the DSPs is in charge of processing the samples of a given group of bunches. The Interface Board receives 32-bit words from the FPDP Input and writes them to the BI-FIFOs of the DSPs to which they are specifically assigned. At the same time it reads the BI-FIFOs and sends out the data words to the FPDP Output. The Interface Module acts as a programmable bi-directional commutator: the switching rules are defined in a table where, for each of the incoming/outgoing FPDP words relative to one machine turn, the destination/source DSP is specified. As more than one destination can be specified for each of the input words, they can be sent e.g. both to the first DSP and to one of the other three. This allows using one DSP for beam diagnostics and the other three for the actual feedback. The table is downloaded on the Interface Module at the time of system initialization.

The TI TMS320C6201 is a fixed point DSP clocked at 200 MHz (5 ns instruction cycle). The VLIW (Very Long Instruction Word) architecture allows to execute up to eight instructions every cycle. The challenging problem is to be able to execute all of the necessary operations in one revolution period (864 ns). With a highly optimized code written in Assembler, the time needed to execute all the operations for a 5-tap Finite Impulse Response (FIR) filter is 600 ns, that is shorter than the revolution time.

Another critical issue is the data transfer between the

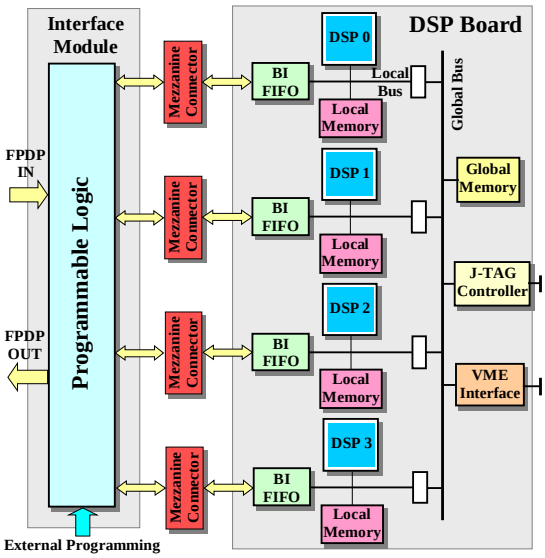

Figure 3: Block diagram of the DSP Board and the Interface Module

DSP and the BI-FIFO. Simulations carried out with the machine/feedback simulator show that the feedback performance degrades with betatron tune shift when the number of processing revolution periods increases. Therefore, the time the data remain in the DSP board must be minimized as well as any delay on every component of the feedback chain. A thorough use of the BI-FIFO facilities, interrupts and Direct Memory Access (DMA) allows to transfer data in a very effective way without interference with the CPU.

5 TIMING ELECTRONICS

The transverse feedback system relies on a very strict timing. The A/D converter must sample the analog signal synchronously to the bunch crossing at the BPM and the D/A converter must generate the analog corrections in phase with the bunches passing through the kicker. Moreover, the Start-ADC and Start-DAC trigger signals must start the conversions in a deterministic and repeatable way with respect to the bunch structure to let every DSP work with a known group of bunches. A new design has been undertaken to fulfil these requirements. It consists of a Clock Distribution Module and a Trigger Generator Board (figure 2).

The Clock Distribution Module accepts a 500 MHz sinusoidal signal from the storage ring RF and generates two 500 MHz Differential ECL (DECL) signals which are the clocks used by the ADC and DAC boards. The phase of the two output signals can be independently programmed in a 5 ns range with 5 ps resolution.

The Trigger Generator Board is a VME general-purpose timing board. For the transverse feedback system it provides two DECL signals: Start-ADC and Start-DAC. By conveniently programming the board via the VME interface it is possible to place the rising edge of the two trigger signals in any position of the revolution period with a resolution of 10 ps. The Start-DAC must follow the Start-ADC and the time between the two has to take into account the delay of the data flowing from the ADC to the DAC board.

6 SYSTEM FEATURES

Being the feedback core realized by software programs, a high degree of flexibility in the implementation of the control algorithms is provided.

The basic requirements for the feedback algorithm are DC rejection and appropriate gain/phase at the betatron frequency. A 3-tap FIR is the most simple digital filter which can be used. However, many features can be added when a more complicated filter is implemented. Studies have been carried out with the support of a machine/feedback simulator [1] using 5-tap FIR and Infinite Impulse Response (IIR) digital filters.

The maximum RF power supplied by the amplifier can be a limitation of the feedback performance when a strong cavity High Order Mode is excited. In order to fully exploit the available power, it can be convenient to increase the open-loop feedback gain and to make the feedback saturate when the oscillations are large. On the other hand, high gain can lead to a greater residual error when the oscillation is damped. The possibility of changing the filter parameters on-the-fly when the feedback is running allows to change the gain and/or the filter type and apply the best algorithm in the different phases of a mode damping.

With a convenient programming of the DSPs, one uncontrolled bunch can be used for betatron tune measurements while applying the feedback to the others. With the measured tune value it is possible to re-calculate the filter parameters and change them when the feedback is running, thus compensating for machine tune shifts.

Thanks to the programmability of the DSPs and the Interface Module the same processing electronics will be used for the Swiss Light Source transverse feedback system and may be adopted also for longitudinal multi-bunch feedback systems.

7 STATUS

A transverse bunch-by-bunch digital feedback system has been designed at ELETTRA for damping multi-bunch instabilities. The digital processing electronics is realized by a programmable modular multi-processor architecture.

The system mainly relies on standard COTS components. The ADC/DAC boards have been ordered while a sample DSP board is under test. The timing electronics and the Interface Module are in-house projects: the first prototypes are foreseen by the end of November.

The feedback project is a collaboration with the Swiss Light Source which is developing the kickers and the RF front-end. The system will be installed and commissioned at ELETTRA: the first tests are foreseen by the end of 1999.

8 AKNOWLEDGEMENTS

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