PCI TO CAMAC EXECUTIVE CRATE INTERFACE

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Abstract

Hardware and software interfaces have been developed for PCI bus to CAMAC. The PCI bus is currently supported on many platforms including Alpha AXPs and PCs. The hardware includes two interface cards, one connecting to the PCI slot in the ALPHA's chassis and the other located in a CAMAC executive crate. Software has been developed for the OpenVMS AXP environment and a port to the NT platform is being planned. This paper describes the hardware and software designs, performance and configuration details.

1 INTRODUCTION

The existing TRIUMF control system consists of several CAMAC [1] highway systems. Each system has at its root a GEC executive crate [2] allowing multiple CPUs access to any of the serial and parallel branches in that system.

Several years ago a pair executive crate interface modules (0782/0783), developed at TRIUMF, formed the connection between the Q-Bus of a VAX and the GEC executive crate. The 0783 was located in the executive crate and the 0782 in the Q-Bus chassis of the VAX. Later, ALPHA AXPs were introduced into the control system and a commercially available module, the BCI 2100, was purchased to connect the PCI bus [3] of the ALPHA to a Q-Bus expansion chassis for the 0782 modules. After this, the Q-Bus interface ICs used in the design of the 0782 became obsolete and could no longer be purchased.

Looking at the new computers in use today, PCs and ALPHA AXPs, it was clear that PCI is the bus of choice. It was therefore decided an interface from the PCI bus directly to the GEC executive crate systems was required.

Since the existing 0783 executive crate interface works well, the possibility of designing a PCI to 0783 interface was considered. This required only one new module design rather than the two needed if both ends of the link were replaced. The software driver changes would also be reduced because the 0783 executive crate module requirements were well known.

2 HARDWARE INTERFACE

2.1 0783 Register Access Sequence:

The PCI interface is designated the 0934 PCI to 0783 CAMAC interface. In the 0934/0783 system CAMAC arbitration and execution takes place independently of the PCI operations. Figure 1 shows the sequence of 0783 read and write operations needed to execute a CAMAC cycle. Each 0783 register access requires a single PCI cycle.

The PCI bus is a synchronous system in which changes of state are recognized at system clock edges. The 0783 module, originally designed to work with Q-Bus, is an asynchronous system requiring handshake signals between the 0783 and the 0934. The 0934 interface synchronizes the two systems by having the PCI wait for the ~rply handshake signal from the 0783. If the ~rply signal is not received within 8 uSec, the 0783 access is terminated and the 0934 reports the transaction status in an error register within the 0934 module.

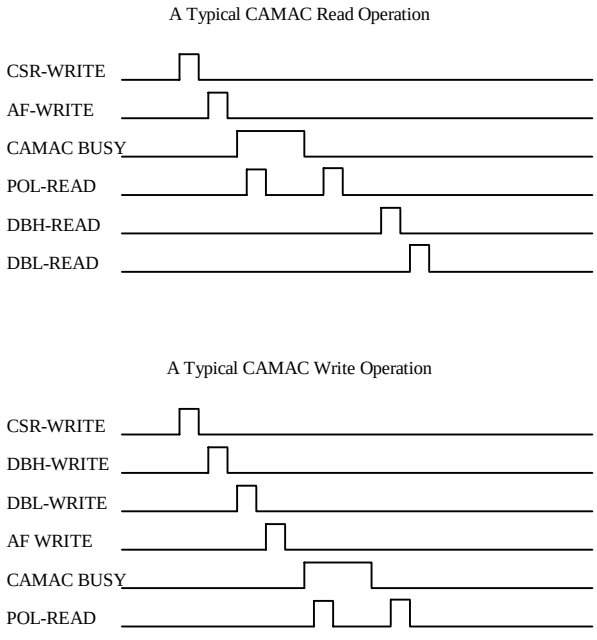

Figure 1. Timing diagram for CAMAC read-and-write operations.

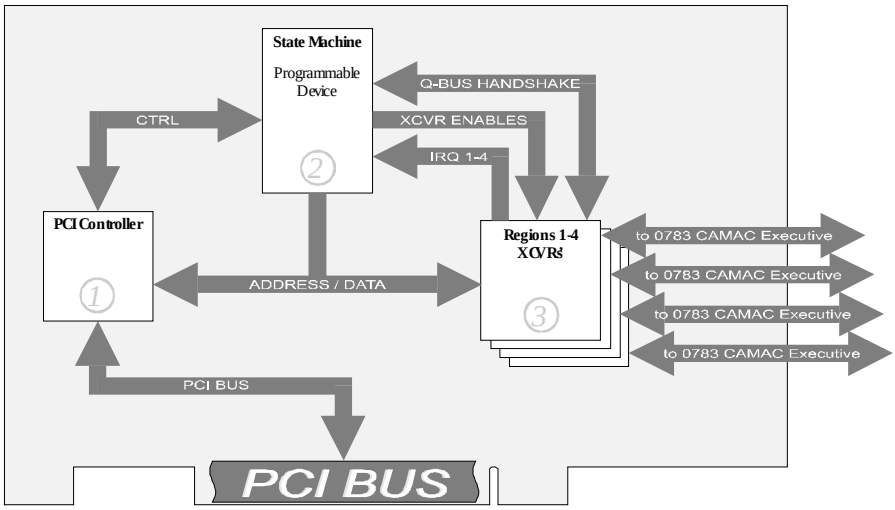

Figure 2. 0934 Module Block Diagram

2.2 0934 Module Block Diagram:

(1) The PCI Controller:

A commercially available IC handles the PCI communications block. It has five PCI regions available, region(0) through region(4). The PCI controller uses Region(0) for its own internal register space. The 0934 module maps Region(1) through Region(4) as 32 bytes of 16-bit wide I/O register space. The 0934 board supports up to four CAMAC executive systems by using one region per system.

Because of the Plug and Play nature of PCI, the base address of each of these regions is assigned by the computers BIOS at power up, and must be determined by software at the CAMAC driver level. Once determined, the driver gains access to the 0783 registers using the regions base address + the specified 0783 registers offset. (See Figure 3.)

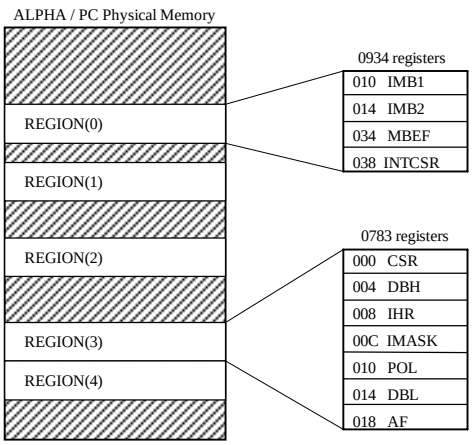

Figure 3. Addresses for 0934 & 0783 registers.

(2) The State Machine:

A programmable device performs several functions on the 0934 PCI board. It contains a state machine, which controls the transaction between the 0934 and the 0783 CAMAC System Crate Interface module, the transaction error handling, and CAMAC Interrupt reporting functions.

(3) The Regions 1-4, Bus Transceivers:

To be compatible with the transceivers in the 0783, the 0934 PCI Interface uses 6 - DS36950 quad transceivers per region. The state machine controls the transceiver Enable/Disable. The CAMAC Interrupt transceiver is always enabled to ensure the 0934 will report an interrupt from the CAMAC system as soon as possible.

2.3 The 0934-0783 Transaction

When the PCI Controller decodes a PCI address within one of the four 0783 Regions, see Figure 4, it latches the PCI Address (and Data if a write operation) from the PCI bus. It asserts CTRL signal *PTATN~* to notify the state machine of a 0783 access request. The state machine then begins the transaction between the 0934 and the 0783. The PCI cycle is completed when the Q-BUS HANDSHAKE signal *RPLY~* is received by the 0934. If this signal is not received within 8 uSec, the PCI cycle is terminated by the 0934 and a transaction error is indicated.

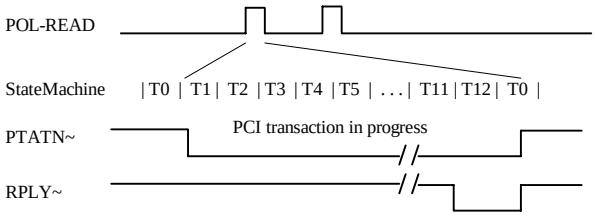

Figure 4. Simplified timing diagram for an 0934 – 0783 transaction

2.4 CAMAC Interrupt reporting

When a CAMAC interrupt (LAM) is present in the executive crate, the 0934 detects this and can generates a PCI interrupt if enabled.

3 SOFTWARE INTERFACE

There are two components for the OpenVMS software interface: a shareable image and a device driver. The shareable image provides the CAMAC cycle calls and is installed as a privileged shareable image for non-privileged user to access the CAMAC system. The CAMAC device driver handles CAMAC interrupts generated by the multiple executive crate system.

3.1 CAMAC Shareable Image

An existing shareable image which provides the standard IEEE CAMAC calls such as CDREG and CFSA as well as non-standard calls to support the commercially available BCI interface card was modified to support the new PCI interface card. It supports region specific access, executive crate specific access, as well as internal register access for the card.

When a process first accesses CAMAC, it traverses the Adapter Control Block (ADP) list to locate one or more CAMAC PCI interface(s) by matching the Device ID and the Vendor ID of each PCI module. Once the module is found, the four address spaces corresponding to the four possible regions are examined. A POL register read is carried out to check if actual executive crate is attached to it. If so, The device I/O space is mapped to a global section for subsequent CAMAC access. A table is set up to map the region number to an actual executive crate IDs and vice versa. The completion of a CAMAC cycle is signaled by a change in the DONE bit of the 0783 POL register. A polling mechanism is used to detect its occurrence

It has been our experience that detailed error code information helps facilitate hardware trouble-shooting. So special attention is paid in setting up unique error codes for various error conditions. Their occurrence could be grouped in four general areas: errors in CAMAC equipment, errors in the 0783 module, errors in the 0934 PCI module and errors in parameter passing.

3.2 CAMAC Device Driver

The approach is very similar to the BCI CAMAC interface driver reported in ICALEPCS 97[4]. The driver provides a SETMODE function which requests an attention AST to be delivered when the CAMAC interrupts. Since all four regions of the interface card are capable of generating interrupts, four multiple list heads for AST Control Block (ACB) are set up. In the Interrupt Service Routine, it determines which region has generated the interrupt and delivered the AST to the corresponding list.

4 PERFORMANCE

Performance was measured on two PC platforms using a pseudo CAMAC driver, one which performs all necessary 0783 accesses and error checking to generate a CAMAC cycle, but does not allow for multiple processes to 'share' the device. The results of this test, shown in Table 1, demonstrate the maximum throughput of the 0934 / 0783 system.

Table 1

CPU Type	CAMAC F(0)	CAMAC F(8)	CAMAC F(16)
Pentium 133	128 kHz	181 kHz	134 kHz
Pentium II 350	127 kHz	179 kHz	135 kHz

Performance was also measured using the CAMAC shareable image. See Table 2. The reduced throughput in the ALPHA is attributed to the software overhead involved.

Table 2

CPU Type	CAMAC F(0)	CAMAC F(8)	CAMAC F(16)
Alpha AXP 250	32 kHz	36 kHz	34 kHz
Alpha AXP 266	37 kHz	42 kHz	39 kHz

5 SUMMARY

The design of the 0934 PCI was undertaken as a replacement for the commercial module BCI-2100 and the TRIUMF 0782 Q-Bus module. It installs into a 32bit 33 MHz PCI bus and can support up to four CAMAC executive crate systems. It connects the synchronous PCI bus to the asynchronous CAMAC through a 16bit parallel cable connected to a TRIUMF 0783 executive crate module. The 0934 module places the PCI bus in a wait state until the asynchronous CAMAC transaction is completed. It supports CAMAC interrupts (LAMs) from each of the four CAMAC executive crates.

A further module pair is planned to replace the 0934 and the 0783 modules. These new modules are to support 32bit data transfers over a high speed serial connection.

REFERENCES

[1] CAMAC Instrumentation and Interface Standards, IEEE, New York, 1982.

[2] GEC-Elliott Process Automation (now HYTEC electronics Ltd) System Crate Catalogue, 1982.

[3] PCI Local Bus Specification, Rev 2.1, 1995.

[4] K. S. Lee, "Handling CAMAC Interrupts in Alpha Open VMS/PCI", ICALEPCS 97, 1997.