SPD VERY FRONT END ELECTRONICS

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ABSTRACT

The SPD (Scintillator Pad Detector) is a part of LHCb calorimeter. It is in charge of discerning between electrons and photons for the level0 trigger. This detector is a plastic scintillator layer where charged particles will produce while photons will not, ionisation on the scintillator. This ionisation generates a light pulse that is collected by a WaveLength Shifting (WLS) fibre that is twisted inside the scintillator cell. The light is transmitted through a clear fibre to the readout system.
The detector is divided in about 6000 cells of different size to obtain better granularity near the beam.. For cost reduction, these 6000 cells are divided in groups of 64 channels using a 64-channel MAPMT for receiving information in the readout system. The signal from SPD PMTs is rather unpredictable as a result combining the low decay time of the WLS fibre and low photo statistics. Then, the signal processing must be performed by first integrating the total charge and later subtracting to avoid pile-up.
SPD Readout system is performed by an specific ASIC which integrates the signal, makes the pile-up compensation, and compares the level obtained to a programmable threshold (distinguishing electrons to photons), an FPGA which programmes the ASIC threshold and pile-up subtraction (The electronics is prepared to deal with programmable level of thresholds and pile-up compensation) and finally LVDS serializers, in order to send information to the first level trigger system.

INTRODUCTION

LHCb is one of the four detectors to be build on LHC, the future proton-proton accelerator in construction at CERN (European Center for Nuclear Research) in Geneva (Switzerland). It is expected to be running by 2007. LHC will be an intense source of hadrons containing quark b, a production of 1012 bb is expected, working at a luminosity of 2·1032 cm-2·s-1 at 40 MHz frequency. These data should provide measurements far more accurate than those obtained in the so-called first generation B-factories. The LHCb detector is designed to make precise studies of CP asymmetries and of rare decays in the B-mesons systems in the LHC proton-proton. collider.

LHCb structure contains a calorimeter whose main purpose is the identification of hadrons, electrons and photons and the measurement of their energies and trajectories. This is the basis of the trigger system containing information to study B physics and enables the reconstruction of this interactions produced in the collider.

The LHCb calorimetry [1] has four elements: a hadronic calorimeter (HCAL), an electromagnetic calorimeter (ECAL), a Preshower detector (PS) and a Scintillator Pad Detector (SPD). The system provides high energy hadrons, electron and photons candidates for the first level trigger (Level 0 Trigger).

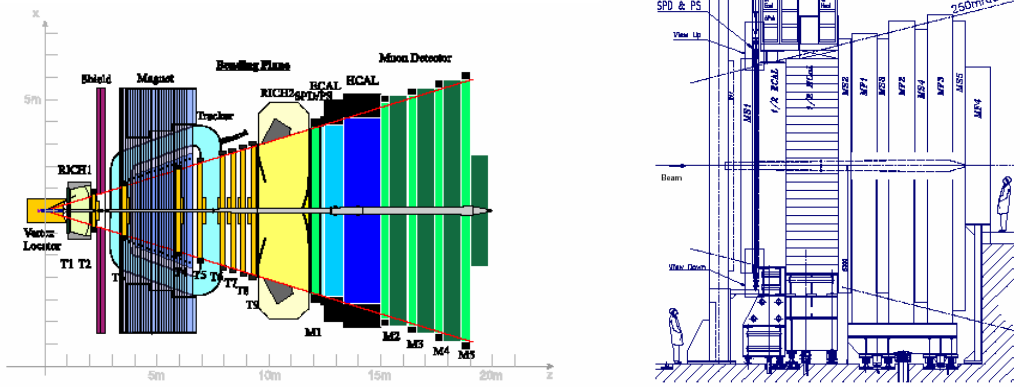

Figure 1: Layout for the LHCb spectrometer./ PS and SPD in LHCb detector

SPD INTRODUCTION

The SPD[1] is a plane of about 6000 scintillator cells of several sizes sitting in front of the lead plate of the PreShower.

Its mission is to increase Level 0 Trigger efficiency by distinguishing charged particles (mainly electrons)from neutral ones (mainly photons). Such distinction is to be made by measuring the energy deposited in the scintillator cells. A coil of Wavelength Shifting Fiber captures the emitted photons and takes them out the pad. A further connection to a clear fiber brings these photons in to the readout system. To lower cost and space, 64channel multi-anode photomultipliers are used to convert light into electrical signal. The expected output is one bit for every pad telling whether a charged particle passed by the cell in the current bunch crossing.

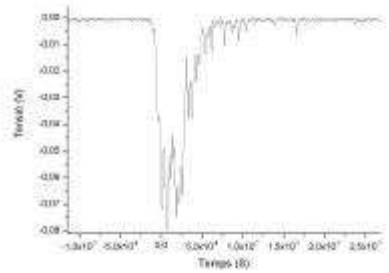

Figure2: Typical MIP signal pulse shape

The signal outing the SPD PMTs is rather unpredictable as a result of the low number of photostatistics, 20-30 photoelectrons per MIP, and due to the response of the WLS fibre, which has a decay time of around 12 ns (figure 3). This “slow” decay time means also that the signal spreads over more than one clock period. According to present data about the 80% of the signal is in the first period. This fact causes another bothering trouble: the potential tail of a high amplitude event could cross the threshold and provoke a fake trigger. Thus, pile-up correction is needed. A range of at least 5 MIP is required to be able to perform this compensation.

ELECTRONIC FUNCTIONAL DESIGN

The analog signal processing of the PMT signal is performed by an ASIC whose working frequency is 40MHz divided in two subchannels that work at 20MHz [9]. The processing involves:

- integrating each signal,

• subtracting and adjustable fraction of the charged integrated in the previous 25ns period (in order to correct pile-ups due to the tail of the expected signal is longer than 25ns),
• comparing the result to programmable thresholds foreach subchannel a digital output is obtained: '1' if above the threshold, '0' otherwise.

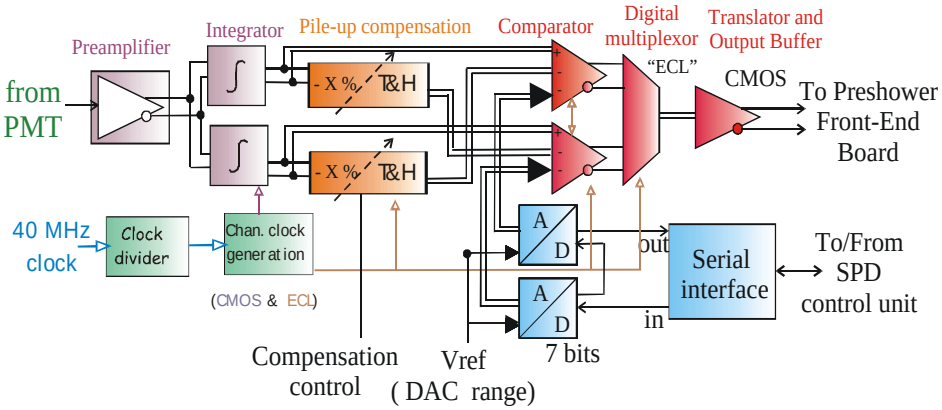

Figure3: Functional diagram of a discriminator channel.

Each subchannel has its own programmable thresholds in order to take care of pad size, PMT gain non-uniformities. Threshold values are fixed by internal DACs sharing a common external references. The programmable substractor is also set by an external reference. Final implementation, where each ASIC encapsulates 8 channels, is made using AMS 0.8 µm BiCMOS technology. To improve radiation tolerance, ring guards protect analog transistors and digital operations implement a triple voting system.
From those elements, functional design for the SPD readout is split into a Very Front End board hosting a PMT with its corresponding 8 ASICs and a control board sitting at the calorimeter front end crates and interfacing the experiment control system and the boards, as depicted in figure 5 Very Front End boards shall be located in boxes sitting on the top and the bottom of the detector, limiting the area of the VFE board to 9 × 9cm2.

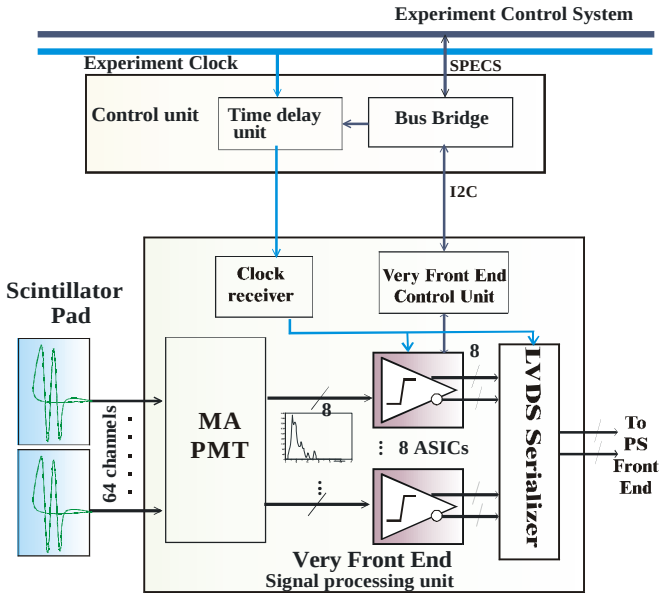

Figure 4: SPD readout system

Threshold values shall be dynamically fixed from the experiment control system through the control board, which shall also provide the system clock.
In order to save connector space and cabling data shall be sent to the PreShower front end card by a multiplexed LVDS link with a distance between 5-25 meters long. The combination of distance and speed (280Mbits/s) makes a problematic link that has to be tested cautiously.

VFE PROTOTYPE

The figure below shows the diagram block of the VFE:

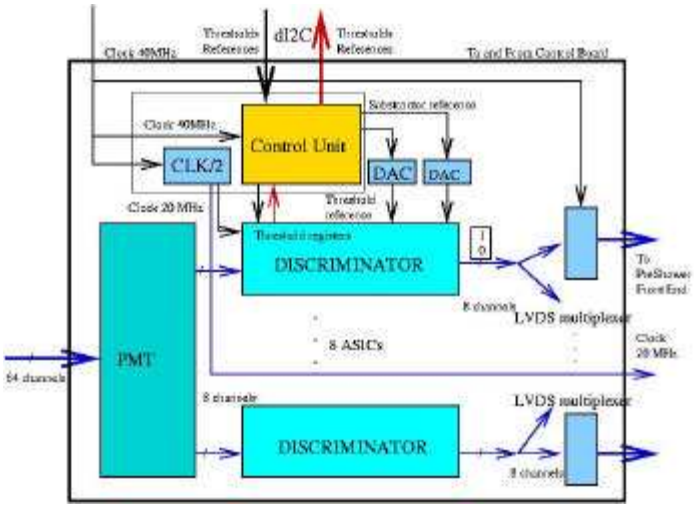

Figure 5: VFE Diagram Block

As a first attempt, the whole design fits in a 15cmx15cm card, but as a result of mechanical problems and the functionalities added, the design has been split to three different cards:

- Base card which contains MAPMT[8], and the active base of the MAPMT.
- ASICs card which involves the 8 ASICs (discriminator in the figure) and all the analogue part (subtractor reference for compensating the pile up, threshold reference for the whole card).
- Serializers card which contains the LVDS serializers, for the multiplexed LVDS link mentioned before, the FPGA as a control unit, LVDS transceivers.

Figure 6: Picture of VFE

All of the component passed the radiation qualification[6] (Single Event Effects and Cumulative Effects). Some useful components has to be discarded because they do not support the levels of radiation (E.g. DS90CR494, 64-channel LVDS multiplexer).

One of the challenges that the design of VFE board has is the voltage levels of components. For e.g. ASICs voltage supply is (+/-1.65V), and the output of the board should be 3.3V (in order to communicate the SPD VFE Board with the PreShower[1] FE board), this implies that it has to be a voltage level adaptation between both boards. This adaptation is made by a passive circuit (2 PIN diodes and 2 resistors).

TESTS AND RESULTS

Laboratory tests have been done about functionality, cooling and LVDS link.
Functionality tests show the good performance of the card. It has been tested the following:

- Programming internal threshold references for each subchannel in ASICs
- Programming DACs for external threshold reference and subtractor reference (pile up compensation)
- Power consumption. It is important to notice that the consumption of the card is an important point for the design of the whole system : a regulator card is needed to feed each VFE.
- Mapping. The SPD is not a subdetector alone, it belongs to the LHCb Calorimeter [1], and map each PMT channel from the Photomultiplier to the other detector has become a tedious task, as a result of the asymmetry of the detector itself.
- Noise. Its value is around 2mV and it is acceptable.
- Clocks. The shape of the signal has been checked in order to control the jitter.

Cooling tests, has been done in Clermont-Ferrand at LPC (Laboratorie Physique Crepuscoulaire) last July. The cooling is made by a cool water circuit around boards. A conductive material of heat put on the cards and it is in contact with an aluminium platform that contains the water circulating on.
Results showed that the maximum temperature achieved is near the limit of the maximum value of temperature of the FPGA.

Figure 7: Cooling Test

The third ones, LVDS tests has been one of the goals of the design. The requirements, 280Mbits/s and 25meters long, is not only the electronics design also the choice of the cables was one of the most important points. After making a considerable amount of tests in different cables, the best cable was a nexans one that accomplish this requirements. The table below shows the results:

More work has to be done in cooling in order to have some tolerances in temperature and on the other one, FPGA consumption tests are been done at the moment, showing a lower power consumption than in the test.
The LVDS link is fully tested, sowing a skew between pairs of the same cable is 2ns – 3ns, but skew between different pair of consecutive cable cuts is small: it needs a cross-connection scheme (figure 8).
The Bit Error Rate (BER) has been measured: BER<10-13 (6 links).

Grounding Tests are planned to be made next November.

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