

## BEAM POSITION MONITOR DIGITAL SIGNAL CONDITIONING

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### ABSTRACT

The performance of multi-channel fast data acquisition systems is limited by anomalies such as nonlinearity, hysteresis, channel-to-channel crosstalk, time, and temperature drifting. The beam position monitor front-end is an example of such a multi-channel system in which the anomalies mentioned above significantly deteriorate measurement performance. This article presents a solution to this problem: an acquisition rate ( $>100$  MHz) Digital Signal Conditioning (DSC) System implemented on a state-of-the-art FPGA. The article also discusses the architectures for efficient acquisition rate digital compensation and software architectures for observing system behavior at lower (decimated) data rates.

### INTRODUCTION

Technology advances in speed and resolution of AD converters is magnifying analog front-end amplitude and frequency dynamics. It is moving the boundary between the analog and digital worlds closer to the sensors. Whereas digital processing is characterized by arbitrary precision and drastic price lowering, analog front-ends are not following such progress. At the point where price/performance optimization is saturated by the analog front-end solution, the digital correction of the sampled signal is a potential approach. The characteristic of the inaccurate analog front-end can be analyzed and by mean of an inverse model compensated for in digital space. In real systems the nature of inaccuracy varies by time, is nonlinear, and greatly depends on different working conditions, so that a permanent model is not useful. In this case two approaches to observing the system anomalies are possible. By using a non-coherent pilot signal, the observer on the end of the signal chain can extract and analyze the pilot signal response. The second approach expects controlled signal chain characteristic varying, so that changes in signal response can be explored and ultimately used for correction.

### LIBERA ELECTRON BEAM POSITION PROCESSOR

The Libera electron beam position processor is a fast data acquisition system with very demanding amplitude dynamics. With Libera an additional 60 dB of dynamics is achieved through digitally controlled amplification. The four channel amplifiers suffer on gain inequality and unequal gain stepping. They are also nonlinear, have crosstalk, and drift with time, temperature, and power supply voltage. Including ADC anomalies, the system also exposes hysteresis characteristics. This is a starting point that cannot expect sufficient resolution and beam current dependence (BCD) in the most direct Libera realization. The switching technique was chosen as the most promising approach for resolution and BCD improvement [1,2,3]. It is based on averaging the gain of the four channel amplifier through time sharing of each channel to each signal. The technique worked well in a phase aligned system. In a phase misalignment case, every change in the signal path introduces a transient at the digital down converter (DDC) output. The transient is not only a discontinuity in phase, but also amplitude and apparently beam position error. This is also the reason why the crossbar switching technique fires a chain of side effects, so that a systematic DSC is the only appropriate solution. It includes phase and gain equalizing, crosstalk and hysteresis compensation, and linearization. AGC is part of the signal conditioning and provides optimal gain due the best resolution and BCD performances.

On the other hand, the plane beam position information is defined as the amplitude ratio of the four pickup signals. The fully differential measuring scheme is efficient in many ways. It compensates all common mode perturbation and suppresses symmetric inequality in the signal path. There is also a

general benefit in its double measuring range. Symmetry of the analog front-end is one of the most challenging issues in the design.

In addition to the symmetric signal attachment (with respect to the RF PCB layout and asymmetry of the crossbar switches), additional balance is gathered by controlled varying of analog front-end characteristics. The Libera analog RF front-end provides gain setting, signal path rerouting, and acquisition clock frequency modulation .

## SIGNAL CONDITIONING ARCHITECTURE

Figure 1 presents the general approach of the Libera DSC architecture. It is a slow closed loop, in which all analog front-end characteristic changes are compensated for by a DSC feed-forward model (DSC corrector). The system observer tracks and analyzes the deviations between model hypothesis and the current inverse model. The model builder follows the control strategy and corrects the differences in the models. The model server is responsible for the control strategy and implementation of the corrected inverse model into the DSC corrector. In the case of Libera, the control strategy is focused in the balance of the analog front-end. It must provide such characteristic changes in the analog section, which can be easily filtered out of the useful DDC output signal. A faster repetition rate provides wider bandwidth. Symmetry in the duration and amplitude of positive and negative influences provides distortion only at repetition and its harmonic frequencies. An advanced frequency spreading technique enables arbitrary bandwidth. These are sufficient conditions for averaging the characteristic of the signal paths. The most efficient example is gain and crosstalk influence averaging of the four channel amplifier. The signal is symmetrically routed through a different channel with the objective for each of the four filtered signals at the output to have an average amplification and optimal crosstalk reduction. At the same time, the control strategy should provide enough information for the observer. In the case of a phase shift, the model observer must extract information about the phase alignment of attached signals and the phase shift of the particular analog channel. The number of different states must correspond to the aim of the model hypothesis.

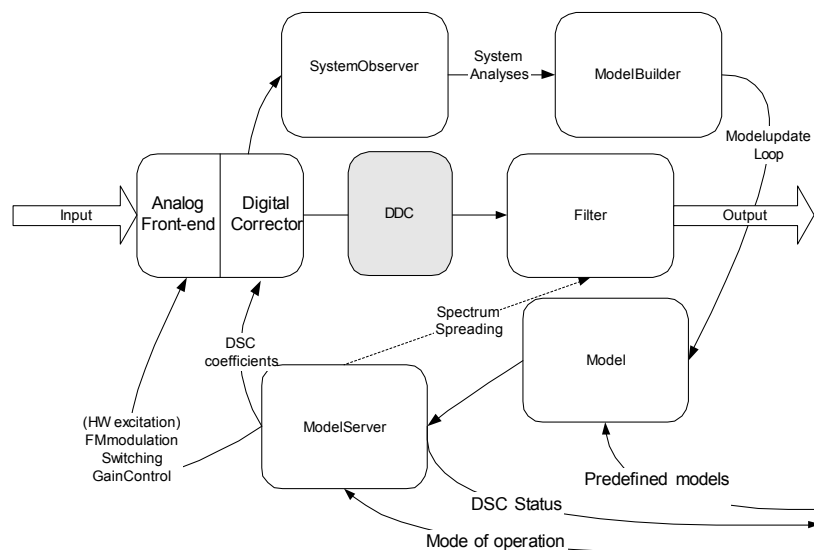


Figure 1: Digital Signal Conditioning Architecture

### Analog Front-end

The analog board consists of a quasi-crossbar switch, four identical RF channels, four analog-to-digital converters, and an interface to the digital board. The innovative patent-pending quasi-crossbar switch unites the benefits of both the multi-channel and the multiplexed system. Specifically, the switch facilitates redirection of any of the four input signals to any of the four RF channels.

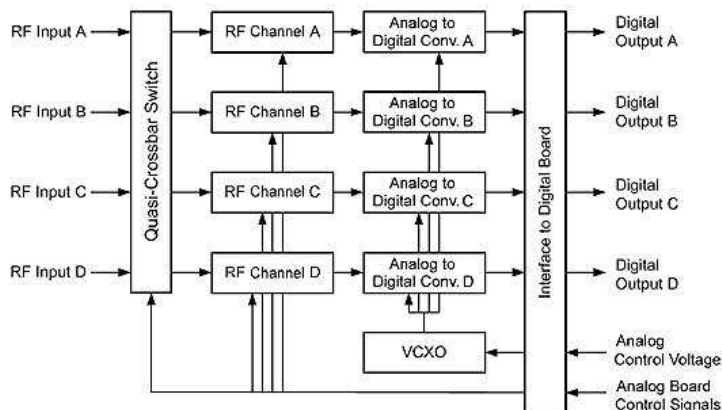


Figure 2: Analog Front-End

### Digital corrector

This is a DSP unit running at acquisition rate. It is implemented in FPGA and represents the highest computational power in Libera. Some of the corrections (phase and gain equalizing) are combined in a common structure. Most of them are filters or coefficient tables with multipliers and adders. It has four identical channels. Correction coefficients are segmented in two pages. The active page provides coefficients for all models, whereas the inactive one can be asynchronously prepared for the next analog front-end state. Page swapping is activated synchronously with every change in the analog front-end. Sub-paging provides synchronous changing of the model at each crossbar switch.

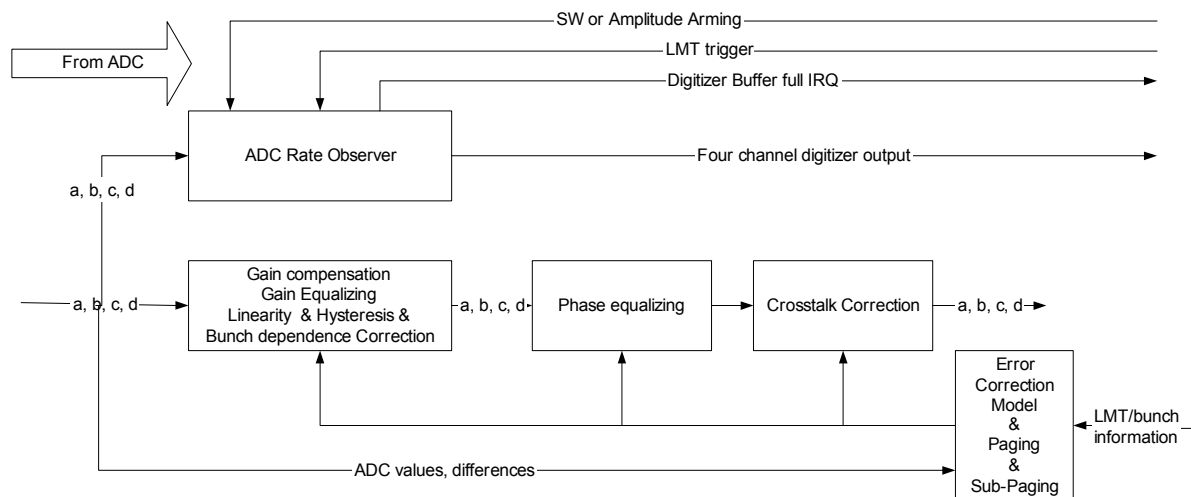


Figure 3: Digital corrector

### *System observer*

This is part of the DSC daemon software running on the Libera Linux SBC. It provides off-line signal analyses retrieved from the circular buffer. The supplemental CB switches information gives several system characteristic reconstruction views in the history data: gain, nonlinearity, hysteresis, and phase channel information. The channel characteristics gathered comply with the previous model and are combined in the new more precise model.

### *Model builder*

This is an expert decision oriented part of the DSC daemon software. The major degree of freedom in the model space represents different gain schemes. In general, at least one model corresponds to each gain scheme. It provides “intelligence” for the modeling. It must decide if the new model satisfies the requirements for renew. The decision is based on statistics. The knowledge decision base is part of the builder. It also marks the new model with new working conditions. It runs statistics for the current model. The model with low STD is a good candidate to be renewed.

### *Model server*

The model server resolves the best choice for the current working conditions. The model server transforms the model into the corrector table format and loads it into the FPGA.

## **CONCLUSION**

We have made analyzes of the DSC concepts for the Libera EBPM. The results of an eight-hour stability test, temperature stability, and BCD test are very promising. The instrument reveals high repeatability, similar and stable characteristics between instruments, and excellent repeatability staying at the same working condition. The tests simulated a crossbar switching method. In the resolution tests, the acquisition clock was locked 1.7 kHz out of the carrier. Simulating the switching method, we gathered sufficient resolution at turn-by-turn frequencies. Resolution in the kHz frequency range is 50% below expectations and will be improved by linearization, hysteresis correction, and potentially through frequency modulated acquisition clock dithering. BCD and bunch dependences must be improved by a factor of three. The crosstalk correction and linearization are the best candidates for such improvements. Off-line modeling of the anomalies produces significant and stable models and expects a high degree of correction. We expect phase alignment for 40dB. The gain equalizing and crosstalk correction will reduce its own ripple in the DDC output from 20 to 30dB. Linearization has not been tested, but promises higher ADC amplitude dynamics and apparently overall improvement.

The DSC project is in the prototype real life implementation phase. The priorities start with phase and gain equalizing and crosstalk cancellation. The preliminary results of the first phase DSC will be presented in the conference poster session.

## **ACKNOWLEDGMENTS**

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