Interfacing Credit Card-sized PCs to Board Level Electronics

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ABSTRACT

In LHCb non-radiation areas the control of electronics boards is implemented interfacing it to a conventional Ethernet network instead than to a proprietary bus (e.g. VME or Fastbus). Small ("credit-card" sized) embedded PCs (Digital-Logic SM520PC SmartModule) provide the necessary local intelligence, interface to the Ethernet network and access to the various components of a board. The access to the board components itself is obtained by means of a special card mounted near the PC as a daughter board on the main board. This card, named "Glue-Card" and described in detail in this paper, provides I^2C and JTAG busses and a simple parallel bus, translated from the PCI bus. The first two are commonly used to configure various chips (e.g. FPGAs) and the latter can be used for fast transfers of large amount of data (e.g. calibration constants).

INTRODUCTION

In LHCb non-radiation areas the control hardware of electronics boards is implemented by means of a conveniently small sized PC, the so called "Credit-Card PC", CC-PC [1][2] (Digital-Logic SM520PC SmartModule [3]), already providing a PCI bus and an Ethernet interface. However, in order that the PC is able to communicate with the board's internal devices, the JTAG and I^2C serial busses as well as a simple parallel bus must be implemented. Thus an interface board to the PC, with the purpose of generating the needed I^2C and JTAG busses and the parallel bus, was devised. This card, called "Glue-Card" [4][5], is mounted on each electronics board as a daughter board near the CC-PC. More specific the Glue Card generates four I^2C channels, three JTAG channels and the Parallel bus, as needed. In addition, it automatically isolates the user electronics from the local bus in case of reset of the PC and it provides a buffered and level compliant RS 232 port to the PC itself. The translation of the PCI bus to a simpler parallel multiplexed bus 32 bits wide, running at a maximum clock speed of 40 MHz, is implemented using the PCI 9030 SMARTarget I/O Accelerator by PLX Technologies [6]. I^2C and JTAG signals are generated by appropriate controllers, which, in turn, are driven by a FPGA connected to the PCI 9030 parallel bus. In fig.1 below a Glue-Card block schematic diagram is depicted.

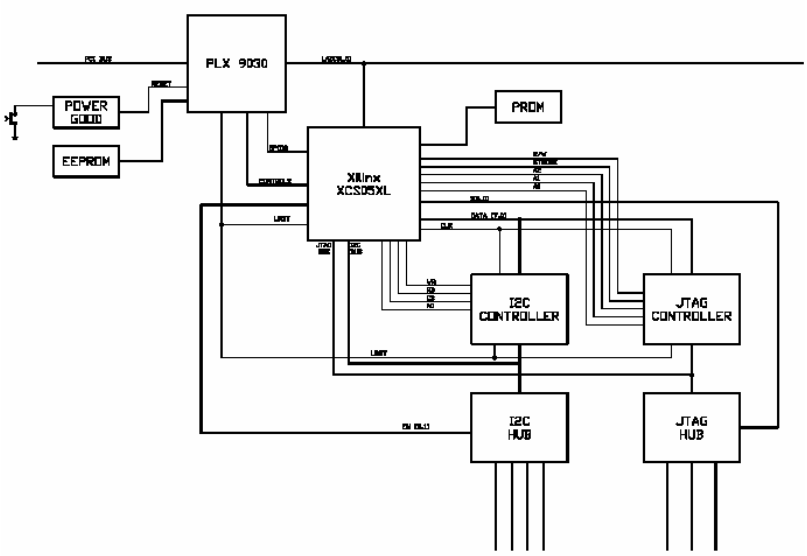

Fig.1 Glue Card block diagram

The dimensions of the Glue Card are 88 x 48.5 mm^2 and schematics of its general layout and photographs of it are represented in fig. 2 and 3.

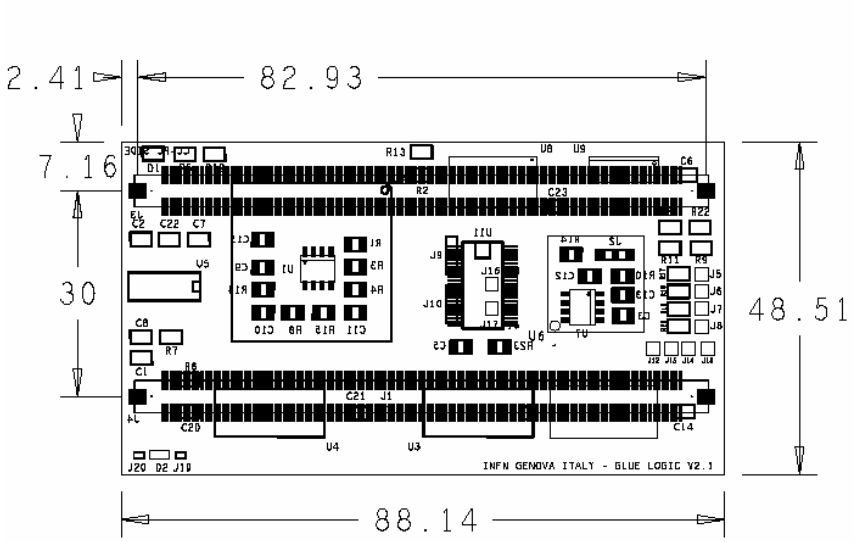

Fig.2 Schematics of the Gluecard with the dimensions in mm indicated

(top view, connectors J3 and J4 seen in transparency)

DETAILED DESCRIPTION

As already mentioned above, the functions performed by the Glue Card in detail are [5]:

1) To translate, by means of the bus accelerator PLX 9030, the PCI bus to a simple 32 bits parallel bus operated in a multiplexed mode.
2) To provide a buffered and level compliant RS 232 port to the Credit-Card PC.
3) To automatically insulate, by means of bus switches put across the parallel bus, the user's electronics from any transient on the PCI bus in case of reset of the Credit-Card PC. The bus switches can also be activated under software control.
4) To provide 4 independent I^2C channels generated by an I^2C controller PCF8584 and fanned out by a hub PCA9516, both circuits are produced by Philips.
5) To provide 3 independent JTAG channels generated by a JTAG controller 74LVT8980 by Texas Instruments and a hub SCANSTA111 by National Semiconductor.

An FPGA (Xilinx XCS05XL) generates the proper signals in order to drive both the I^2C and JTAG controllers. From the user's point of view the FPGA appears as a set of 3 devices resident in address space 0 of the PLX 9030.

1) Enable Register: a R/W register, in charge of controlling the bus switches so to connect / disconnect the Local bus to / from the PCI bus and to enable the I^2C and JTAG controllers.

2) I^2C Controller: consisting in a set of software registers in charge of transmitting the proper commands to the I^2C controller.

3) JTAG Controller: consisting in a set of software registers in charge of transmitting the proper commands to the JTAG controller in the same way as for the I^2C Controller.

The needed 40 MHz clock is provided by the mother board on which both the Glue Card and the "Credit-Card PC" are mounted.

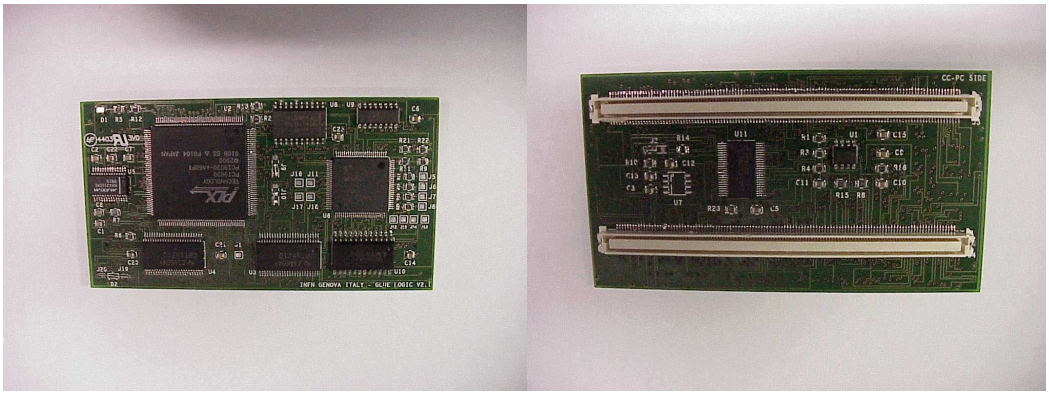

Fig.3 The two sides of the Glue Card with the connectors to the Mother Board

GLUE CARD TEST BOARD

In order to check the functionality of the Glue Card and to have a permanent test system available a Glue Card Test Board was designed. This test board consists of a mother board for both the CC-PC and the Glue Card where a number of devices controlled by the parallel PLX9030 bus, the I^2C bus and JTAG bus are installed. Its Block Diagram is shown in fig.4

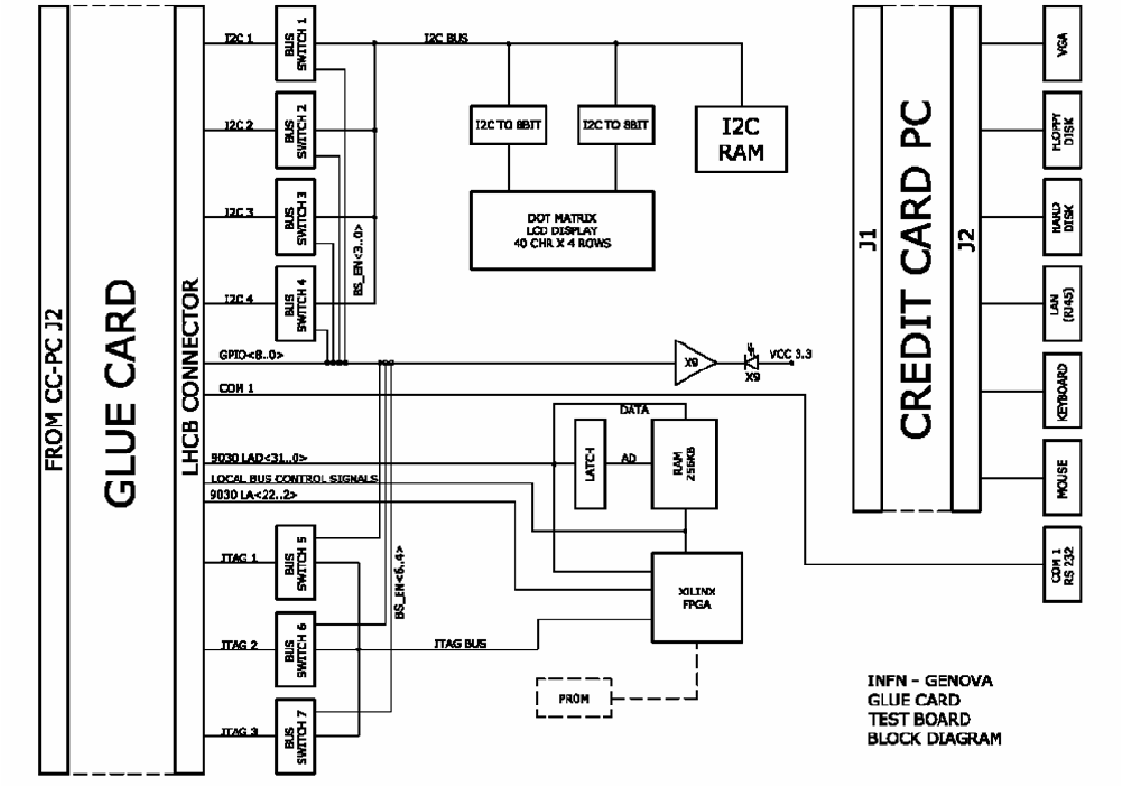

Fig. 4 Glue Card Test Board block diagram

More in detail the PCB of the Glue Card Test Board is in compliance with the ATX standard, i.e. as a PC mother board, and can be assembled in a standard ATX chassis for a PC. The connectors are the same of a standard PC so that it can be connected to standard PC peripherals and power supply. In fig. 4 a block diagram of the Glue Card Test Board is depicted and in fig. 5 a picture of the test board with the "Credit-Card PC" and the Glue Card is shown. An important test feature implemented on the board is a dot matrix LCD display (40x4 cells) which allows the user to test immediately the functionality of the Glue Card's I^2C bus e.g. by writing a message on it. Moreover the I^2C bus can also be tested by writing and reading appropriate I2C memories. Furthermore the JTAG functionality can be tested by programming a Xilinx XCS05XL FPGA of the same type of the mounted on the Glue Card. The same FPGA, once programmed, can be used to check the complete functionality of the PLX9030 Local Bus. Appropriate test programs running under both Windows and Linux have been written.

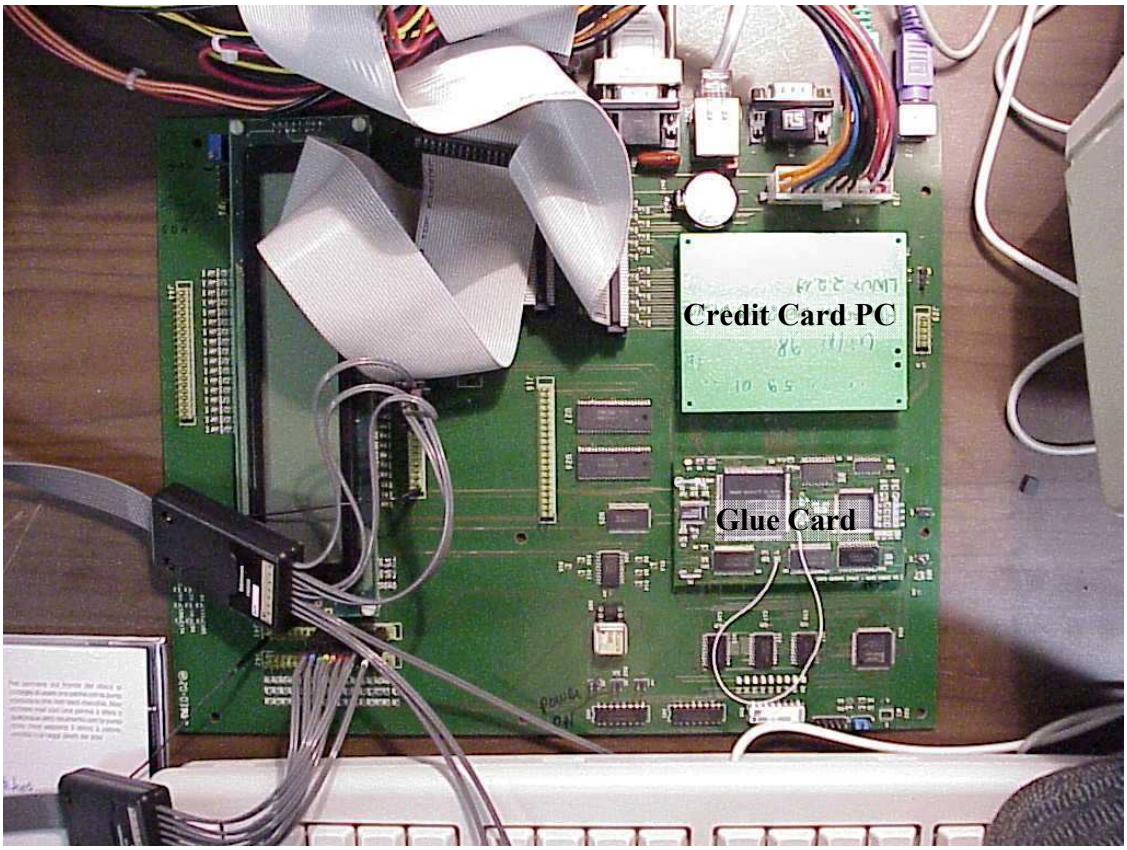

Fig.5 The Glue Card Test Board under bench test. On the left the display for the I^2C bus test can be seen

CONCLUSIONS

The electronic boards in non radiation areas in LHCb are controlled by small ("credit-card" sized) embedded PCs in charge of providing the necessary local intelligence, interface to the Ethernet network and access to the various components of a board. A special "Glue-Card" was devised in order to translate the PCI bus of the Credit-Card PC into JTAG and I^2C serial busses and a simplified 40 MHz parallel bus derived from the PCI bus. These busses are, in fact, used internally in each board. The card also isolates the internal busses from the PCI bus in case of reset of the Credit-Card PC. In order to test the functionality of the Glue Cards, a test board having the characteristics of a ATX mother board was designed and standard test programs have been written.

REFERENCES

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