A DEVELOPMENT OF HIGH-SPEED A/D AND D/A VME BOARDS FOR A LOW LEVEL RF SYSTEM OF SCSS

T.Fukui[1], R.Tanaka[1], T.Ohata[1], Y.Otake[2]
[1]SPring-8, Hyogo 679-5198, Japan, [2]Harima Institute,RIKEN, Hyogo 679-5148, Japan

ABSTRACT

The SPring-8 Compact SASE Source (SCSS) project aims to build an X-ray SASE-FEL. The coherent X-ray generation requests a revolutionary improvement on an accelerator performance. To improve the performance, we developed an A/D and a D/A VME board for high-speed signal control. These are key components for the stable accelerator operations. The boards control the acceleration gradient variation caused by the instability of the klystron output RF power. The A/D board with a down converting mixer and an IQ demodulator was designed for an RF-detector of phase/amplitude signals that are generated with the klystrons. The board is used for the readout of signals from RF beam position monitors as well. An analog-to-digital converter is running at 238MHz clock, which is the sub-harmonic of C-band main acceleration frequency (5712MHz). It has 4Mbytes (2k word * 1k samples) memory for each of four inputs. An effective number of bits (ENOB) and usable dynamic range are better than 10.7bits. In addition, the A/D board has a fault detection capability to compare an observed waveform with a reference waveform stored in the memory. The D/A board is connected to an IQ modulator and an up-converting mixer. It was designed to form the RF modulated phase/amplitude signal to the klystron input. A digital-to-analog converter is running at 238MHz clock, and it has 4MBytes(2k word * 1k samples) memory for each of four outputs. A group delay time is within 0.5nsec, and an ENOB is better than 11bits. The D/A board has 32 taps FIR filters to control a rise time. This paper gives an overview of the low level RF control system, and also describes the function and the performance of the A/D and D/A board.

INTRODUCTION

SCSS project [1][2] aims to build an 8GeV XFEL facility in the SPring-8 site. The X-ray FEL based on the self-amplification of spontaneous emission (SASE) usually requires a large-scale accelerator and a long undulator. It provides a few X-ray beamlines therefore the construction cost per beamline becomes quite higher. One of the most predominant factors on the machine cost is the facility size. To lower the cost, the machine has to be compact. A combination of the short period in-vacuum undulator and the high gradient C-band accelerator makes a machine compact, and it enables the construction site to fit the SPring-8 1km-long beamline space. We developed two high-speed VME boards, i.e. an A/D and a D/A, for a stable accelerator operation [2]. The A/D board with a down converting mixer and an IQ demodulator was designed for an RF-detector of phase/amplitude signals that are generated with the klystron and beam position signals of RF beam position monitor. In addition, the A/D board will be used to measure a beam current with a current transformer. The D/A board is connected to an IQ modulator and an up converting mixer. The board was designed to form the RF modulated phase/amplitude signal for the klystron input.

GENERAL SPECIFICATION

A/D board

The A/D board was designed as 6U VME board with D32/A32 slave interface. An analog-to-digital converter (ADC) is running at 238MHz clock, which is the sub-harmonic of C-band main acceleration frequency (5712MHz). It has 4Mbytes (2k word * 1k samples) memory for each of four inputs. Table 1 shows the specification of the A/D board. We use two analog-to-digital converters, for each channel in a time-interleaved configuration to double the sample rate. A clock is divided by two and

distributed to each ADC channel, 180° out of phase from each other. There are two major factors to consider when designing the input clock circuit: an aperture jitter and harmonic content. The aperture jitter must be less than 1psec (rms) to achieve our requirements, 10.7bit of ENOB (effective number of bits). In addition to the jitter, the harmonic content of single-ended sine wave clock sources must be controlled as well. When using PECL or other square-wave clock sources, unstable behaviour such as overshoot and ringing can affect phase matching and degrade the performance. When two ADCs are time-interleaved, gain and/or phase mismatches between each channel will produce an Image Spurious and an Offset Spurious. These mismatches can be the result of any combination of device tolerance, temperature, and frequency deviations. For example, 0.025% of gain mismatch will cause -70dBc of an Image Spurious for specific condition. The clock input source connects to SMA edge connectors and the analog input source connects to 4-pin LEMO connectors via a 100Ω balanced line cable on a front panel. An FPGA is used for a digital post processing circuit and an output data format is twos complement. There are two ways to read a waveform: a standard mode and an IQ mode. For the IQ mode, a waveform is calculated from IQ component signals to amplitude and a phase. In addition, an FPGA is used for interface to VMEbus. An analog input is AC-coupled and a –3 dB bandwidth of 30 MHz.

Table 1: A/D board specifications

Parameter		
Input channel	4	
Signal level	± 1V	100Ω differential
Resolution	12bits	
Integral non-linearity	±2LSB with no missing code	
Analog input bandwidth	30MHz	
SINAD	-66dBc	
Clock input channel	1	
Clock input level	0 ~ +3dBm	50Ω single-ended
Conversion rate	238MHz	100 ~ 240MHz
Trigger channel	2	
Trigger input level	0.8Vp-p	50Ω single-ended
Trigger cycle	1/60 sec or 1/120 sec	
Waveform memory	4M samples per channel	

D/A board

The D/A board was designed as a 6U VME board with D32/A32 slave interface. A digital-to-analog converter is running at 238MHz clock, which is the sub-harmonic of C-band main acceleration frequency. It has 4Mbytes (2k word * 1k samples) memory for each of four outputs. Table 2 shows the specification of the D/A board. The clock input source connects to SMA edge connectors and the analog output connects to 4-pin LEMO connectors via a 100Ω balanced line cable on the front panel. An FPGA is used for digital signal processing. There are two ways to output a waveform: standard

mode and an IQ mode. For the standard mode, each channel is independent to output. For the IQ mode, a waveform is calculated from the amplitude and the phase of IQ component signals. In addition, an FPGA is used for interface to VMEbus. The analog output bandwidth is a 30 MHz at -3dB. Figure 1 shows the A/D board and D/A board.

Table 2: D/A board Specifications

Parameter		
Input channel	4	
Signal level	± 1V	100Ω differential
Resolution	12bits	
Integral non-linearity	±2LSB with no missing code	
Analog output bandwidth	30MHz	-3dB typ
SINAD	-66dBc	
Clock input channel	1	
Clock input level	0 ~ +3dBm	50Ω single-ended
Input data rate	238MHz	100 ~ 240MHz
Sampling skew	< 1nsec	
Trigger channel	4	
Trigger input level	0.8Vp-p	50Ω single-ended
Trigger cycle	1/60 sec or 1/120 sec	
Waveform memory	4M samples per channel	

FUNCTIONS OF THE A/D BOARD

The A/D board has several functions to fit the SCSS control system.

Trigger Modes

The A/D board has two trigger modes: fixed trigger count and continuous mode. For the fixed trigger count mode, trigger count is set from 1 to 2048, and the data readout stops after the preset number of sampling. For continuous mode, a data buffer is divided by four banks, and the data is written from the first address of the bank (512 samples) as ring buffer.

Sampled Data

The A/D board can be set two sampling point (T_A,T_B) relative to the trigger timing. Each data (V_A,V_B) is sampled and stored into the register with trigger number of waveform. This function is used for sample and hold ADC. In addition to sampled data, the board capable to detect a maximum point (T_C,V_C) and a minimum point (T_D,V_D) with the timing from trigger, then stores them into the register. This function can be used as peak-hold ADC with timing information. Figure 2(a) shows the data

sample scheme.

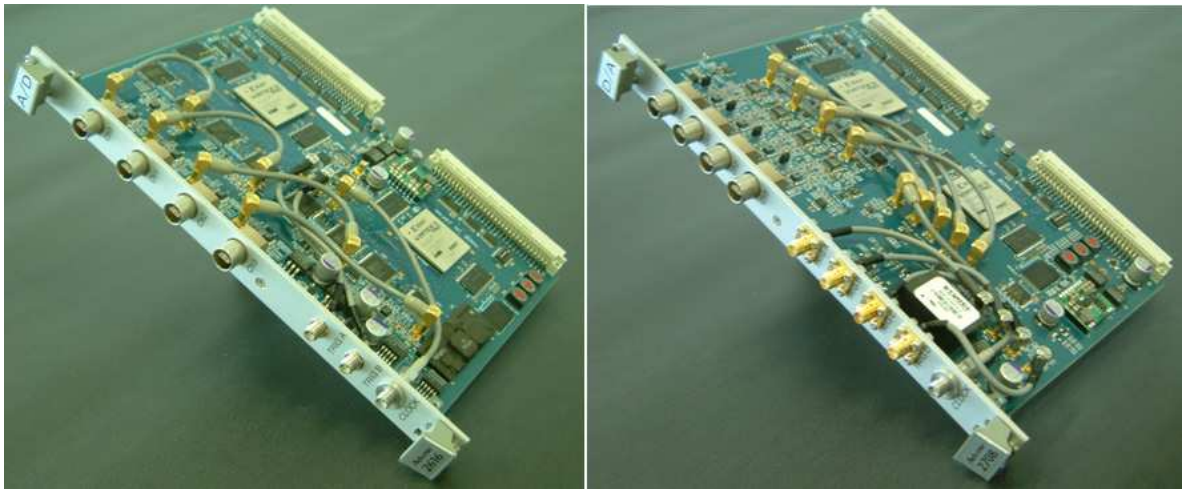

Figure 1: The A/D board (left) and the D/A board (right).

Abnormal Waveform Detection

The A/D board is capable to detect an abnormal waveform by comparing with a reference waveform. When a sampled data exceed the defined tolerance, an interrupt occurs as shown in figure 2b. When it happens, the board switches the data bank to the next bank to preserve the abnormal data for analysis.

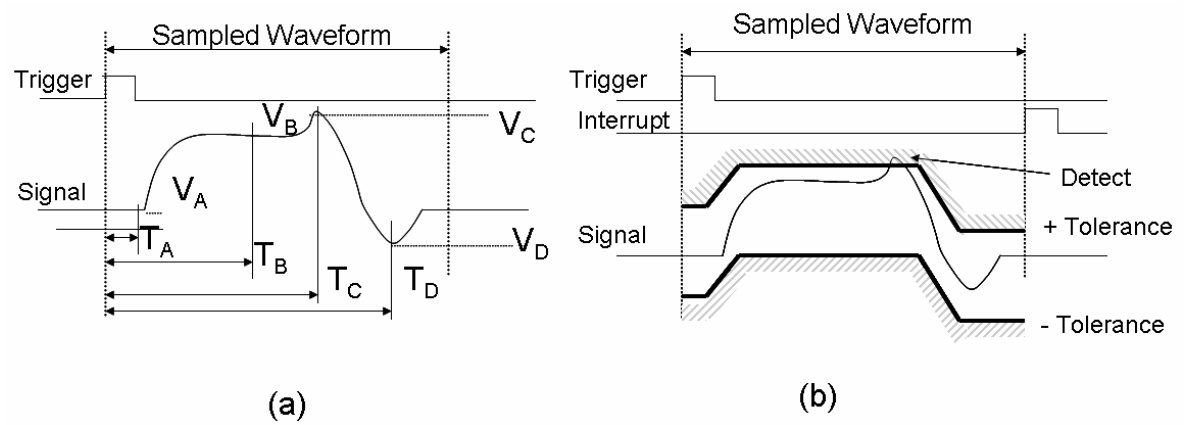

Figure 2: (a) The A/D board sampled data scheme. (b) Abnormal waveform detection scheme.

FUNCTIONS OF THE D/A BOARD

The D/A board has several functions to fit the SCSS control system.

Output Modes

The D/A board has two output modes: a standard mode and an IQ mode. Figure 3 shows block diagrams of D/A board. Each of four channels is independently controlled for the standard mode. A gain register is used to control gain, from 0 to 1.0. A rise time register is used to control rise/fall time with a 32 taps FIR filter. For the IQ mode, amplitude and a phase are used to generate IQ component signals. A phase register instead of gain register for the standard mode is used to control an overall

phase. A phase flip timing register is used to control timing of phase flip which is needed to use a rf-pulse compressor, the peak power is raised 3.5 times higher, of C-band rf-system for SCSS. A rise time register is same function of the standard mode.

Output Timing and Double Pulse

The D/A board capable to change output timing from 0 to 256 clocks. It is use to compensate a difference of a cable length. The board is possible to generate double pulses for warm-up of an rf power amplifier.

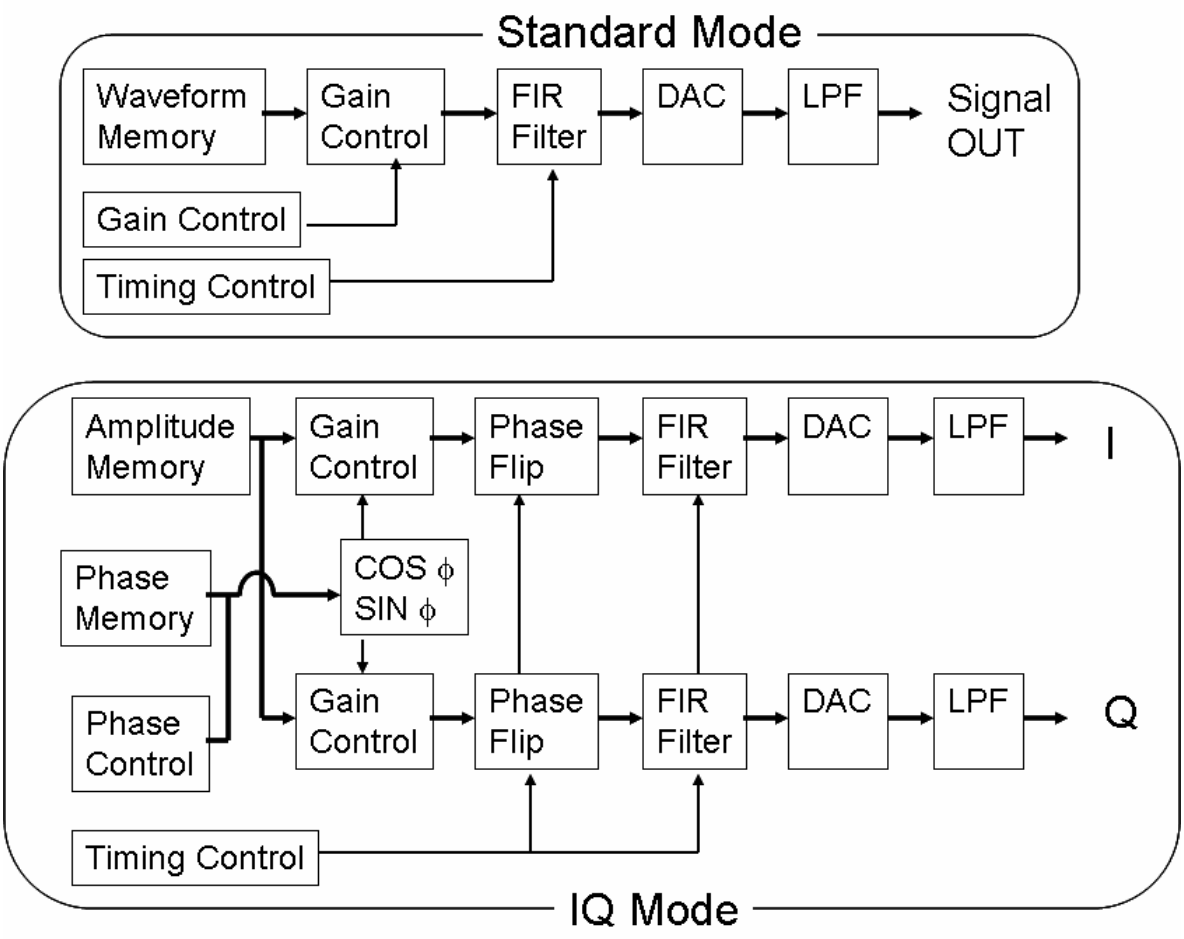

Figure 3: A block diagram of standard mode configuration and IQ mode configuration.

PERFORMANCE

The figure 4 shows a set-up of a performance measurement. The output of the D/A board was fed into an IQ modulator. The IQ modulator was connected to an IQ demodulator directly and output signal of the IQ demodulator was detected by the A/D board. A difference between D/A, A/D board and Vector voltmeter is measured. A deviation of amplitude was less than 0.5% and deviations of phase was less than 0.5 degree. It is enough performance to use C-band rf-system.

SUMMARY

We developed an A/D and a D/A VME board for the high-speed RF-system of SCSS. The boards

are running at 238MHz clock with 12bit resolution. Its performance is good enough to achieve the high quality 8-GeV electron beams with the RF-system, to meet the stable operation of the SCSS C-band accelerator system. The boards will be adapted to the digital feedback system of the RF low-level control.

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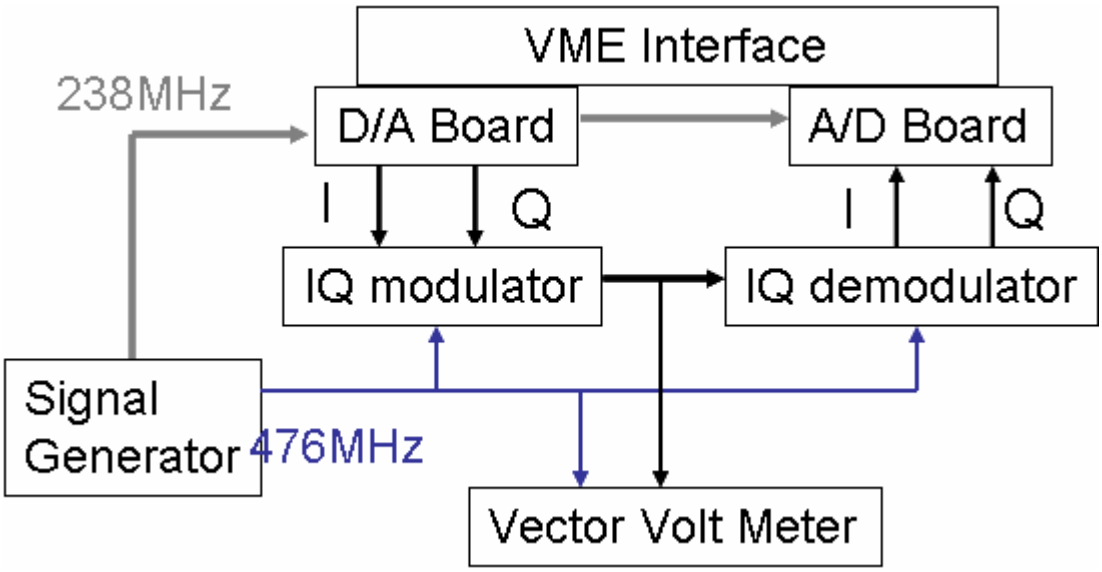

Figure 4: A setup of performance measurement