A NOVEL FPGA-BASED DIGITAL APPROACH TO NEUTRON/γ-RAY PULSE ACQUISITION AND DISCRIMINATION IN SCINTILLATORS

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ABSTRACT

During the last years, extensive experimental work has been carried out by ENEA in the framework of Nuclear Fusion activities, in particular in Frascati Tokamak Upgrade (FTU) and Joint European Torus (JET) tokamaks, to demonstrate the possibility of digitally acquiring the γ-ray and neutron pulses generated in scintillators, separating neutrons from γ-rays and calculating the pulse height spectra (PHS). This has been done using a commercially available high speed (200 MSamples/s, 12-bit) digital acquisition board, equipped with a PC workstation hosting the board and suitable software for acquiring and elaborating data. Although the results have been promising, showing the capability of the post-processing software of correctly separating γ-rays from neutrons and produce the PHS, several limitations have appeared (e.g.: short time acquisition, excessive amount of stored data). Therefore, we have decided to start the design of a new front-end digital acquisition system (200 MSamples/s, 14-bit, FPGA-based), capable of overcoming these limitations and also able to perform on-line signal pre-elaboration and to produce real-time outputs (i.e.: count rates) for feedback purposes. In the article, we will describe the results obtained using the previous system, showing its limits and drawbacks, and the new system, describing its main characteristics and the first tests we have performed.

PROBLEM DESCRIPTION

In neutron measurements for nuclear fusion experiments, organic scintillators (e.g.: NE213) coupled to photomultipliers are normally used to detect γ-rays and neutrons. The slight difference in the pulses generated from the scintillator is used to discriminate between γ-rays (γ) and neutrons (n), see Fig. 1: this is called Pulse Shape Discrimination (PSD).

A typical n/γ PSD method is based on charge comparison: integrating the pulse for two different intervals Δt_F and Δt_S, we obtain respectively the integrals Q_S and Q_F. Since neutron pulses have larger slow components, the ratio Q_S/Q_F identifies, regardless of the pulse amplitude, a neutron or a γ-ray event. In JET, for example, 19 analogue PSD modules are used and they normally operate up to ~200 KHz output count rate [1]. The main drawback of such modules is that they do not allow any kind of data reprocessing, as they do not have any storage capability and therefore it is necessary to take particular care in the hardware set-up of the systems.
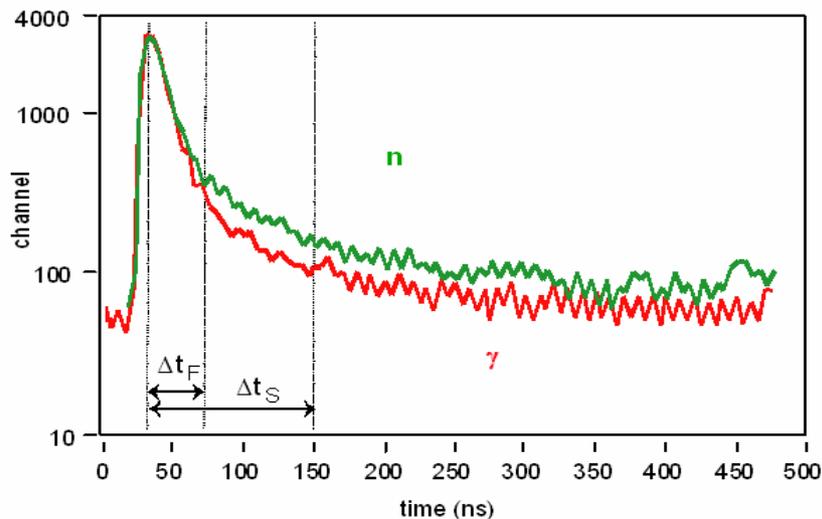
Figure 1: Difference between neutron and γ-ray pulses.

In this article we will show how we have replaced an analogue PSD module with a Digital Pulse Shape Discrimination system (DSPD), which in a first phase was simply a commercial fast analogue to digital (A/D) transient recorder coupled with a personal computer equipped with a suitable software to perform the n/γ discrimination. Due to various limitations of this system, we decided to start the design and development of a new DSPD system, based on a Field Programmable Gate Array (FPGA) and two 100 MSamples/s A/D converter, able to overcome the difficulties and providing data pre-elaboration and real-time capabilities. The article will also describe this new system and its first results.

PAST EXPERIENCE

The first DSPD system we tested on tokamak experiments [1,2] is based on a commercial 200 MSamples/s 12-bit A/D transient recorder PCI board (Strategic Test model UF 3025) which digitizes the scintillator pulses. The board can operate in several modalities, but we used mainly two: the first is to acquire continuously, after a trigger signal, until the 512 MBytes memory board is filled. The second is to acquire a pre-programmed time window each time the signal is over a given threshold.

The first modality is optimal in acquisitions where we do not want to lose any data. As soon as the trigger arrives, the acquisition starts and continues without any interruption until the memory is full. After that, the elaboration software, written in LabVIEW™, performs the n/γ separation and calculates the PHS by integration of the pulses. The main drawback of this method is the insufficient physical memory of the board: it takes about 1.3 s to fill the 512 Mbytes RAM, regardless of the pulse frequency. This is largely inadequate to cover the 30-40 s needed in tokamak experiments like JET.

The second modality is more flexible, due to the fact that we acquire only the triggered pulse signals, taking for each pulse a fixed time window [3,4]. In this way, by choosing the correct number of pre-triggers and post-triggers we can store all pulses for longer time intervals using the 512 MBytes RAM. However, there are limitations also using this technique, the main one being on the hardware side. In order to operate fixed time windows a buffer-mode feature of the board must be used. Once a pre-programmed memory size is filled, data and timing information (a time stamp for each pulse) are sent to the computer memory (via PCI). Unfortunately, during the data transfer no acquisition takes place and, therefore, a temporal gap in the data stream is experienced: in laboratory tests, we measured about 4 ms of lost data each buffer sent (see Figure 2).
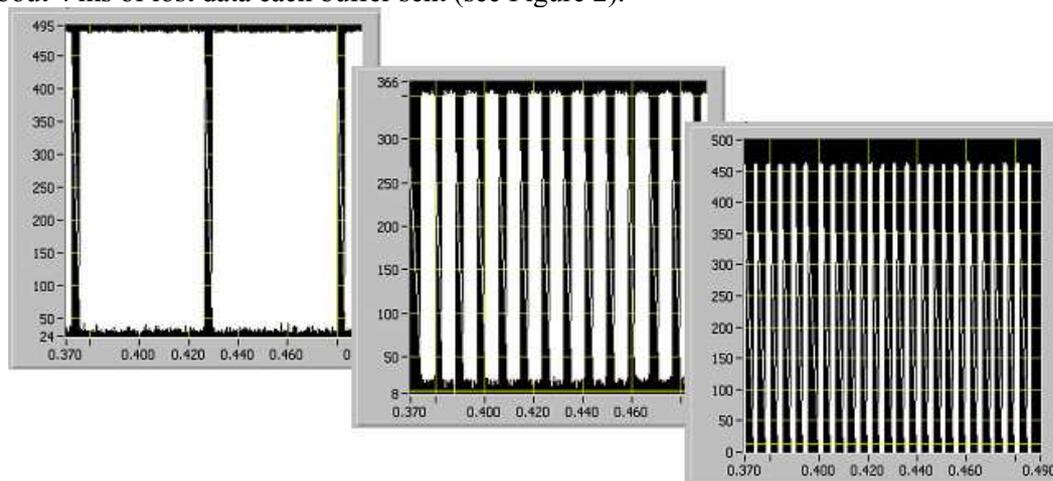
Figure 2: Showing the temporal gap due to the PCI transfer in three cases at different pulse rates (10-100-400 KHz).

This can be acceptable or not, depending on the application. In this case, the total count rate can be obviously given at time resolution > 4 ms. In addition, having a fixed window, also complicates the software analysis in presence of pile-ups (i.e.: multiple or overlapping events in a given window): for example, when a rising pulse in the tail of the window is cut due the fixed time window duration this pulse as well as the subsequent one would be probably rejected.

THE NEW SYSTEM ARCHITECTURE

Our experience with the commercial 12-bit board drove us towards a new system capable of overcoming the limitations discussed above. We decided to find a general solution to the pile-up problem with fixed time windows. The simplest solution we found was to relax the constraint on the length, allowing it to dynamically increase/decrease depending on the pulse shape. This allowed us to reduce at minimum the acquired data per pulse. On the other hand, the acquisition file structure is a little bit more complex than in the previous system, as the actual pulse length plus the time stamp must be stored. With this solution we store only the meaningful data, performing a strong data compression. For example, in case of a pulse rate of 1 MHz, acquiring 32 samples per pulse, we obtain about an 84% data compression. In this way, data can be stored continuously to the PC, because the reduced bandwidth is compatible with the PCI bus throughput. This solved the second problem we had: the temporal gap between data as shown in Figure 2. The general layout of the new system is given in Figure 3.
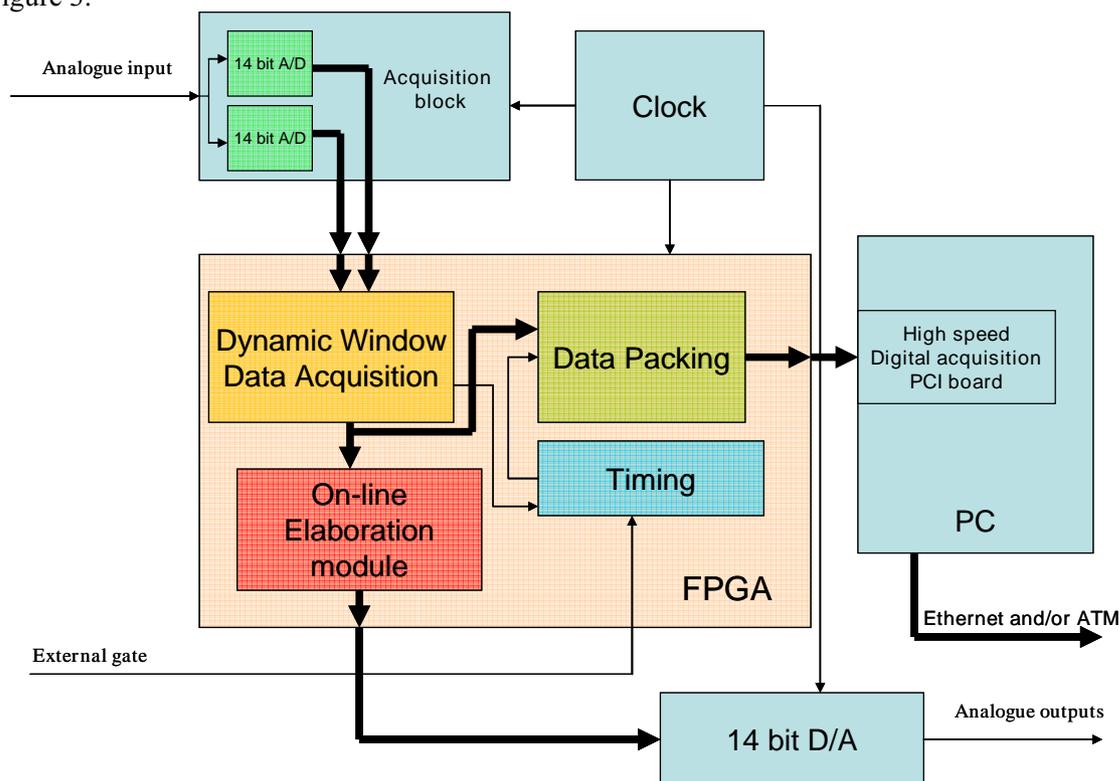
Figure 3. General system architecture.

The analogue signal coming from the photomultiplier is acquired by the 14-bit ADC block. This is a 200 MSamples/s acquisition block and it is formed by two 100 MSamples/s, 14-bit Analog Devices ADC, coupled in interleaved mode. Preliminary results on the prototype have shown for the Signal to Noise Ratio (SNR) and Effective Numbers Of Bits (ENOB) values of about 75 dB and 12.2 bits respectively. This is a good result, because the real values will be certainly better, due to the fact that we did not use a pure sine wave generator with low Noise/Distortion for this measurement. The 14-bit data go to the Dynamic Window Data Acquisition (DWDA). This block acquires a pre-programmed number of samples, unless another pulse arrives during the time window. In this case the length is automatically increased to include the new pulse. This feature can be disabled, returning to the standard fixed length window.

The window data are sent in parallel to two blocks: the On-line Elaboration module performs calculations on the data, as approximate integrals, count rate, etc.; the Data Packing completes the data packet adding the time stamp information to the data.

Finally, the packed data go to the digital acquisition board on the PC which collects and stores data on memory. On the other side, data go to the D/A block from the online side and analogue signal can be used for real-time purposes.

For the prototype, we used an evaluation board mounting an Altera FPGA 1S25, equipped with two D/A 14-bit channel. The digital acquisition board is a National Instrument high speed PCI I/O 6534, allowing a fast continuous bandwidth to the PC memory. The software running on the PC was written in C++, using National Instrument libraries to access the PCI digital I/O board. It manages the initial board parameter set-up (e.g.: buffer length) and acquires the blocks arriving from the board as soon as they are ready.

The board operates in First In-First Out (FIFO) mode. When half buffer is full it is sent to the PC via the PCI bus, while the board continues data acquisition in the second half buffer. In this operational mode no data are lost, up to a total throughput of 80 MBytes/s. After the acquisition is finished, data are written on disk in the correct format, containing, for each pulse, the time stamp data, the pulse length and all the pulse samples. A parallel software module is under study to perform on-line data elaboration, in order to calculate relevant quantities to be sent digitally to a real time control system.

FIRST RESULTS

A LabVIEW™ program has been written for post-acquisition data elaboration and analysis (Figure 4). Starting from the stream of acquired and formatted data, the software performs the analysis as follows: each single pulse above a preset threshold is selected and two outputs are produced according to whether *single* or *pile-up* pulses are identified in any time window. *Pile-up* events are defined as multiple or overlapping pulses above threshold in any given time window. Single events are further processed for n/γ separation and PHS analysis.

Figure 4. LabVIEW™ program.

The total count rate is produced (sum of *pile-up* plus *single* pulses), as well as, separately, *single*, neutron and γ-ray count rates. The n/γ separation is performed, as described above, using Q_S = 25 ns and Q_F = 120 ns, starting from the peak of each pulse: a graphical output is produced (Figure 5) and the separation line can be adjusted in order to reach the best separation according to the experimental conditions. The PHS analysis (Figure 6) is performed by digital integration of the single pulses over their full time window. It has been found that the pulse baseline determination is crucial for the achievement of the best energy resolution in the PHS: the software is capable of determining the baseline for each single pulse.

Figure 5: Graphical output of n/γ separation algorithm.

Total count rates up to ~1 MHz have been handled in laboratory tests with a periodic pulse generator, using time windows of 32 samples. The system has also been preliminarily tested in experimental conditions with γ-ray calibration sources as well as 2.5 and 14 MeV neutron sources showing good overall performance. Using a minimum of 96 samples per time window, count rates over 240 kHz have been handled without problems in 14 MeV operation. Figures 5 and 6 refer to 2.5 MeV operation.
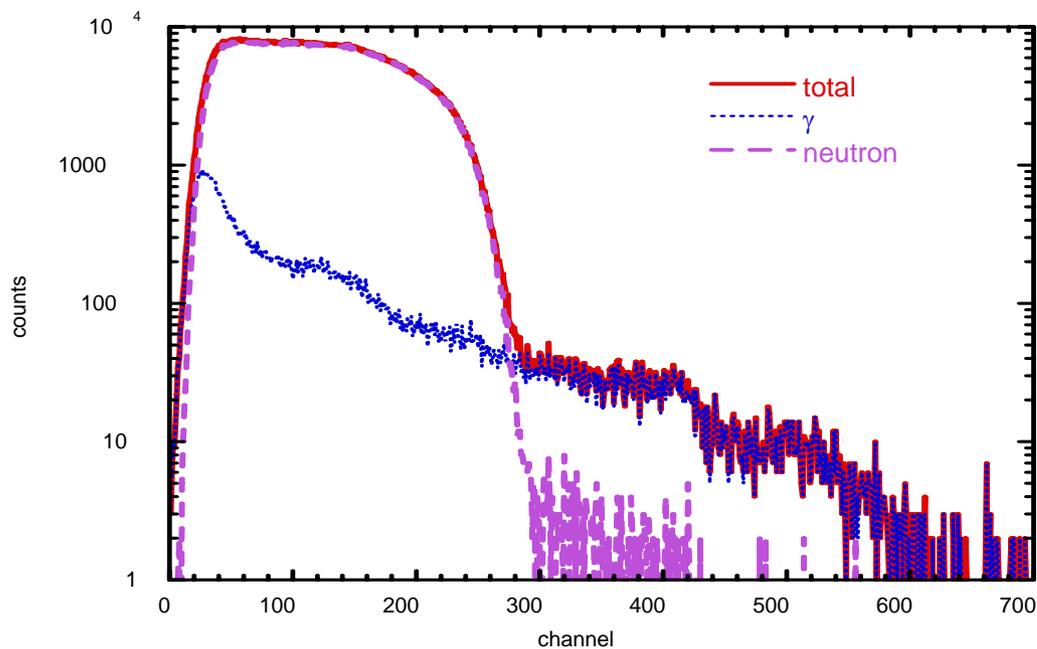
Figure 6: Result of PHS analysis.

CONCLUSIONS AND PLANNED WORK

In this paper, we presented a new FPGA-based approach to the digital acquisition of neutron and γ-ray pulses coming from scintillators (the same approach can be obviously used in any other application with similar pulse characteristics). We called it Dynamic Windows Data Acquisition (DWDA). It allows acquisition of any pulse type without pulse truncation due to fixed length window. The first tests showed promising results. We are currently working on a new version of the system in which we will remove the high speed PCI fast digital acquisition board and will introduce several optimisations, in order to simplify the system and have a cost reduction. Another improvement under study is a series of on-line algorithms to make various signals available for real time control purposes.

ACKNOWLEDGEMENTS

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