SYNCHRONOUS RAMPING SCHEME FOR SRS INDUS-2

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ABSTRACT

Beam energy ramping in Synchrotron Radiation Sources (SRS) requires synchronous increase in power supply currents attached to various magnets. This paper describes the control system scheme to perform ramping in INDUS-2.

INTRUDUCTION

Indus-2 is a 2.5 GeV SRS under construction at Centre For Advanced Technology (CAT). This has a 450/700 MeV Booster as the beam injection source. The beam in Indus-2 SRS has to be ramped to energy of 2.5 GeV from injection energy.

Ramping the beam energy requires ramping of magnetic fields in Dipole (DP), Quadruple (QP), Sextuple (SP), Horizontal and Vertical steering magnets (HS, VS) and the Radio Frequency (RF) source. The beam optics and tune may shift during the beam energy ramping. Thus the beam acceleration has to be programmed in such a way that the beam survives. The increase in the field value of various magnets has to be synchronized for this purpose.

REQUIREMENTS

Based on the studies and the discussions with Beam Dynamics group, following requirements are found necessary:

- Synchronously increase the current of a group of power supplies that are set to ramping mode.
- Allow the user to select the rate of current increase and selectively stop in-between.

The ramping current curve in different power supplies depend on many factors:

1. Non-linear relationship of the current to magnetic field of the magnets.
2. Inter-relationship between different magnets e.g. Dipole-Quadruple.
3. Effect of field due to main coil on the field set by the secondary coil on Dipole magnets.

THE SCHEME

Energy ramping can be considered as a process in which the beam energy is changed from initial energy 'E_1' to final energy 'E_N' in '*N*' steps say

$$E_1,\ E_2,\ E_3,\ E_4,\ \ldots\ E_N$$

Considering that the accelerator machine (the ring) is composed of 'm' number of magnets whose corresponding field values for a particular energy 'E_i' are given by

$$_{Ei}B_1,\ _{Ei}B_2,\ _{Ei}B_3,\ _{Ei}B_4\ \ \ldots\ \ _{Ei}B_m$$

The corresponding magnet power supplies currents are given by

$$_{Ei}I_1,\ _{Ei}I_2,\ _{Ei}I_3,\ _{Ei}I_4\ \ \ldots\ \ _{Ei}I_m$$

So to achieve beam energy 'E_1' required fields in various magnets can be denoted by

$$_{E1}B_1,\ _{E1}B_2,\ _{E1}B_3,\ _{E1}B_4\ \ \ldots\ \ _{E1}B_m$$

and the corresponding currents are represented as

$$_{E1}I_1,\ _{E1}I_2,\ _{E1}I_3,\ _{E1}I_4\ \ \ldots\ \ _{E1}I_m.$$

Similarly, for beam energy value 'E_2', the field & currents may be expressed by

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$_{E2}B_1$, $_{E2}B_2$, $_{E2}B_3$, $_{E2}B_4$ ... $_{E2}B_m$

$_{E2}I_1$, $_{E2}I_2$, $_{E2}I_3$ ... $_{E2}I_m$ and so on.

All these values can be put in a table-1, given below.

Table 1: Beam Energy and Power supply currents

Energy	PS1	PS2	PS3	…	PSj	…	PSm
E_1	$_{E1}I_1$	$_{E1}I_2$	$_{E1}I_3$	…	$_{E1}I_j$	…	$_{E1}I_m$
E_2	$_{E2}I_1$	$_{E2}I_2$	$_{E2}I_3$	…	$_{E2}I_j$	…	$_{E2}I_m$
E_3	$_{E3}I_1$	$_{E3}I_2$	$_{E3}I_3$	…	$_{E3}I_j$	…	$_{E3}I_m$
…	…	…	…	…	…	…	…
E_i	$_{Ei}I_1$	$_{Ei}I_2$	$_{Ei}I_3$	…	$_{Ei}I_j$	…	$_{Ei}I_m$
E_{i+1}	$_{Ei+1}I_1$	$_{Ei+1}I_2$	$_{Ei+1}I_3$	…	$_{Ei+1}I_j$	…	$_{Ei+1}I_m$
…	…	…	…	…	…	…	…
E_N	$_{EN}I_1$	$_{EN}I_2$	$_{EN}I_3$	…	$_{EN}I_j$	…	$_{EN}I_m$

A particular row i of the above table represent the values of current to be set synchronously in corresponding power supplies to get beam energy 'E_i'. Going from one row to another row to get a corresponding energy 'E_{i+1}', requires changing current settings in all power supplies as given in the next row i+1.

In the above table, a particular column j, represents the array containing various current values to be set for a particular power supply for various beam energies E_1, E_2, E_3, E_4, … E_N. Each individual 'array' is in-fact stored in the memory buffer of the DAC board interfaced to that power supply.

So, the ramping process can be seen as setting simultaneously the k^{th} values ($1<k \leq N$) of each 'array' (column) on the respective power supply, thus arriving to a new state with higher beam energy while keeping the identical optics. The synchronicity of setting guarantees the transition to the next state without any undesirable deviation in the beam optics.

Again, the power supply current for a particular power supply from k^{th} value to $(k+1)^{th}$ value of the 'array' is reached linearly in small increments depending on the required fine control. Let us call the array values shown in above table as 'samples' and the linear small increments between two samples as 'steps'. This is shown in figure-1.

The limit of fine control 'step value' will depend on the resolution of the control hardware and the power supply. As far as control system is concerned, the 'step value' will be in multiple of Least Significant Bits (LSBs).

While going from one energy level 'E_i' to 'E_{i+1}' all these small steps are set synchronously on respective power supplies with the best possible resolution.

CONTROL SYSTEM

The INDUS–2 control system is based on a three-layer architecture namely the 'User Interface Layer' (UI), the 'Supervisory Controller Layer' (SC) and the 'Equipment Controller Layer' (EC) [1].

VME bus based modular ECs house a special Digital to Analog Converter (DAC) boards having 16-bit resolution. A 64 K word memory buffer is provided on these boards to implement the above ramping scheme. The 'sample value array', given by the user is interpolated linearly by CPU of EIU to get the 'steps array'. This steps array is stored in the memory buffer of the DAC card. The 'steps arrays' for all the power supplies required to be ramped are stored in memory buffers of corresponding DAC boards [2]. The number of elements in steps arrays of all the ramping power supplies must be same between two 'sample' values.

All j^{th} elements of such step arrays are set synchronously to DAC, which in turn generate the required analog reference voltage which is given to corresponding power supplies.

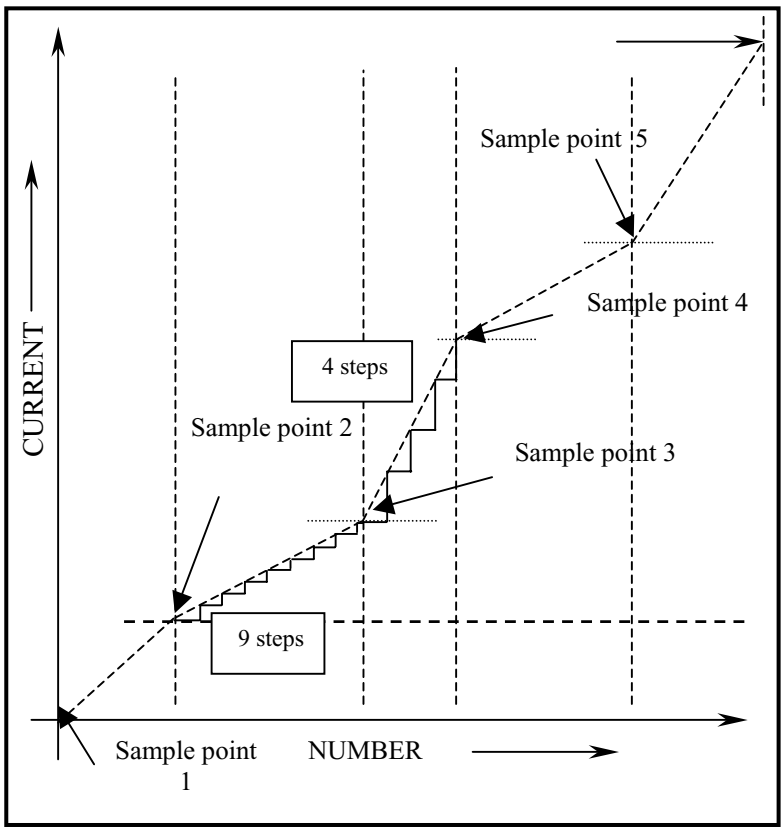

Figure 1: Samples and Steps

SYNCHRONISATION SYSTEM

The synchronicity among the increments of references to all power supplies is achieved by outputting the data (steps) from memory buffers of DAC boards following an external clock common to all DAC boards.

- A custom made VME bus compatible programmable clock generator and driver board (CG) sitting at SC layer generates this synchronization clock. This can provide a programmable number of clock pulses and programmable pulse frequency. This board has following features: Programmable pulse frequency range from 1MHz to 1 mili Hz.
- Outputs programmable number of clock pulses (1 to 65535) with the programmed frequency.
- Two independent output channels with auto switching mode.
- Multiple sets of frequencies and number of pulses can be output sequentially in interrupt mode.
- The clock pulse output can be paused/resumed and stopped with software.
- Read back of current pulse count.

The clock from this board is distributed in the field (~800 meter) to all the DAC boards housed in various ECs. The delay measured is less than 2 microseconds between the extreme ends.

OPERATION AND USER INTERFACE

The total system operation comprises of three steps-

1. The user inputs the sample values from the UI layer using a user interface. This interface looks like a spreadsheet (figure 2). The number of samples can be typically few tens but even few hundreds can be given. This depends on the current to magnetic field (I-B) relationship of the magnets.
2. These samples are stored on the corresponding CPU boards of the ECs. A program running on the CPU then interpolates these sample values to get the step array and store them in the memory buffer of the corresponding DAC boards.

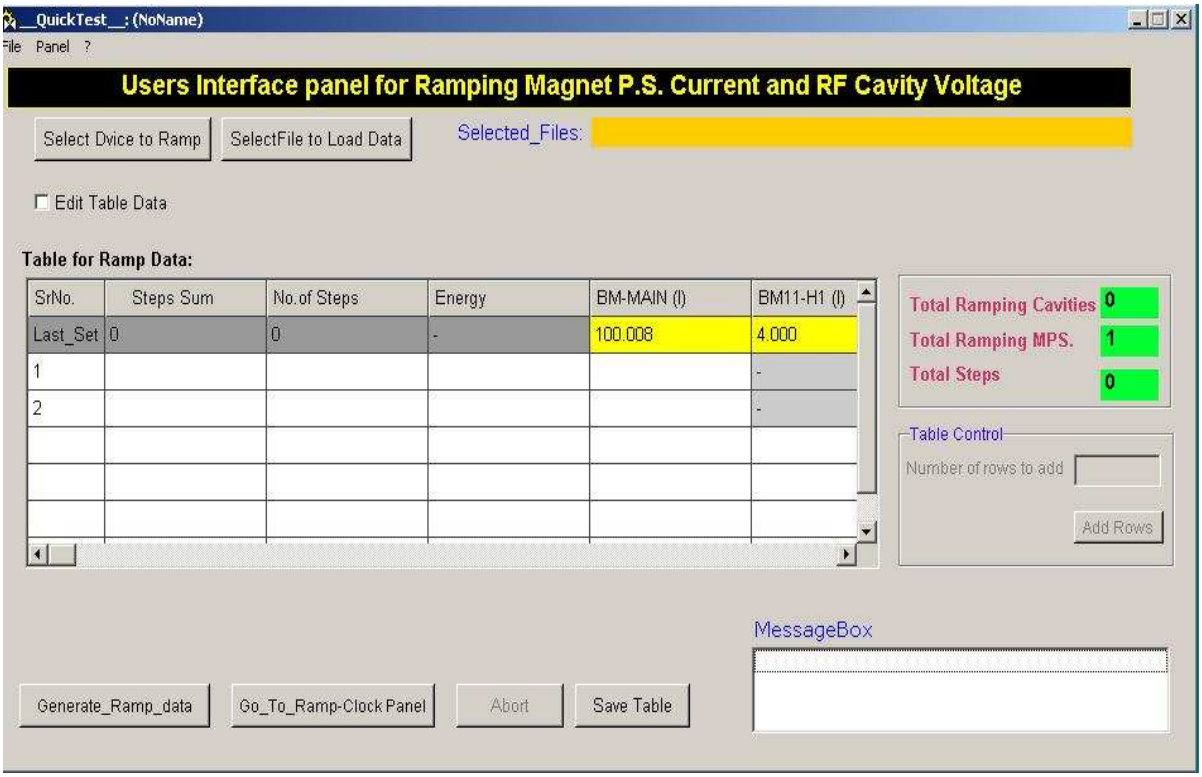

Figure 2: Ramp Data Panel

3. When all the ECs complete this interpolation operation, the user interface program allows the user to go to the Ramp Clock Generator window (figure 3). This window basically communicates to SC layer CPU housing the CG. The user can enter number of pulses, frequency and then start the ramping. He can pause, resume, stop and change number of pulses & frequency and again start the ramping.

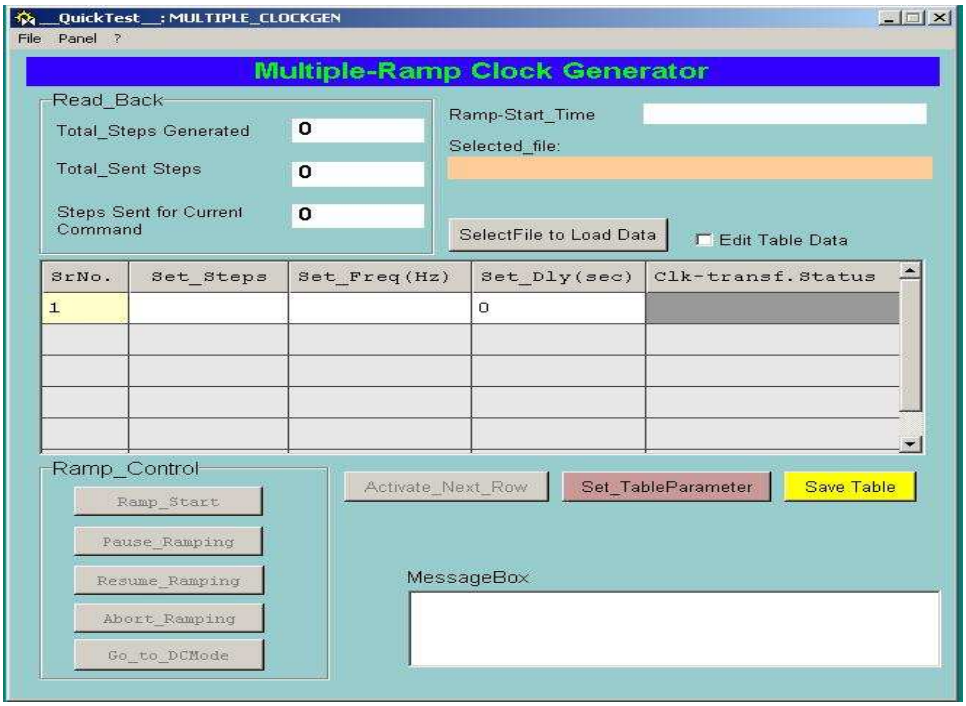

Figure 3: Ramp Clock Generation Panel

CONCLUSION

The above ramping scheme is quite robust and general in nature. This scheme decouples the ramp data and timing information and allows user to select the ramping slope as required. It is also capable to cater the negative slope as required in dipole secondary coils and steering coils. We hope that it would cater to the complex and changeable requirements usually found in the accelerator field.

REFERENCES

[1] P. Fatnani et al, "INDUS-2 control system," PCaPAC'99, Tskuba, Japan.
[2] M. Seema et al, "Magnet Power Supply Control System for INDUS-2," InPAC'2003, Indore, India.