A Versatile Carrier Board and Associated Timer Module Applications

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ABSTRACT

Because of a need for fast prototyping due to frequent upgrades and a large variety of users at the Jefferson Lab Free Electron Laser Facility (FEL), a 4-slot carrier board was designed along the lines of the Industry Pack carriers, with a 6U4HP form factor. In one slot is an Altera Field Programmable Gate Array (FPGA) which communicates with an Experimental Physics and Industrial Control Software (EPICS) interface through the main bus, in the immediate case VME, but potentially PCI and others. The FPGA also provides 64 bits of digital i/o and communicates with a local bus that covers the other 3 slots. In these 3 slots may be placed a variety of daughter boards that may be of a size to span 1, 2 or even all 3 spare slots, depending on the job it has to do. Among the uses implemented in the FEL were a simple digital i/o board (only the first slot occupied), and a timer module occupying 2 slots. The latter has four independently programmable outputs, where each output is a two-variable function of the common event trigger input. The first variable is a delay time after the trigger and the second a duration. All four outputs can be made synchronous to an externally provided master timing reference signal (optionally used). Resolution can range from 50ns (5ms max delay) to 50ms (100 min. max delay) on each channel independently. This paper will describe the design, rationale and operation of the carrier board and timing module. Other daughter boards planned or already implemented are a Drive Laser Pulse Controller; track and hold for optical beam position monitors; analog and digital distribution modules; a digital relay module; and a fiber driver.

HARDWARE

Carrier Board Layout

The layout of the Carrier board is shown in Figure 1. The design was developed with maximum configurability as a priority. It begins with a simple dual 16-line i/o module, to which is added two 16-line buses for communication with up to three other possible modules. If this communication is not needed, the bus lines can be configured as additional i/o lines. The i/o and bus lines on both sides are brought out to 40-pin ___ connectors, with 32 pins used for signals, and 8 for power/ ground. The latter pins allow for a variety of the voltage levels that are typically needed for instrumentation and control. The Carrier Board is packaged as a standard height, single wide (6U4HP format) VME card.

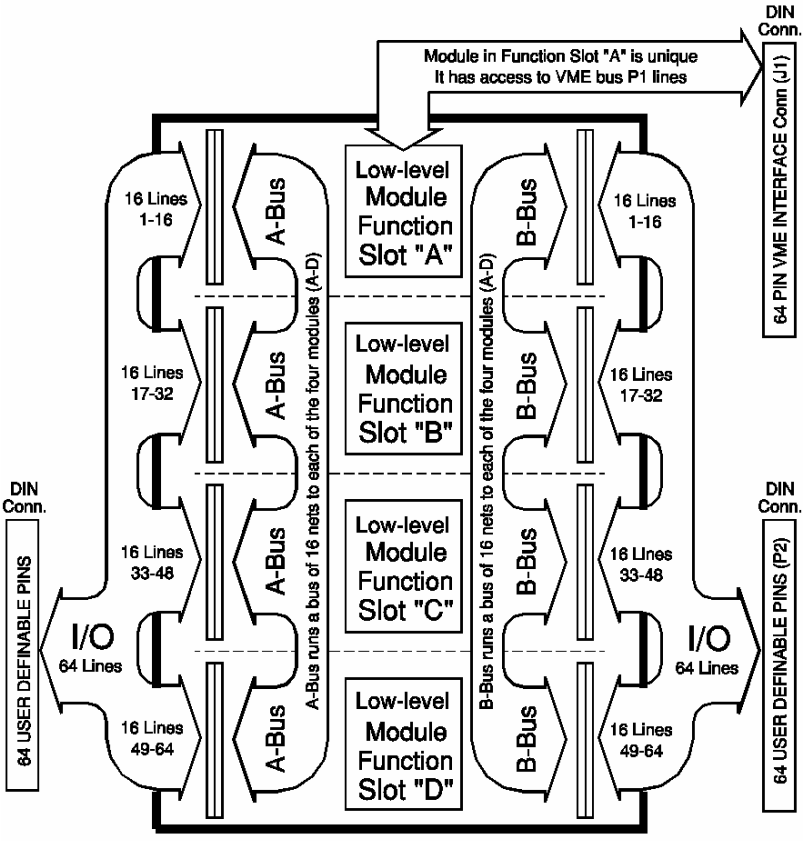

Figure 1: Block Diagram of the 6U General Purpose Carrier Card

The first module in slot A of the card will generally be an

intelligent board that interfaces to the primary VME (or potentially PCI) bus through the P1 connector, with all transfers being 16-bit words. The logic for this has been put in an Altera PLD. The other two 64-pin DIN connectors are user definable. By jumpering the buses as i/o lines, this interface module can, in the simplest case, be turned into a 64 bit digital i/o board without using any other module slots on the Carrier board. If 128-bit digital i/o is needed, the bus must be utilized as a bus, communicating with three additional low-level modules in slots B-D. The interface module then handles signals through the P1 connector, passes i/o signals through its own dual 16 i/o lines, and, via one of the buses, controls the three low level modules. These in turn handle converting the bus signals and passing them through their own dual 16 i/o lines.

Timer Board Description

An overview of the layout and functionality of the 4-channel Programmable Timing Module is shown in Figure 2. This card utilizes three of the four carrier slots. The first handles the VME interface, but also handles clock and trigger distribution, global parameters, and the passing of specific timing commands to the four channel timers. Both internal (40 MHz) and external clocking

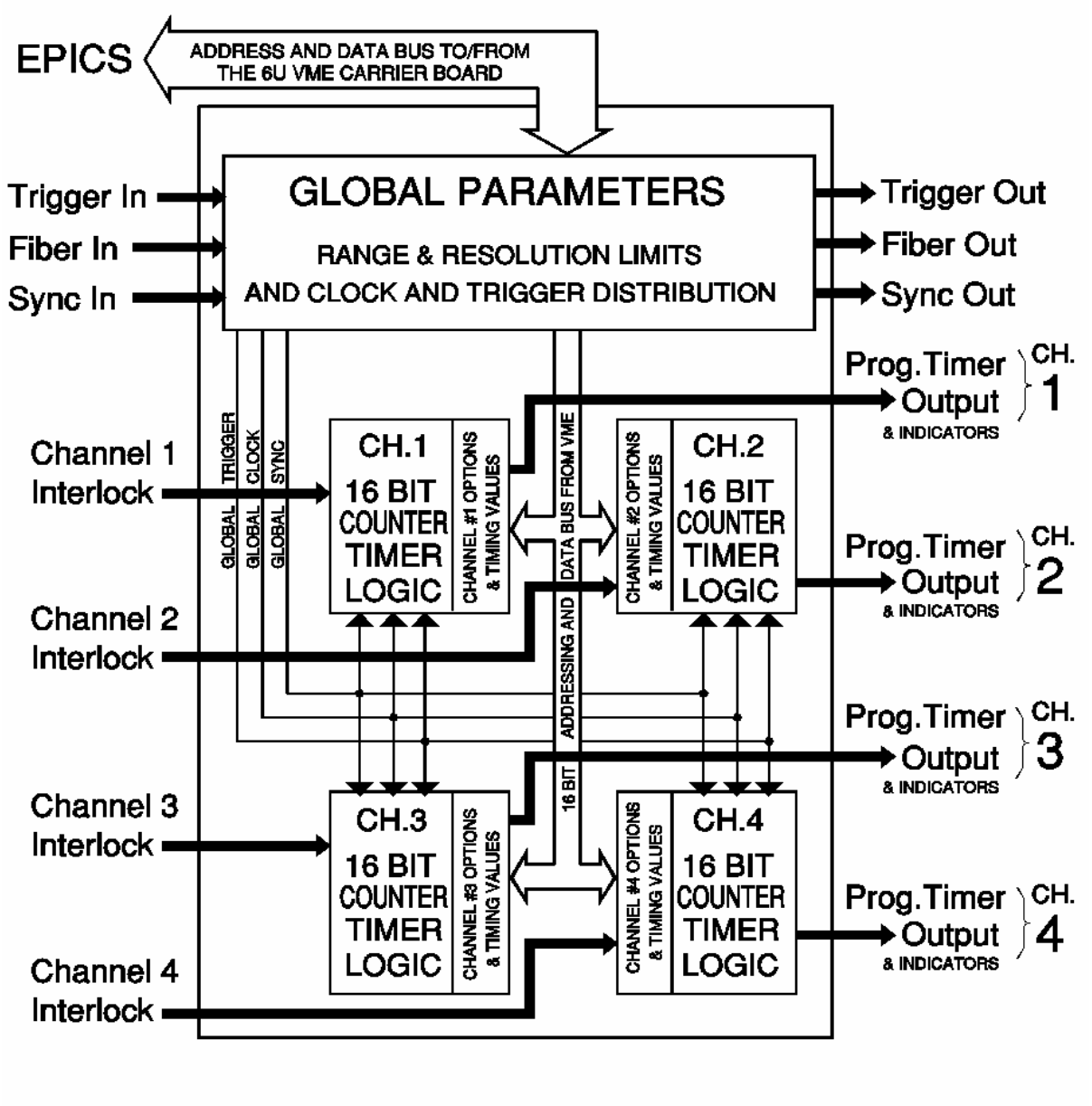

Figure 2: Block Diagram of the 4 Channel Programmable Timer Module

options are provided, as well as fiber inputs. The channel timers occupy the next two slots and provide a square wave output with programmable frequency, delay and pulse width. These and other output options are sent to the channel timers via the 16-bit local bus. This is accomplished as follows. The high-level (EPICS) software talks to the timer board strictly through the i/o pins on the interface module. The latter interprets these signals and sets the bus lines accordingly. Three of the bus lines provide an address (channel number), three more tell the module which of 8 possible commands is being sent, two are read/ write and strobe lines, and the last 8 comprise a data byte. The clock timing itself is passed to the channels strictly through hardware and causes incrementing of 16-bit counters on each channel. Using the internal 40 MHz clock, frequency dividers from 2 to 512 on both the global and channel timing allow resolution to range from 50ns (5ms max delay) to 50ms (100 min. max delay) on each channel independently. Interlock dongles are used to inhibit the output of individual channels independent of any software control. Although intended for machine protection purposes, they can also be used for gating of the timer outputs.

SOFTWARE

As mentioned, external control of this card is generally through EPICS [1] software communicating on the VME bus. Up to three layers of software were developed to make it easy to develop new applications and multiple instances of a single application. At the lowest level is the driver for the 64-bit i/o and VME interface module. This driver simply sets or reads the appropriate bit from the VME memory map whenever the corresponding EPICS signal is processed. For control bits this processing could occur whenever a user presses a control bit button on a screen, or it might perhaps be automatically triggered in software whenever certain conditions are present; for read back bits, it generally occurs automatically, say once or twice a second. The driver itself always reads or writes 16 bits, and masks out all but the data bit that is connected to the signal being processed, the bit to signal mapping being specified in an easily changed table. The generic control/ diagnostic screen for a single 64-bit i/o card is shown in Figure 3. Any of the individual bits can be toggled and their hardware read back is displayed, providing a simple diagnostic tool. In the event other software is controlling the bits, a software switch allows this non-manual control to be disabled during troubleshooting. About 30 such screens are currently in use at the FEL, and a new one can be created in just a few minutes. Software for the new screen is also a matter of just launching new instances of the basic program.

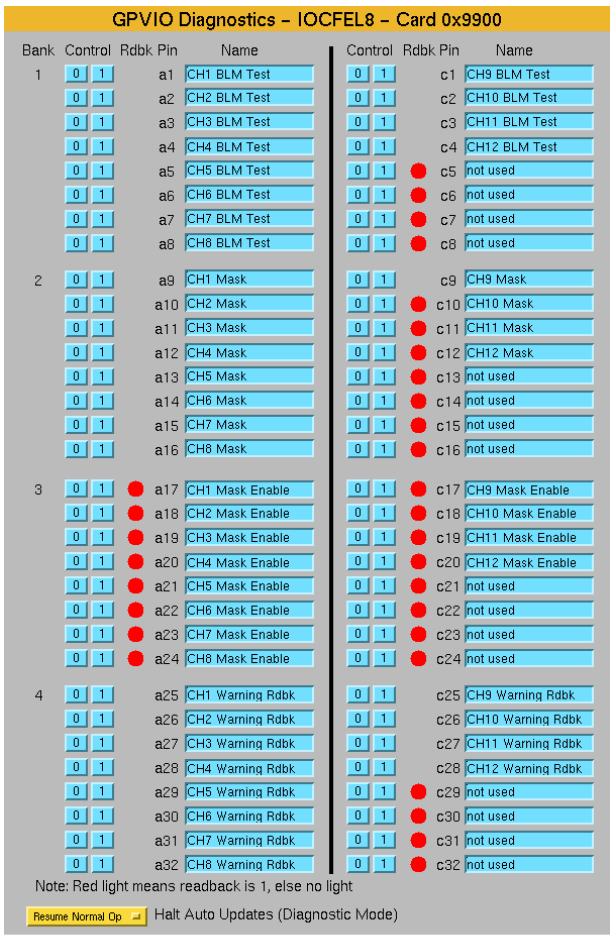

Figure 3: GPIO Diagnostics EPICS screen

The second layer of software is specific to the application. If only the i/o bits are used in the application and if a group of n bits is used to control/ monitor a hardware device, then a layer of signals is created for the device, and these are locked to the bits in the first layer. The names of the second layer of signals are physically meaningful for the device, as opposed to just being a bit number in the first raw layer of signals. This allows software and screens for multiple instances of the device to be easily created. In the case of the timer card application, the mapping is more complicated, in that a group of bits may hold a delay value or frequency, but the principle is the same. Generic screens for this card are shown in Figures 4, the first

showing global parameters that apply to all timer channels, and the second showing the parameters and options for one of the four identical timer channels.

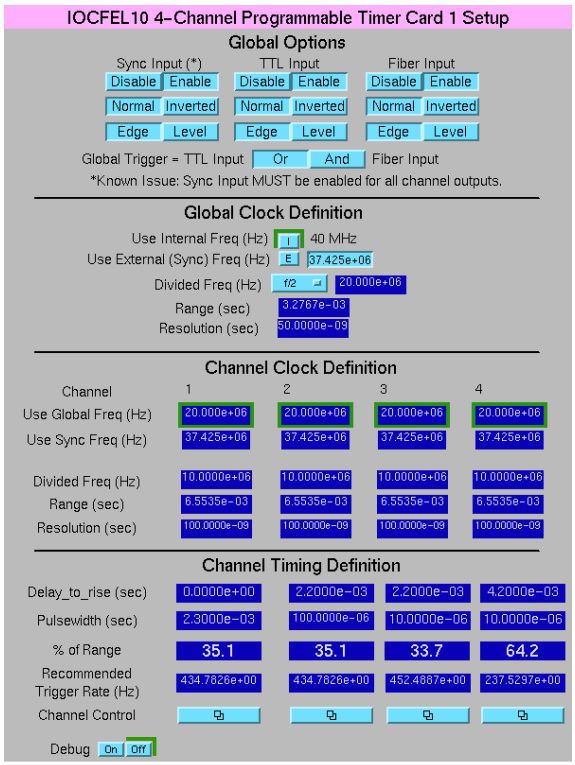

Figure 4: Timer Board Global Parameters

A third layer of software can be developed when one or more timer cards are used to control a specific hardware device. An example of this at the FEL is the Drive Laser Pulse Selection System. This laser is used to provide the electron beam for FEL by stimulating electron flow from a High Voltage gun [2]. The Timer cards are used to provide micro pulse frequency control and to gate the Drive Laser output, thereby providing macro pulse frequency and pulse width control. A fourth digital i/o card calculates duty factor. The user screen for these controls is shown in Figure 5.

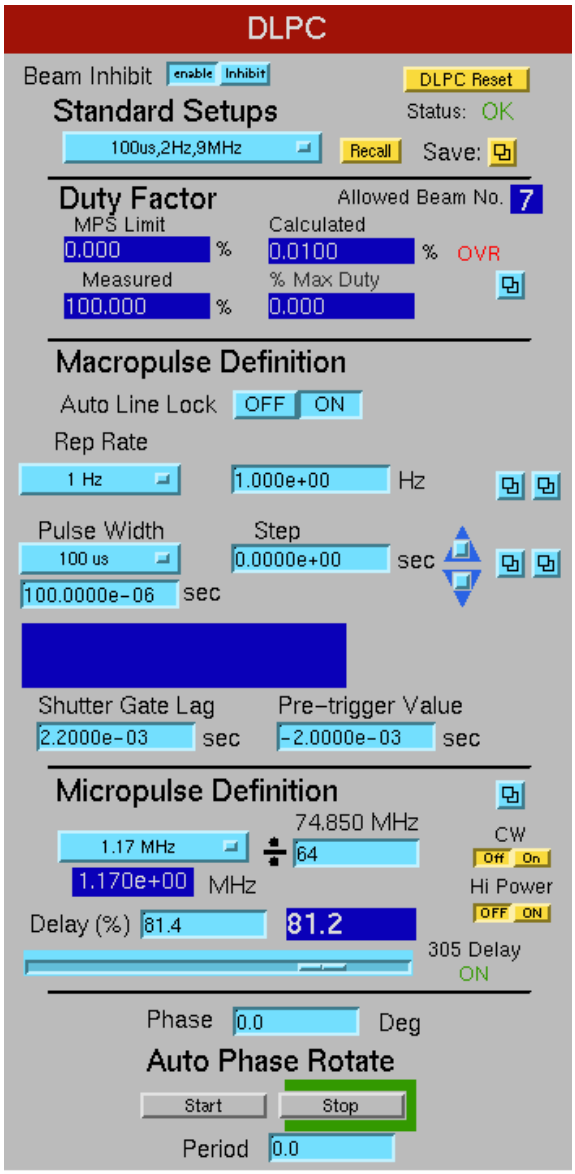

Figure 5: Multiple Carrier based timer boards used for High Level FEL Drive Laser Pulse Selection Application

SAMPLE APPLICATIONS

At the Jefferson Lab Free Electron Laser User Facility [3] the 30 or so VME i/o or Timer cards are presently in operational use for a variety of applications. At the simplest level, use for digital i/o, they control the Laser Safety System in 6 User Laboratories, they switch relays to allow mux control of 32 picomotors from a single driver channel, and they provide control for 48 BLMs. A sample of a diagnostic screen for one of four 12-channel BLM chassis was shown in Figure 3. A related Timer Card provides a gate which masks the BLMs from the MPS [4] system for ~ 400us microseconds after the start of a pulse. Finally, the Timer Cards mentioned in the previous section control the Drive Laser pulse output used to generate the electron beam.

CONCLUSIONS

Developers at the Jefferson Lab Free Electron Laser Facility have found the described Carrier Board design and the associated Timing modules to be highly versatile, convenient and reliable, and both hardware and software development time for new projects has been significantly reduced. The general purpose carrier board allows designers to focus the design of new functions to an efficient compact IP-pack sized footprint and provides an easy method of packaging and interfacing the design for rapid deployment in the field.

REFERENCES

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