DEVELOPMENT OF A TIME SYNCHRONIZATION SYSTEM FOR KSTAR WITH A VME-BUS SYSTEM

Mikyung Park, K.H.Kim, M.C.Kyum, and M.Kwon
National Fusion R&D Center, Korea Basic Science Institute, Daejeon, 305-806, KOREA

ABSTRACT

KSTAR tokamak is a superconducting reactor for nuclear fusion experiments, presently being constructed in Daejeon, KOREA. Tokamak, not such as accelerators, accomplishes experiments of plasma discharge during only a given time slot, and all subsystems such as superconducting magnet systems, magnet power supply systems, heating systems, diagnostics systems as well as control systems must be synchronized in operation referred to a specific time of starting the discharge shot. A Time Synchronization System (TSS) is being developed to achieve synchronized operation of all experiments according to a reference scenario which is determined by a pre-shot simulation. Moreover, it provides universal time information same as GPS (Global Positioning System) time to all subsystems, and an appropriate time-tagging function on every acquired data and events. The TSS is composed of a timing host, a central timing system with a reference time generator such as a GPS receiver and a central time unit (CTU), and local timings with local timing units (LTUs). The CTU produces the universal time data and the trigger/event information, and then broadcast them to local systems periodically via a dedicated fibre-optic time network. Also, the TSS communicates via the giga-bit machine network for the provision of universal time, and uses the shared memory-based real-time network for real-time feedback control. The LTU receives the information signal from the CTU and separates out the time and the trigger/event information as well as a master clock signal, and produces the properly delayed trigger pulses and sampling clocks to activate events in local devices. Simultaneously, the current time data is stored in time stamp buffer at the same rate of the sampling clock to tag on the acquisition data. Prototype timing modules has been developed in the VME bus standard, which uses FPGA and micro-processors to implement the major functions such as time decoding, a 64-bit time counter, data processing, clock/pulse generation, etc. We are testing the pilot timing system which is integrated with the home-made central and local timing units, and operated in an EPICS environment, the middle ware program of the KSTAR control system. This paper presents features of KSTAR timing system, details of the developed prototype timing module, and an integrated design with local control systems.

DESCRIPTION OF THE SYSTEM

Introduction of KSTAR Control System

The mission of the KSTAR project is to develop a steady-state-capable, advanced super-conducting tokamak to establish the scientific and technological bases for a fusion reactor as a future energy source. For this mission, the following requirements must be met at any price.

- Active control of profiles and transport to extend present stability and performance boundaries of tokamak operation.
- Achieve steady-state operation using non-inductive current drive to explore methods.
- Integrate optimized plasma performance and continuous operation.

To achieve the requirements, the KSTAR control system has been developed to have real time feedback functionality, long term maintainability, high reliability and flexibility. [1]

First, we have chosen the Experimental Physics and Industrial Control System (EPICS) as the middleware of KSTAR control system and a standard development tool. It has advantages that the framework provides network-based real-time distributed control, operating system independent programming tools, operator interface (OPI) tools, archiving tools, and interface tools with other commercial and non-commercial software. And Model Driven System Plus (MDSplus) has been chosen as an archiving tool for physics data handling and analysis.

The KSTAR integrated supervisory control system (SCS) is to have a capability of performing supervisory control and monitoring for all systems of tokamak. It is divided into plasma control system (PCS), machine control system (MCS), diagnostic control system (DCS), time synchronization system (TSS), and interlock system (ILS), in functionality. The control system must also integrate all local control systems being developed in various platforms such as Peripheral Component Interconnect (PCI) Extension for Instruments (PXI) and Compact PCI (cPCI), VME etc, by subcontractors. Connection between these systems is accomplished by several networks such as machine & control network based on Ethernet, storage network, timing network with own network protocol, reflective-memory-based real-time network (RTNet), and interlock network based on optical ControlNet™. [2]

Features of the Time Synchronization System

The tokamak operates in a pulse mode not such as continuously operated machine, and plasma discharge experiment is fulfilled only during a specific time slot. Therefore, all devices taking a part in the experiment must be precisely synchronized in operation for a success of plasma discharge. The primary purpose of the TSS is just to provide synchronized operation of the tokamak in conformity to the reference scenario as a result of pre-shot simulation by the plasma control system. Other functions are that the TSS supplies universal time data to let all the systems comprising the KSTAR be operated with same time value at the same moment, and provides time-tagging on every event and all acquisition data. In addition, the TSS must have a capability to support real-time feedback control by generating the intermediate triggering signals during the shot, upon the reception of the corresponding commands from the plasma control system for long pulse operation in the future.

There are two kinds of modes to obtain the operation synchronization, that is, feed-forward mode and feedback mode. In feed-forward mode, the TSS simply follows the flow of pre-determined operation. In that case, triggering signals necessary for the local devices are generated by receiving the preloaded operation-related information through the dedicated time net. On the other hand, to achieve real-time feedback control for long-pulse operation, the TSS can receive new event information from the PCS using a reflective memory with bus interrupt in conjunction with the real-time network.

System Configuration

The TSS is composed of a timing host and a central timing system installed in main control room, and local timing units housed in the local I&Cs (Instrument and Controls) which adopt various types of platforms. The timing host receives a reference triggering scenario for the next discharge experiment from a discharge program, converts it to the specific data format which the CTU can recognize, and then downloads it to the central timing system. The control and supervision of the system are obtained using the OPI panel running at the timing host developed with EDM (Extensible Display Manager) which is an API (APplication Interface) tool provided by EPICS.

The central timing system is implemented in a VME bus system which is equipped with a VME controller running on VxWorks 5.5.1, a home made Central Time Unit (CTU), a reflective memory board (RFM), and a home made Local Time Unit (LTU). In addition, the Datum ET6100 GPS (global positioning system) time receiver is used as a universal time source and a Rubidium atomic clock is used as a master clock source. The key functions of CTU are the generation of the time-critical triggering information based on the reference scenario, the current time information received from GPS time, and a 100MHz master clock signal which is used as an operation clock signal in both CTU and LTU. These entire signals are combined into a data stream and transferred to the LTU via the dedicated time network. The universal time data is also served to all systems using SNTP (Simple Network Time Protocol) via the machine & control network based on Ethernet. The local timing system is composed of the LTU to generate the actual triggering pulse signals and sometimes the clock signals required for data acquisition, and the reflective memory board for real-time feedback control.

The LTU can have several bus types depending on the platform types of the local I&C, where the LTU installed in.

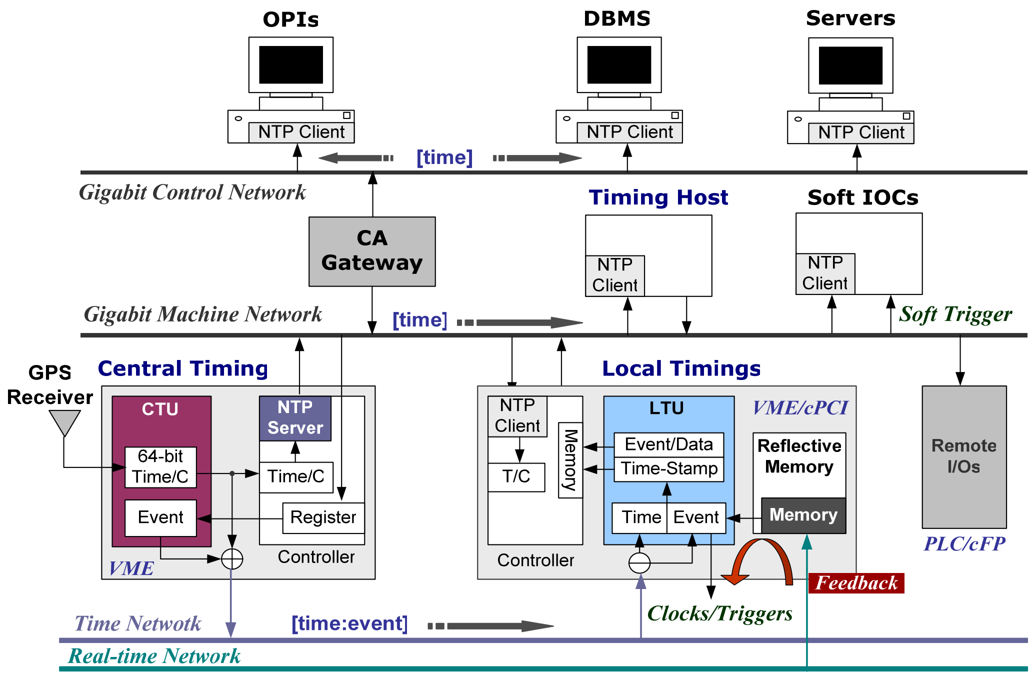

Figure 1: Structure of Time Synchronization System.

The TSS uses several networks for data transfer and communication. To ensure the TSS operated without any interference from other data traffic, it has the dedicated network between the central and the local systems, which it is built from an optical network using star topology. The universal time service using NTP is accomplished through the gigabit machine & control network. Additionally, the shared-memory based real-time network is used for the real-time feedback control of triggering time during the discharge shot.

FEATURES OF TIMING HARDWARES

Central Timing Unit (CTU) and Local Timing Unit (LTU)

The CTU in the VME-bus standard adopts one FPGA and two microprocessors with real-time capability for treating the key functions. One microprocessor, Helium 210-80 with a clock speed of 450MHz, takes charge of VME-bus interface, Ethernet drive, and function management. The other fulfils the decoding of IRIG-B GPS time code, serial interface, and LED drive. Most of the functions which the microprocessors have will be transferred to FPGA, later. The FPGA, a Xilinx Spartan II with 100k gates, handles a decoding of the timing-related data, a frame formatting, a signal encoding, and a signal modulation. The master clock of 100MHz results from multiplying the 10MHz signal from the external atomic clock generator by 10. The master clock is modulated with the timing signal from the FPGA and GPS time data, and transmitted to the LTU for use as a local clock after clock recovering process.

The CTU has an optical port, a 100Mbase Ethernet port, and several interfaces such as a serial port for downloading the processor’s program, a JTAG for FPGA debugging, and 7-segment LED driving port. The data frame generated in the CTU is composed of 2 bytes preamble, 2 bytes address, 30 bytes data, and 2 bytes of CRC (cyclic redundancy checksum). The preamble field identifies if the frame contains the current time data or event message data. The CTU runs under EPICS, version 3.14.4.

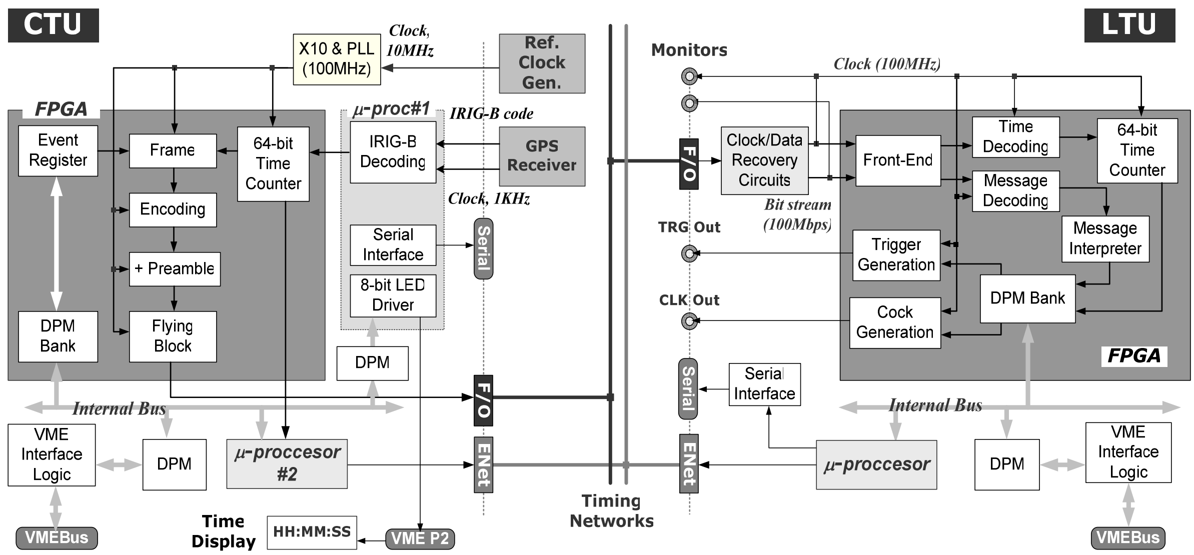

Figure 2: Functional diagram of CTU and LTU

The LTU uses same types of FPGA and microprocessor as the CTU's except that only one microprocessor is used. The key functions are to recover the 100MHz clock signal from the received modulated signal from the CTU and discriminate the time data and event message from the data stream by detecting the preamble embedded in. The decoded GPS time data is written in a 64-bit time counter ticked with the recovered local clock, which is synchronized with the master clock of the CTU to better than 1ns accuracy. The decoded event message data is loaded in an event register whose contents are used to generate trigger signals and clock signals in accordance with the reference scenario. Except for the clock/data recovery circuit, most of the functions are implemented in the FPGA such as time/message decoding, trigger/clock generation, a 64-bit time counter, etc. [3]

Pilot Timing System

The pilot system is implemented with a timing host, the VME-bus platform equipped with the MVME5100 VME controller, the home-made CTU, the LTU, a time display unit, and the optical time network of 1300nm in multi-mode. The VME controller runs in VxWorks5.5.1, and Linux red hat 9.0 is used for the timing host, and EPICS driver with v.3.14.4 was developed. The OPI panel developed by EDM runs in the timing host. The E6100 GPS receiver and a Rubidium source are used as the universal time and clock source, respectively. We confirmed the feed-forward operation from the timing host to the LTU. IRIG-B time code from the GPS receiver was converted to a real time value, and transferred successfully to the LTU with 1 second time lag. The LTU recovered a 100MHz clock from the 100MHz modulated signal with the time data and triggering data. The time jitter of the recovered 100MHz clock is less than 1 ns. The LTU generates 4 trigger signals and 2 clock signals with adjustable time delay, pulse width and frequency according to the reference triggering scenario from the timing host through the CTU. The time jitters of these trigger signals are less than 1ns, too.

REALIZATION OF THE SYNCFRONIZED OPERATION FOR LOCAL CONTROL SYSTEMS

Operation of Discharge Experiment

All the operations of tokamak for a discharge experiment must be controlled by the reference scenario in consecutive. Before a discharge shot, operation-related parameters such as PF coil charging waveform, timing-related parameters, etc, are downloaded to each local system. When a 'shot start' as a reference time 0 is released, each local system goes into action such as 'system turn-on',or 'start data acquisition' by receiving the triggers from the TSS. The local systems which should be operated synchronously are the magnet power supply system for superconducting magnets, heating system like ECH, NBI, ICRH, gas fuelling system, physics diagnostics system, plasma control system, and machine control system to supervise and control the tokamak. A timing chart of KSTAR operation scenario is shown in Figure 3 in brief.

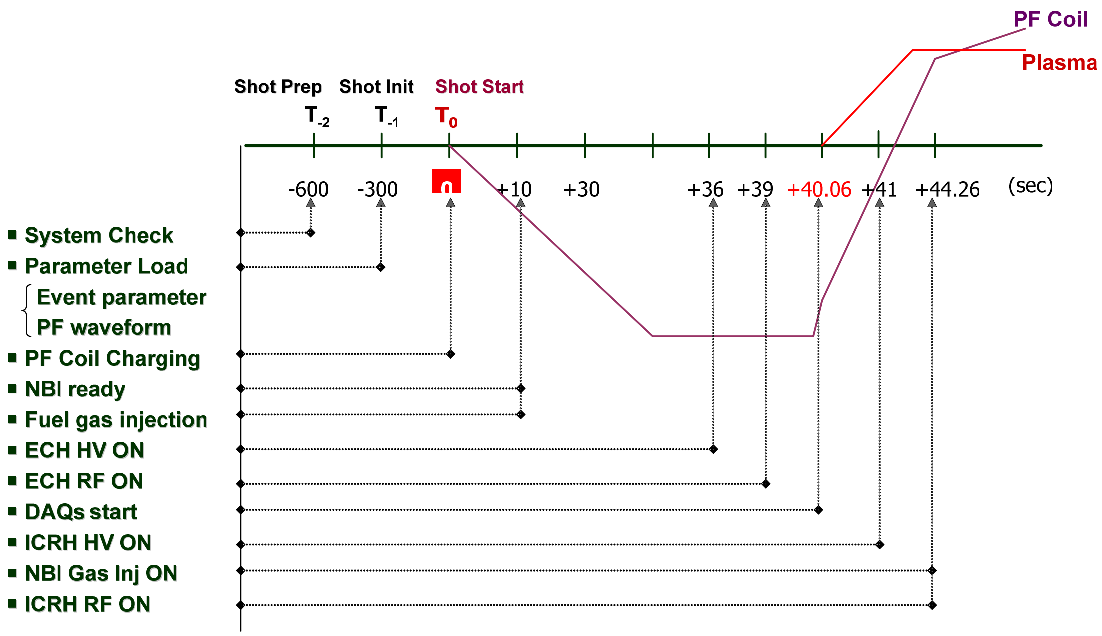

Figure 3: Operation Time Chart

There are several operation modes for the local systems in a view of timing.

- Pre-planned single trigger: A preloaded trigger required for activating the related event.
- Pre-planned triggering pattern : Preloaded multiple triggers required for several events
- Feedback control : The triggering time changed during a shot in real-time
- Software triggering : The triggering signal provided by software program, not LTU

Example of Magnetic Diagnostics System

Magnetic diagnostics system is basic plasma diagnostics to measure a magnetic flux and plasma current, etc. This system has the most in number of sensor channels and starts to collect physics data from the moment of plasma generated in tokamak and continues until the plasma is vanished. The data acquisition rate for most of sensors is maximum 200KHz except for Mirnove coil required of 20MHz sampling rate. The local I&C for the magnetic diagnostics is implemented in a VME system, and a G4Power PC series is chosen for the VME controller. Digitizer boards with 32 channel differential inputs, a LTU, and a reflective memory board are equipped in, together. As well, it has a local storage system of JBOD (Just a Bunch Of Disks) to acquire data even during a long pulse operation. Nevertheless, the whole data amounts with maximum sampling rate exceed 3 GB/shot in the case of only 20 sec operation, and it must be a burden on the local storage. To save the local storage, the system activates the digitizers with the trigger signals only at specific times to get meaningful data, not the entire time period of the shot. At that time, the LTU generates trigger/clock signals according to the pre-planned, trigger pattern. When it is required to change the triggering time during a shot, the related parameters are transferred to a memory in the reflective memory board via the real-time network. Using the VME bus interrupt, it is written in the event register in the LTU to generate the new trigger/clock signals. Figure 4 is the drawing of the local I&C for the Magnetic Diagnostics.

FUTURE WORKS

We must thoroughly test the integrated performance through entire hierarchies, from the supervisory control system to the local subsystem. Then the new timing boards, CTU and LTU, will be developed with real-time features in different bus standards such as cPCI and PXI. Another remaining issue is to device the method to calibrate signal path delay between all timing nodes through not only electrical path but optical path.

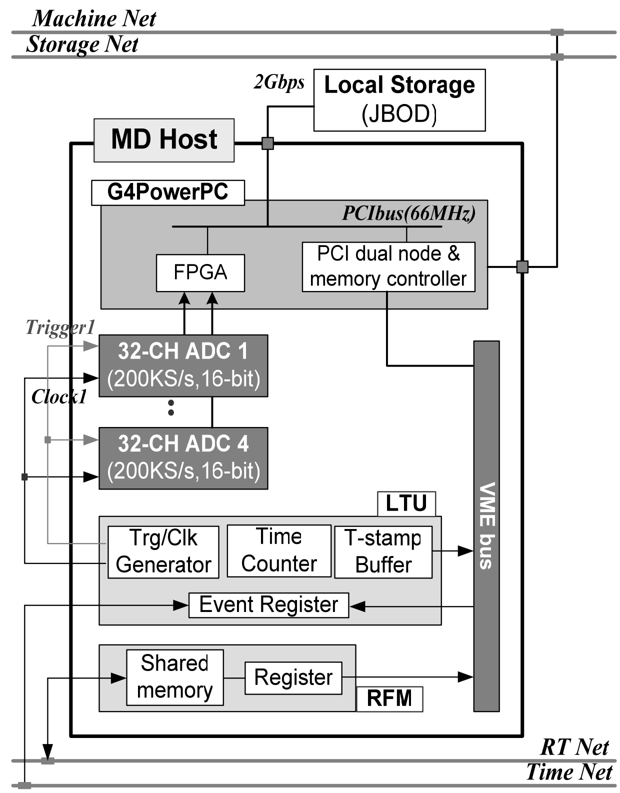

Figure 4: Configuration of Local I&C for Magnetic Diagnostics

SUMMARY AND CONCLUSION

- The TSS is a primary system to obtain the synchronized operation of tokamak in following the reference scenario what we would like to do.
- The TSS also provides the universal time information to all the systems comprising the KSTAR using GPS time code and NTP service function.
- The dedicated optical time network is used to ensure communication channel between the central and the local timing systems
- The prototype timing hardwares, the central timing unit and the local timing unit, have been developed in a VME-bus standard, and tested of performance of feed forward operation from the timing host to the local timing unit, successfully.
- The next versioned timing boards are being developed to have a functionality of real-time feedback control using the reflective memory board and the real-time network.

REFERENCES

[1] M. Kwon, et. al., “The control system of KSTAR”, Fusion Engineering and Design Vol.71 (2004) 17-21.
[2] K.H.Kim, et. al., “The KSAR Integrated Control System Based on EPICS”, IAEA TM2005, Budapest, Hungary, July 2005
[3] Jorg Schacht, et. al., “A trigger-time-event system for the W7-X experiment”, Fusion Engineering and Design Vol.60 (2002) 373-379.