STATUS OF THE SCSS CONTROL SYSTEM – FIRST PHASE OF AN 8GEV XFEL PROJECT IN SPRING-8

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ABSTRACT

The high brilliance coherent X-ray is an ideal light source to explore deep inside of material structure to know fundamental scientific phenomena. The SPring-8 Compact SASE Source (SCSS) project aims to build an 8GeV XFEL facility in the SPring-8 site. A project proposal has been submitted to the government of Japan; also project funding and feasibility hearings are now opened to scientific committees. A combination of the short period in-vacuum undulator and the high gradient C-band accelerator makes a machine compact, and it enables the construction site to fit the SPring-8 1km-long beamline space. The first phase of the SCSS project is to build a test facility, called the SCSS prototype accelerator facility, to ensure component technology and feasibility. The prototype accelerator consists of a low emittance electron gun with a CeB6 crystal thermionic cathode, a 40MV/m C-band (5712MHz) linac powered by 50MW klystrons, in-vacuum undulators, and other sophisticated components for the coming XFEL accelerator. The prototype machine commissioning is planned in autumn this year. The undulator will generate soft FEL with 250MeV low-emittance electron beams to serve as a VUV-FEL users facility. The control system has to provide the flexibility for the test and stability for users. This paper gives an overview of the project, and describes the control framework of the Message And Database Oriented Control Architecture (MADOCA) for the prototype and the 8GeV XFEL machine.

INTRODUCTION

RIKEN/SPring-8 started SPring-8 Compact SASE Source-project (SCSS) [1][2] in 2001. The SCSS project aims to build an 8GeV XFEL facility in the SPring-8 site. The X-ray FEL based on the self-amplification of spontaneous emission (SASE) usually requires a large-scale accelerator and a long undulator. A larger accelerator with several X-ray beamlines would raise the construction cost per beamline quite higher. One of the most effective factors on the facility construction cost is the machine size. To lower the cost, the machine has to be compact. A combination of the short period in-vacuum undulator and the high gradient C-band accelerator makes a machine compact, and it enables the construction site to fit the SPring-8 1km-long beamline space. The name SCSS, SPring-8 Compact SASE Source, was given by this reason. Figure 1 shows the machine layout of the SCSS to overlay the SPring-8 accelerator complex. The SCSS will be constructed adjacent to an operating 3rd generation synchrotron radiation source. This layout will give various opportunities of simultaneous use of the X-ray FEL and synchrotron radiation beams. The SCSS machine construction is planned to start in 2006 and should be completed by 2010.

The first phase of the SCSS project is to build a test facility, the SCSS prototype accelerator facility. The prototype accelerator consists of essential components for the coming full-scale SCSS as described in the below. In addition, other sophisticated components will be checked to ensure technology and feasibility. We also have a plan to test a seeding laser to compensate a variation of peak power.

The prototype machine commissioning is planned in autumn this year. The undulator will generate soft FEL with 250MeV low-emittance electron beams to serve as a VUV-FEL users facility. The control system has to provide the flexibility for the test and stability for users.

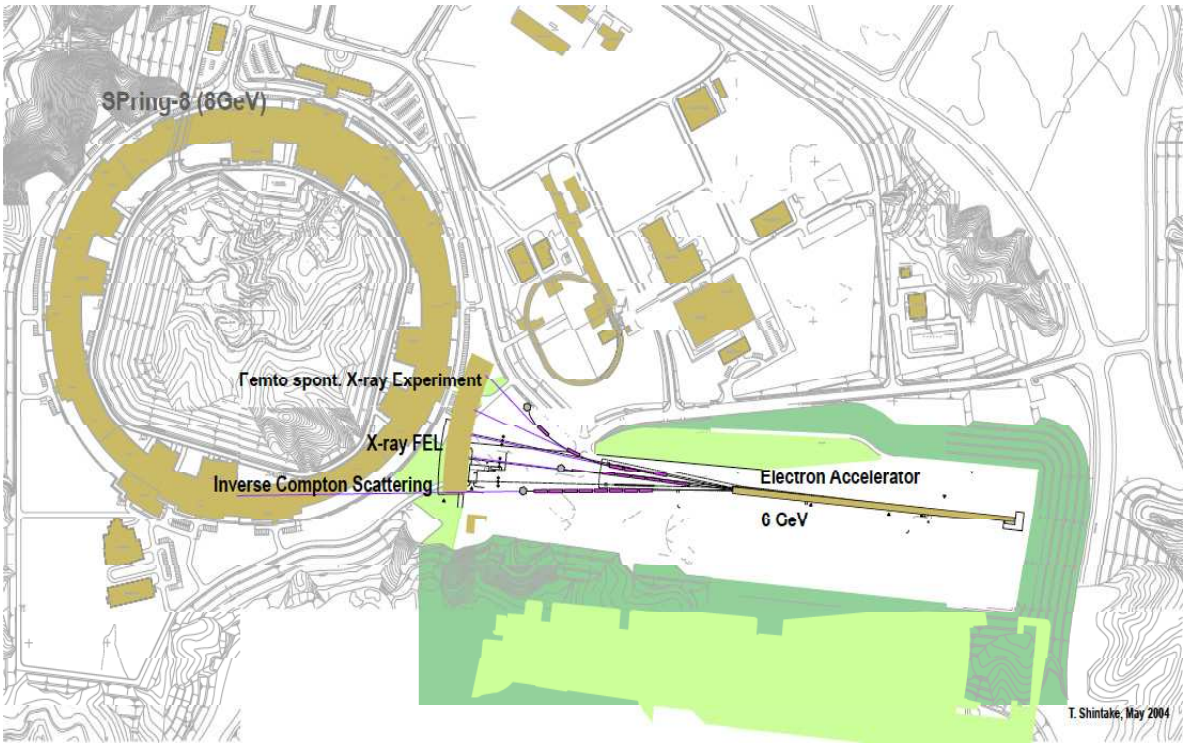

Figure 1: A bird eyes view of the 8GeV SCSS facility.

OVERVIEW OF THE PROTOTYPE ACCELERATOR

Figure 2 shows the machine layout of the prototype accelerator. The parameters of the accelerator are summarized in Table-1. The prototype accelerator consists of a low emittance electron gun with a CeB6 crystal thermionic cathode [3], a beam deflector with a fast high voltage pulsar, a 238 MHz pre-buncher cavity, a booster cavity at 476 MHz, a S-band buncher (2856MHz with APS structure), a S-band linac, two C-band (5712MHz) linacs powered by 50MW klystrons [4], and in-vacuum undulators. The high peak current is generated by compressing the beam bunch length in the injector (pre-buncher, booster and buncher) and in magnetic-chicane bunch compressor. We use two units of the C-band accelerating structures to form a C-band linac which generates 40 MV/m accelerating gradient. The beam energy will reach to 250 MeV within a 20 m long accelerator, and a radiation wavelength becomes 60 nm.

To monitor beam positions, we use screen monitors with high-resolution camera. The cavity-BPM type electron beam position monitors are installed specially at the C-band linacs and the undulators. The cavity type BPM has much larger beam-to-circuit coupling coefficient than a button type BPM electrode, therefore the intrinsic beam position resolution defined by a signal-to-noise ratio to the thermal noise in the detector circuit could be very high. The cavity BPM moves in transverse direction using precise mover.

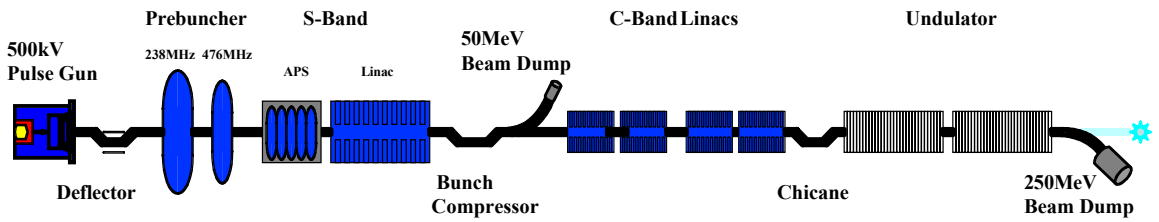

Figure 2: A schematic layout of the prototype accelerator.

Accelerator components such as magnet power supplies, klystron modulators, timing system and vacuum system are located along with the accelerator tunnel. Thirteen VME controllers are distributed around the linac and placed near accelerator components.

Table 1: The prototype accelerator specifications

Parameters		**Parameters**	
Bunch charge (core part)	~ 0.3 nC	Undulator period	15 mm
Normalized emittance	2 πmm.mrad	Radiation wavelength	60 nm
Final electron energy	250 MeV	Minimum gap	3.5 mm
Final r.m.s. energy spread	0.02 %	Maximum K-parameter	1.3
Final FWHM bunch length	0.5 psec	Undulator segment length	4.5 m
Transverse beam size	100 um	Total undulator length	10 m
Peak current	0.5 kA	FEL saturation length	20 m

CONTROL FRAMEWORK

The control system has to provide the flexibility for the test and stability for users. The Message And Database Oriented Control Architecture (MADOCA)[5] is used for the prototype accelerator control framework. The MADOCA was originally developed for SPring-8. The relational database management system (RDBMS) is prepared as one of the MADOCA components. The MADOCA software framework is adaptive and scalable from an X-ray beamline experiment to the SPring-8 accelerator complex (a linac, a booster synchrotron and an 8GeV storage ring). This feature is promising to develop the prototype accelerator control software to adapt the full-scale SCSS. MADOCA provides flexibility and power to fulfil the needs to run various operation modes at an accelerator facility. MADOCA is expected to control the combined operations of the SCSS accelerator and its insertion device for X-ray generation.

The RDBMS is a key for stable operation. For example, an energy change will cause trajectory deviation by dispersion in focusing system, or change of a bunch compression factor in chicane magnet. The charge variation will cause energy variation by beam loading effect. Those parameters are closely related, and it is not simple to deduce the beam stability limitation factor. To understand the beam dynamics phenomena, all of logging data and parameters of the accelerator have to be analysed by the correlation search method relating to the beam conditions by intensively using the RDBMS. MADOCA provides an analyzing power by using Sybase ASE12.0 for the RDBMS [6].

Accelerator operation programs will be developed using X-Mate, a GUI builder on the bases of X-Window. The GUI builder enables rapid prototyping and easy development of a sophisticated GUI. For an operation console, we selected Intel architecture (IA-32) workstation running Red Hat Enterprise Linux 3.

HARDWARE COMPONENT

Equipment Interface

An interface from the upper control layer to the equipment is through the VME systems. The Equipment Manager (EM) program runs on each VME system as device control software. Thirteen VME systems are installed for each component system, e.g. vacuum on the klystron gallery. The VME controllers use IA-32 processor boards running Solaris 9 x86 with capability of booting from a Compact Flash card. High-speed analog and trigger signals are controlled by direct connections

between the VME and the equipment. Other connections are Programmable Logic Controllers (PLC) and OPT-VME remote I/O boards [7]. The FL-net [8] is used for communication with PLC, as described in below. The PLC and the OPT-VME reduce the number of I/O signal wiring.

Programmable Logic Controller

We selected a FM-A3 from Yokogawa Electric Co.,Ltd [9] for the PLC. The PLCs are installed on vacuum system, interlock, RF system (e.g. modulator) and magnet power supply. The PLC executes a fixed control sequence and handles interlock signals. A local control capability is implemented to support maintenance and monitoring of the equipment. A display panel is attached to each PLC for local control.

The peripheral bus, the DeviceNet, is used for slow control. The DeviceNet interconnects between the PLC and the equipment to reduce the number of signal cabling as well.

FL-net

We selected the FL-net for communication between PLC and front-end control devices [10]. A FL-net is one of the Ethernet-based open standard protocols for a factory floor network authorized by the consortium in Japan. The FL-net started from the bases on the network requirements of Japan Automobile Manufacturers Association (JAMA). The specification was established afterwards as the JEM standards in Nov 2000, and as the Japanese industrial standards (JIS) in Feb 2004. Main features of the FL-net are listed as follows:

- Physical layer is Ethernet.
- The newly developed 'FA link protocol' on UDP/IP meets a high speed, large quantity data transmission.
- Automatic participation or out of a node (a station) is possible.
- Adopting a master-less token method and good RAS function.
- An 8k words and an 8k bits data are transferred by a cyclic transmission.
- A message transmission service of 1,024bytes per frame is possible.

A VME-based FL-net interface board has been developed to control front-end devices through VMEbus systems. The board has a function to execute the FL-net protocol by the firmware.

High-speed A/D and D/A

To improve a stability of RF system, we developed a high-speed A/D and D/A VME boards. The boards work with a 238MHz clock, the sub-harmonic of 5712MHz. Each board has four channels of inputs or outputs with 12bits resolution [11]. The A/D board was designed for an IQ demodulator with a down converting mixer which detect phase/amplitude signals generated by the klystron. In addition, the board is used for beam position signals observed by the cavity type beam position monitors. The A/D board is capable to detect an abnormal signal generated by the klystron, and save the signal waveform. This function is useful to find a problem. The D/A board has a function to generate signals of Q and I component for the klystron input. It has 32 taps FIR filters to control a rise time and phase flip for the SLED.

The A/D and D/A combination allows a digital feedback of a low-level RF system for driving the C-band klystrons. The system can detect and remove unwanted variations of a RF power/phase caused by thyratron instability, thermal drift, and other sources.

Master Trigger and Trigger Delay Unit

To improve a performance of trigger jitter, we developed a master trigger unit and a trigger delay unit as a VME board, respectively [12][2]. The master trigger unit can set a repetition rate up to 60 Hz. The

trigger is either synchronized or unsynchronized with the commercial power mains frequency for extracting electron beams from the electron gun or pulsing the klystron modulator. The system continuously outputs master trigger pulses. Each trigger pulse is distributed from the master trigger to the various accelerator devices.

The trigger delay unit is a 5712MHz synchronous delay VME module. We employ a fast GaAs logic device and an FPGA with 15 bits counters to synchronize to the 5712 MHz RF signal at the trigger delay unit. The time jitter is less than 1ps. This can decrease rise time jitter in the trigger pulse.

OPT-VME

The OPT-VME system was already developed and adopted for the linac of SPring-8. The system consists of master VME boards and slave remote boards. A master board and a remote board is linked with H-PCF optical fiber cable. One master board can connect four remote boards. The system provides high-speed communication of a 64 bits data within 40 microseconds. We use the 64 bits DI/DO remote board with photo-coupler isolation to control beam correction electromagnet power supplies.

Motor Control Unit (MCU)

We selected a pulse motor control unit (MCU) with Ethernet connectivity for local control of motor drivers of the BPM alignment mover, beam collimators, and slits. The MCU was developed and adopted for the linac of SPring-8 [7]. The controller is 4U height, fan-less, and disk-less system with three PCIbus slots. For a local operation, a 4-inch LCD with touch panel is attached to the front of the MCU.

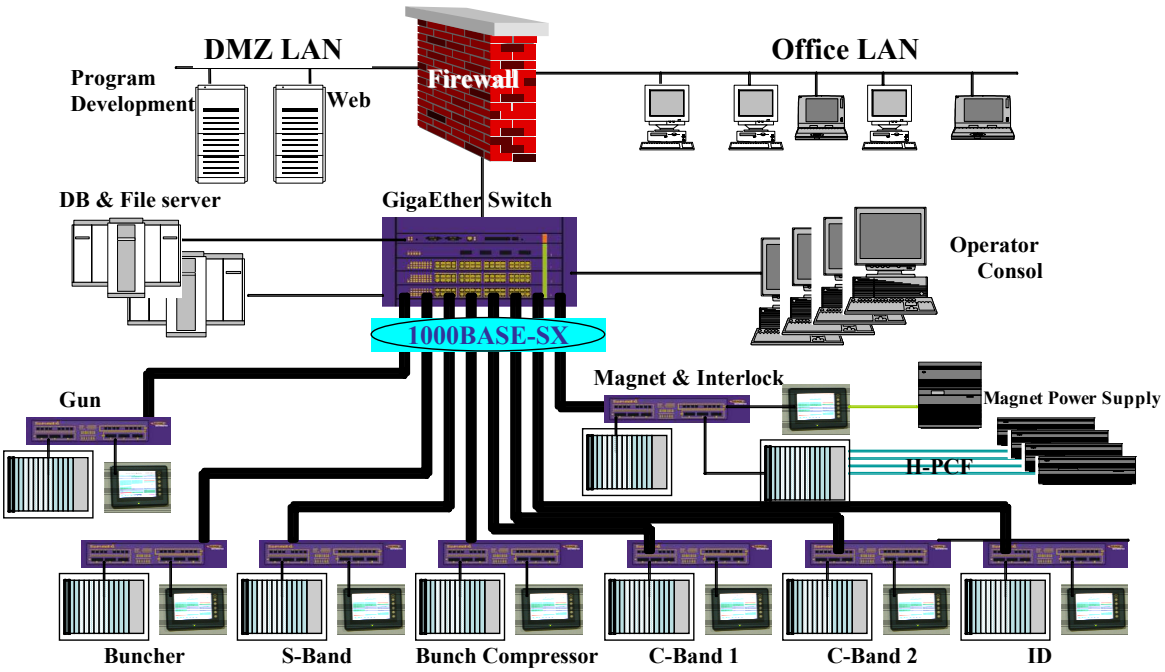

Figure 3: A schematic layout of the accelerator control network

Network System

A firewall protects and interconnects the accelerator control network, the DMZ LAN, and the office LAN as shown in Fig. 3. The program software development servers are placed in the DMZ LAN. A Gigabit Ethernet with optical fiber is used for the backbone of the accelerator control network. Because

the FL-net is based on the Ethernet, an accelerator control network and the FL-net share the backbone. Each FL-net segment and the control network are separated by virtual LAN. A bandwidth of the CPU of VME is 100Mbps and the FL-net is 10Mbps. We define two or three FL-net segments on the backbone. Total maximum bandwidth is estimated less than 150Mbps and average bandwidth is less than 100Mbps. Because network utilization is expected to be less than 10% of the backbone, the FL-net is capable to perform real-time response as defined in its specification. A maintenance network with wireless LAN is in the accelerator tunnel separately from the control network. The wireless network is useful for equipment maintenance by a connection to the control network.

For event synchronization data acquisition, we have a plan to introduce a shared memory network and event driven data acquisition framework, which was already developed and adopted for the linac of SPring-8 [7].

PROJECT SCHEDULE

The machine construction has been completed, and we will start RF component conditioning and system check in October this year. The machine commissioning will start on December, to observe the first radiation from the prototype accelerator within this year.

ACKNOWLEDGEMENT

The authors would like to thank to all of contributors in the SCSS project, including members from RIKEN/SPring-8, and JASRI/SPring-8.

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