NEW TECHNOLOGIES IN THE DESIGN OF RF CONTROLS FOR ACCELERATORS

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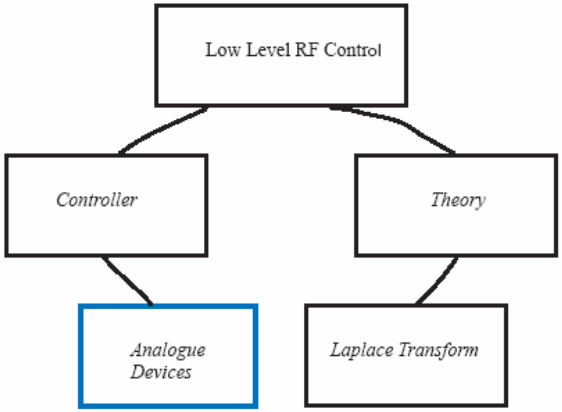
Trends in Low Level RF Control



Outline

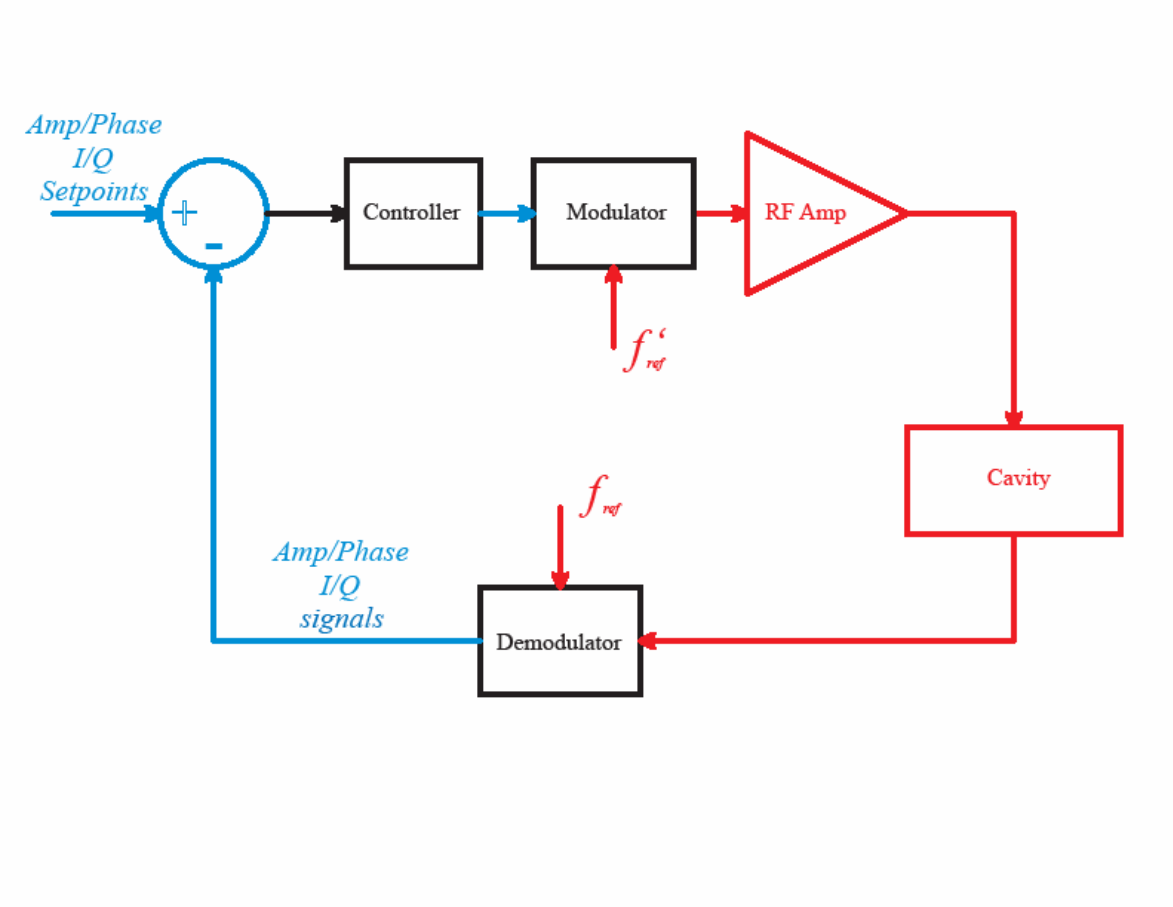
- Difference between Signal processing and digital feedback control
- Demodulations and Modulations
- Signal processing hardware
  - FPGA and DSP
- Self Diagnostic
  - JTAG Boundary Scan
- Adaptive Control
  - Self-tuning Regulator
- Advances in software
  - Multi-tasking and multi-threading
- Conclusion

Difference between Digital Feedback Control and Signal Processing

	Feedback Control	Signal Processing
Signal Bandwidth f_s	< 1MHz	> 10 MHz
Transport Lag	$< \frac{1}{10 f_s}$	< 100 ms
Sampling rate	$> 10 f_s$	$\geq 2 f_s$
Signal Strength	Strong	weak
Phase noise	$<0.01^o$	$< 2^o$

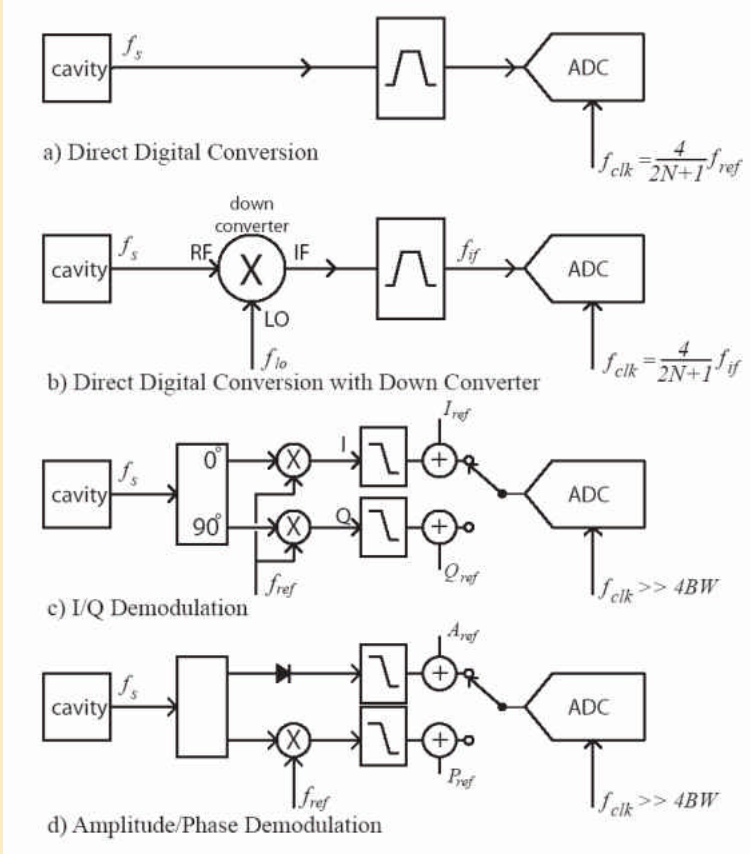
Digital feedback is digital signal processing with some special requirements

A Basic Low Level RF Feedback Control System

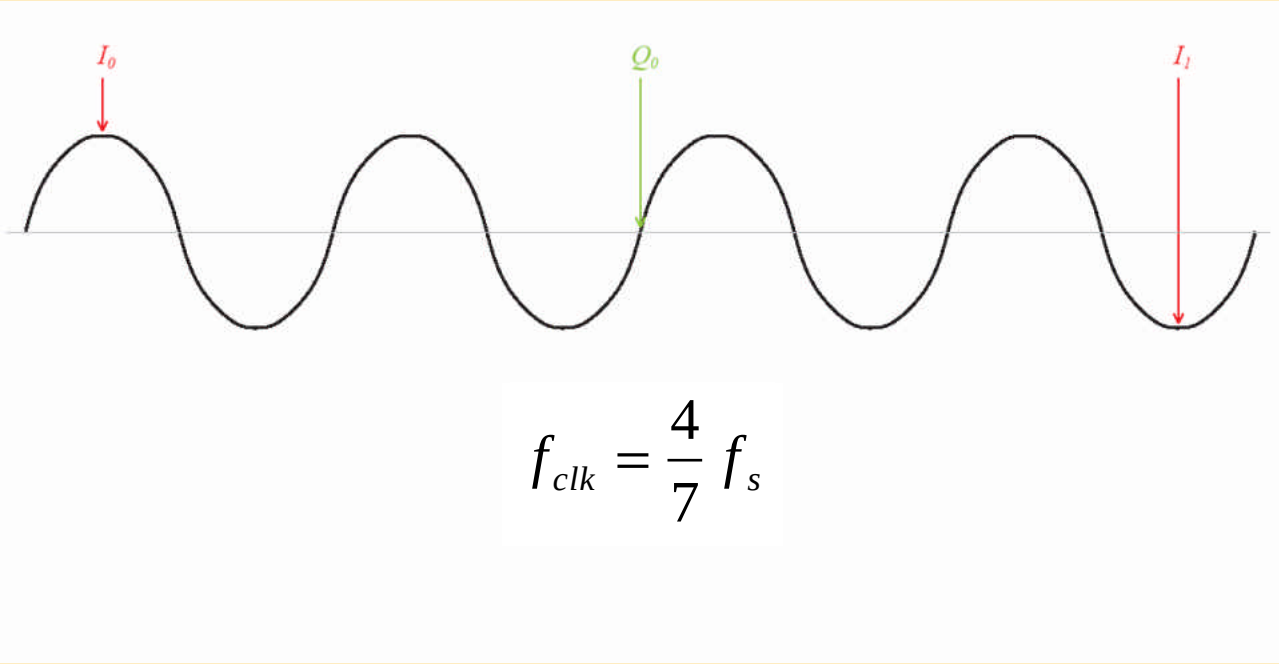


Regulate : To control the RF voltage and phase in the cavity.
Safety : Protect personnel and equipment.
Info : Tell what is going on

RF Demodulation Schemes



Quadrature Sampling and undersampling



$$f_{clk} = \frac{4}{7} f_s$$

Direct Digital Conversion

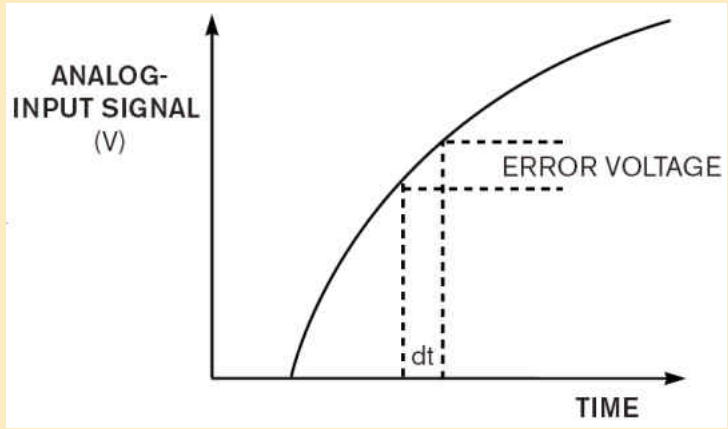
- Direct Conversion from RF – no analogue baseband
- Quantization noise $SNR_{adc} = 6.02N + 1.76dB$
  - 8, 10 bit ADC – significant quantization noise. 0.08%, 0.046°
  - 14, 16 bit ADC – quantization noise not a factor. 0.001%, 0.0007°
- Quadrature sampling – I/Q channels separation in digital form

$$f_s = \frac{4}{2N+1} f_{ref}$$

- Use undersampling to reduce sampling rate.
- Sampling clock needs to be phase locked to signal
- Requires sampling clock with high sampling rate and very low jitter/phase noise :

$$SNR_{clk}(dB) = 20\log\left[\frac{1}{2\pi f_s \sqrt{s_{clk}^2 + s_{adc}^2}}\right]$$

$$SNR_{clk}(dB) = 20\log\left[\frac{f_{clk}}{f_s}\frac{1}{\int 2\Phi(f)df}\right]$$



Direct Digital Conversion, ctnd

- using down converter
  - Less stringent requirement on ADC, sampling clock,
  - But local oscillator needs to be phase locked.
    - Highly complicated frequency generation.

Some state-of-art ADCs

LINEAR TECHNOLOGY

LTC2209

16-Bit, 160Msps ADC

FEATURES

- Sample Rate: 160Msps
- 77.3dBFS Noise Floor
- 100dB SFDR
- SFDR >84dB at 250MHz (1.5V_{P-P} Input Range)
- PGA Front End (2.25V_{P-P} or 1.5V_{P-P} Input Range)
- 700MHz Full Power Bandwidth S/H
- Optional Internal Dither
- Optional Data Output Randomizer
- LVDS or CMOS Outputs
- Single 3.3V Supply
- Power Dissipation: 1.45W
- Clock Duty Cycle Stabilizer
- Pin Compatible 14-Bit Version
  160Msps: LTC2209 (16-Bit), LTC2209-14 (14-Bit)
- 64-Pin (9mm × 9mm) QFN Package

APPLICATIONS

- Telecommunications
- Receivers
- Cellular Base Stations
- Spectrum Analysis
- Imaging Systems
- ATE

DESCRIPTION

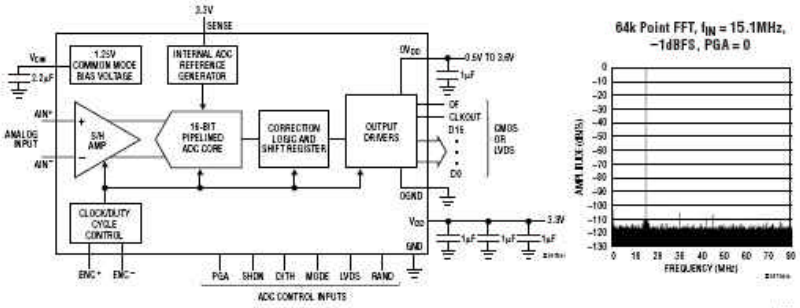
The LTC®2209 is a 160Msps 16-bit A/D converter designed for digitizing high frequency, wide dynamic range signals with input frequencies up to 700MHz. The input range of the ADC can be optimized with the PGA front end.

The LTC2209 is perfect for demanding communications applications, with AC performance that includes 77.3dBFS Noise Floor and 100dB spurious free dynamic range (SFDR). Ultra low jitter of 70fs_{RMS} allows undersampling of high input frequencies with excellent noise performance. Maximum DC specs include ±5LSB INL, ±1LSB DNL (no missing codes).

The digital output can be either differential LVDS or single-ended CMOS. There are two format options for the CMOS outputs: a single bus running at the full data rate or demultiplexed busses running at half data rate. A separate output power supply allows the CMOS output swing to range from 0.5V to 3.6V.

The ENC+ and ENC– inputs may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed with a wide range of clock duty cycles.

TYPICAL APPLICATION



ANALOG DEVICES

16-Bit, 80/100 MSPS ADC

AD9446

FEATURES

- 100 MSPS guaranteed sampling rate (AD9446-100)
- 83.6 dBFS SNR with 30 MHz input (3.8 V p-p input, 80 MSPS)
- 82.6 dBFS SNR with 30 MHz input (3.2 V p-p input, 80 MSPS)
- 89 dBc SFDR with 30 MHz input (3.2 V p-p input, 80 MSPS)
- 95 dBFS 2-tone SFDR with 9.8 MHz and 10.8 MHz (100 MSPS)
- 60 fsec rms jitter
- Excellent linearity
  - DNL = ±0.4 LSB typical
  - INL = ±3.0 LSB typical
- 2.0 V p-p to 4.0 V p-p differential full-scale input
- Buffered analog inputs
- LVDS outputs (ANSI-644 compatible) or CMOS outputs
- Data format select (offset binary or twos complement)
- Output clock available
- 3.3 V and 5 V supply operation

APPLICATIONS

- MRI receivers
- Multicarrier, multimode cellular receivers
- Antenna array positioning
- Power amplifier linearization
- Broadband wireless
- Radar
- Infrared imaging
- Communications instrumentation

GENERAL DESCRIPTION

The AD9446 is a 16-bit, monolithic, sampling analog-to-digital converter (ADC) with an on-chip track-and-hold circuit. It is optimized for performance, small size, and ease of use. The product operates up to a 100 MSPS, providing superior SNR for instrumentation, medical imaging, and radar receivers employing baseband (<100 MHz) IF frequencies.

The ADC requires 3.3 V and 5.0 V power supplies and a low voltage differential input clock for full performance operation. No external reference or driver components are required for many applications. Data outputs are CMOS or LVDS compatible (ANSI-644 compatible) and include the means to reduce the overall current needed for short trace distances.

FUNCTIONAL BLOCK DIAGRAM

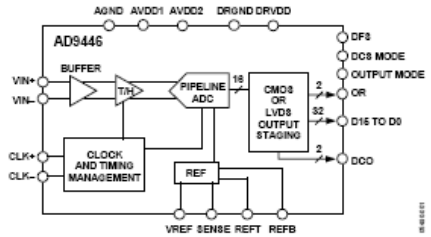


Figure 1.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data mode.

The AD9446 is available in a Pb-free, 100-lead, surface-mount, plastic package (100-lead TQFP/EP) specified over the industrial temperature range –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. True 16-bit linearity.
2. High performance: outstanding SNR performance for baseband IFs in data acquisition, instrumentation, magnetic resonance imaging, and radar receivers.
3. Ease of use: on-chip reference and high input impedance track-and-hold with adjustable analog input range and an output clock simplifies data capture.
4. Packaged in a Pb-free, 100-lead TQFP/EP package.
5. Clock duty cycle stabilizer (DCS) maintains overall ADC performance over a wide range of clock pulse widths.
6. OR (out-of-range) outputs indicate when the signal is beyond the selected input range.

Some state-of-art Clocks

ANALOG DEVICES

1.2 GHz Clock Distribution IC, PLL Core, Dividers, Delay Adjust, Eight Outputs

AD9510

FEATURES

Low phase noise phase-locked loop core
- Reference input frequencies to 250 MHz
- Programmable dual-modulus prescaler
- Programmable charge pump (CP) current
- Separate CP supply (V_{CP}) extends tuning range

Two 1.6 GHz, differential clock inputs
8 programmable dividers, 1 to 32, all integers
Phase select for output-to-output coarse delay adjust
4 independent 1.2 GHz LVPECL outputs
- Additive output jitter 225 fs rms

4 independent 800 MHz/250 MHz LVDS/CMOS clock outputs
- Additive output jitter 275 fs rms
- Fine delay adjust on 2 LVDS/CMOS outputs

Serial control port
Space-saving 64-lead LFCSP

APPLICATIONS

Low jitter, low phase noise clock distribution
Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
High performance wireless transceivers
High performance instrumentation
Broadband infrastructure

FUNCTIONAL BLOCK DIAGRAM

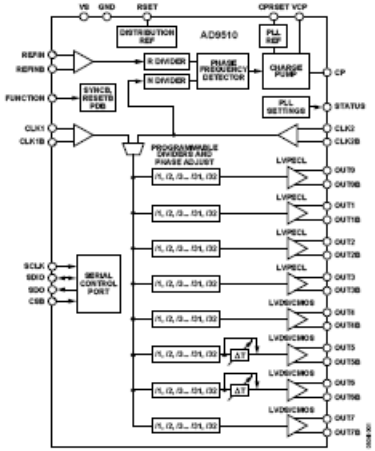


Figure 1.

GENERAL DESCRIPTION

The AD9510 provides a multi-output clock distribution function along with an on-chip PLL core. The design emphasizes low jitter and phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

The PLL section consists of a programmable reference divider (R); a low noise phase frequency detector (PFD); a precision charge pump (CP); and a programmable feedback divider (N). By connecting an external VCXO or VCO to the CLK2/CLK2B pins, frequencies up to 1.6 GHz may be synchronized to the input reference.

There are eight independent clock outputs. Four outputs are LVPECL (1.2 GHz), and four are selectable as either LVDS (800 MHz) or CMOS (250 MHz) levels.

Each output has a programmable divider that may be bypassed or set to divide by any integer up to 32. The phase of one clock output relative to another clock output may be varied by means of a divider phase select function that serves as a coarse timing adjustment. Two of the LVDS/CMOS outputs feature programmable delay elements with full-scale ranges up to 10 ns of delay. This fine tuning delay block has 5-bit resolution, giving 32 possible delays from which to choose for each full-scale setting.

The AD9510 is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

The AD9510 is available in a 64-lead LFCSP and can be operated from a single 3.3 V supply. An external VCO, which requires an extended voltage range, can be accommodated by connecting the charge pump supply (VCP) to 5.5 V. The temperature range is −40°C to +85°C.

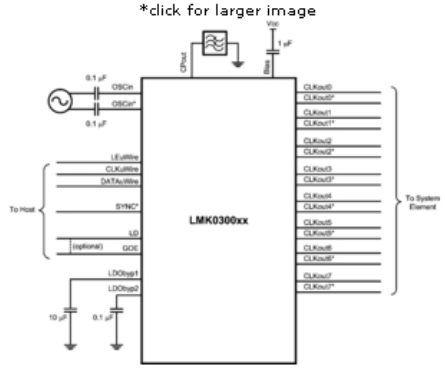
One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

Features

- Integrated VCO with very low phase noise floor
- Integrated Integer-N PLL with outstanding normalized phase noise contribution of -224 dBc/Hz
- Clock generator performance (10 Hz - 20 MHz)
- LMK03000C/ LMK03001C: 200 fs RMS jitter
- Two jitter cleaner performance grades (12 kHz to 20 MHz)
- LMK03000/ LMK03001: 800 fs RMS jitter
- LMK03000C/ LMK03001C: 400 fs RMS jitter
- Two VCO frequency plans
- LMK03000/ LMK03000C: 1185 to 1296 MHz
- LMK03001/ LMK03001C: 1470 to 1570 MHz
- Clock output frequency range of 1 to 785 MHz
- 3 LVDS and 5 LVPECL clock outputs
- Partially integrated loop filter
- Dedicated divider and delay blocks on each clock output
- Pin compatible family of clocking devices
- 3.15 to 3.45 V operation
- Package: 48 pin LLP (7.0 x 7.0 x 0.8 mm)

Typical Application

*click for larger image



Typical Application

Parametric Table expand

LVDS Outputs	3
LVPECL Outputs	5
PLL Type	PLL + VCO

Phase noise resulting from jitter and signal frequencies

- Aperture jitter – 60 fs
- Clock jitter – 275 fs

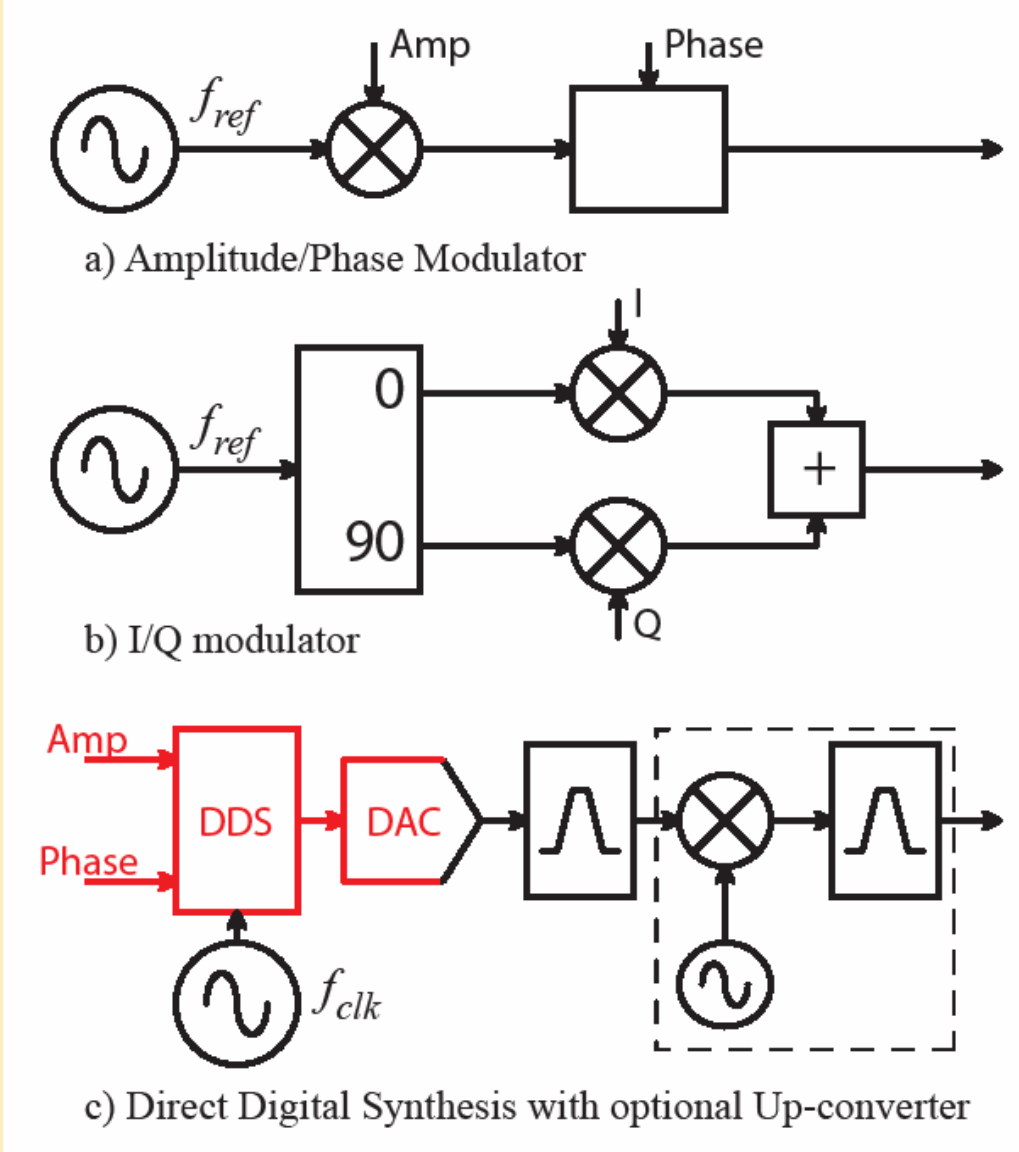
Signal Frequency	SNR	Phase accuracy
5 MHz	101 dBc	0.0005^{o}
30MHz	85 dBc	0.003^{o}
70MHz	78 dBc	0.007^{o}
140 MHz	72 dBc	0.014^{o}
250 MHz	67 dBc	0.025^{o}

How important is phase noise to accelerator control?

- For non-separated turn cyclotron – not important
- For short linacs –important
- For separated turn cyclotrons, storage rings and long linacs – very important
- ERLs, FELs – very very important

- The phase noise requirement + clock generation + mode of operation (self-excited vs driven) determines whether Direct Digital Conversion is suitable or not.

RF Modulation Schemes



Merits of different Modulator Schemes

Amp/Phase Modulator	I/Q modulator	Direct Digital Synthesis
Large phase control range -90º to +90º	Small phase control range -45º to +45º	Large phase control range infinite
Large cross-talk AM-PM, PM-AM conversion	Small cross-talk Incorrect quadrature	No cross talk
Subject to thermal drift	Subject to thermal drift	Not subject to thermal drift
Suitable for self-excited mode	Suitable for self-excited mode	Not suitable for self-excited mode
Uses external frequency reference	Uses external frequency reference	Requires external frequency that is rational fractions of reference frequency
Low phase noise	Low phase noise	High phase noise
Low data latency	Low data latency	High data latency

1 GSPS, 14-Bit, 3.3 V CMOS Direct Digital Synthesizer

2007

AD9910

FEATURES

1 GSPS internal clock speed (up to 400 MHz analog output)
Integrated 1 GSPS, 14-bit DAC
32-bit tuning word
Phase noise ≤ −125 dBc/Hz @ 1 kHz offset (400 MHz carrier)
Excellent dynamic performance with
  >80 dB narrow-band SFDR
Serial input/output (I/O) control
Automatic linear or arbitrary frequency, phase, and
  amplitude sweep capability
8 frequency and phase offset profiles
1.8 V and 3.3 V power supplies
Software and hardware controlled power-down
100-lead TQFP_EP package
Integrated 1024 word × 32-bit RAM
PLL REFCLK multiplier
Parallel datapath interface
Internal oscillator, can be driven by a single crystal
Phase modulation capability
Amplitude modulation capability
Multichip synchronization

APPLICATIONS

Agile local oscillator (LO) frequency synthesis
Programmable clock generator
FM chirp source for radar and scanning systems
Test and measurement equipment
Acousto-optic device drivers
Polar modulator
Fast frequency hopping

FUNCTIONAL BLOCK DIAGRAM

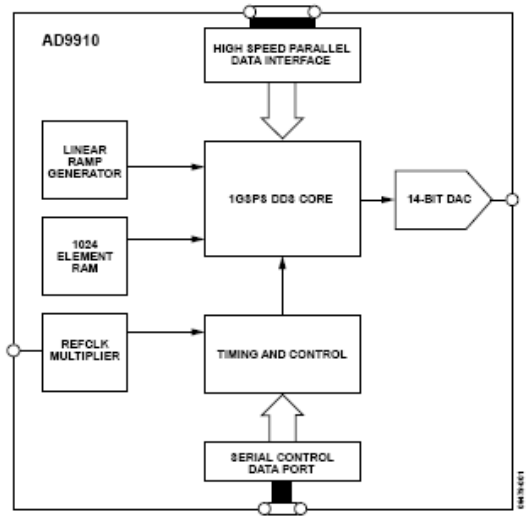


Figure 1.

Rev. 0

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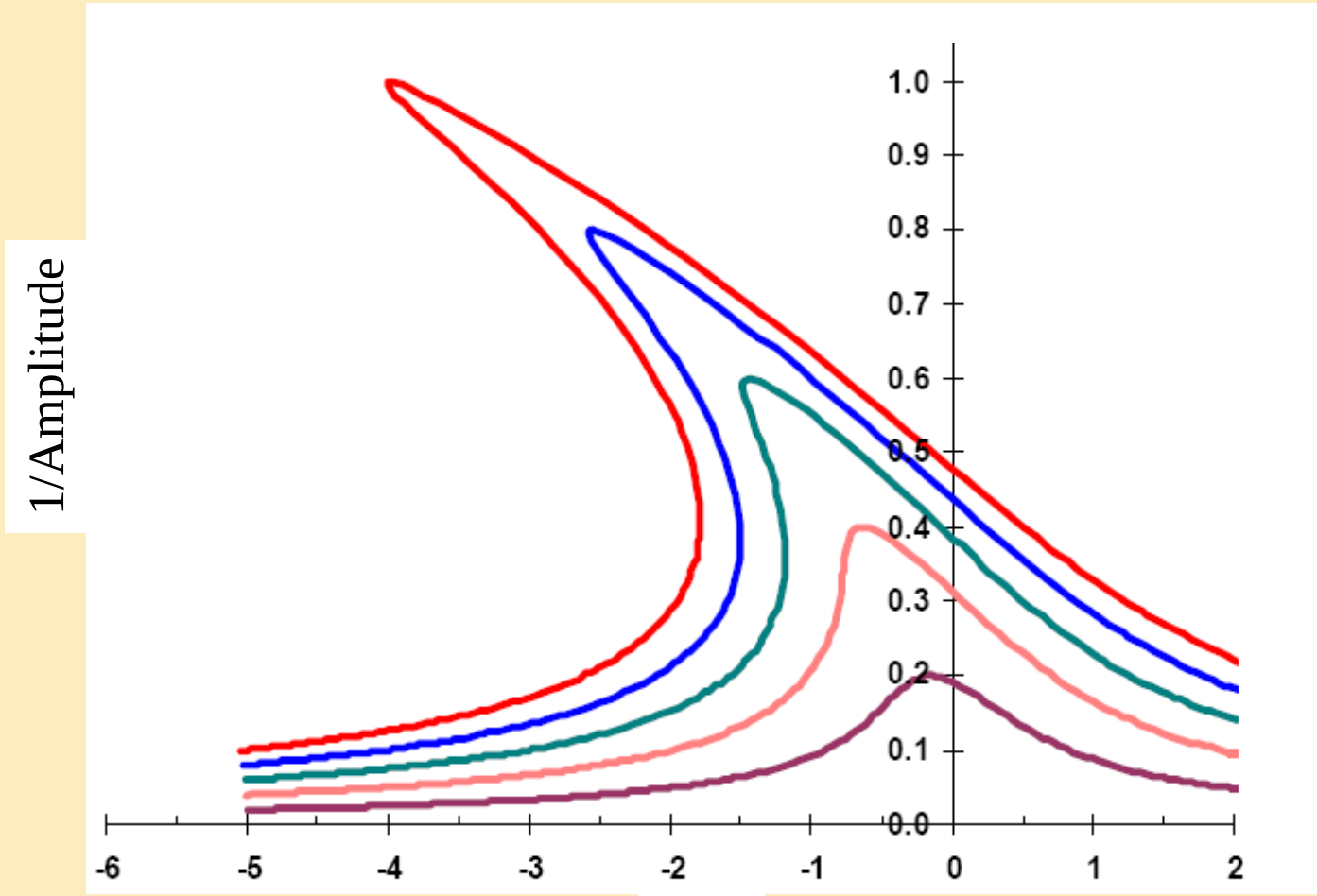
Parameter	Conditions/Comments	Min	Typ	Max	Unit
201.1 MHz Analog Output	±500 kHz		−87		dBc
	±125 kHz		−87		dBc
	±12.5 kHz		−91		dBc
301.1 MHz Analog Output	±500 kHz		−86		dBc
	±125 kHz		−86		dBc
	±12.5 kHz		−88		dBc
401.3 MHz Analog Output	±500 kHz		−84		dBc
	±125 kHz		−84		dBc
	±12.5 kHz		−85		dBc
SERIAL PORT TIMING CHARACTERISTICS					
Maximum SCLK Frequency			70		Mbps
Minimum SCLK Clock Pulse Width	Low	4			ns
	High	4			ns
Maximum SCLK Rise/Fall Time			2		ns
Minimum Data Setup Time to SCLK		5			ns
Minimum Data Hold Time to SCLK		0			ns
Maximum Data Valid Time in Read Mode				11	ns
I/O_UPDATE/PS0/PS1/PS2 TIMING CHARACTERISTICS					
Minimum Pulse Width	High	1			SYNC_CLK cycle
Minimum Setup Time to SYNC_CLK		2			ns
Minimum Hold Time to SYNC_CLK		0			ns
Tx_ENABLE and 16-BIT PARALLEL (DATA) BUS TIMING					
Maximum PDCLK Frequency			250		MHz
Tx_ENABLE/Data Setup Time (to PDCLK)		2			ns
Tx_ENABLE/Data Hold Time (to PDCLK)		1			ns
MISCELLANEOUS TIMING CHARACTERISTICS					
Wake-Up Time[2]			1		ms
Fast Recovery			8		SYSCLK cycles
Full Sleep Mode				150	µs
Minimum Reset Pulse Width High			5		SYSCLK cycles[3]
DATA LATENCY (PIPE_LINE DELAY)					
Data Latency, Single Tone or using Profiles					
Frequency, Phase, Amplitude-to-DAC Output	Matched latency enabled and OSK enabled		91		SYSCLK cycles
Frequency, Phase-to-DAC Output	Matched latency enabled and OSK disabled		79		SYSCLK cycles
	Matched latency disabled		79		SYSCLK cycles
Amplitude-to-DAC Output	Matched latency disabled		47		SYSCLK cycles
Data Latency using RAM Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		94		SYSCLK cycles
Amplitude-to-DAC Output	Matched latency enabled		106		SYSCLK cycles
	Matched latency disabled		58		SYSCLK cycles
Data Latency, Sweep Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		91		SYSCLK cycles
Amplitude-to-DAC Output	Matched latency enabled		91		SYSCLK cycles
	Matched latency disabled		47		SYSCLK cycles
Data Latency, 16-Bit Input Modulation Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled		103		SYSCLK cycles
	Matched latency disabled		91		SYSCLK cycles

Some feedback induces instabilities that affect the choice of modulation schemes

Instabilities from Limit cycle oscillations

AM-PM Conversion $\Delta f = -k|V|$



Which Modulation/Demodulation Scheme?

- Lorentz Force is strong when
  - High field strength (>2MV/m)
  - Soft metal (e.g. Nb)
  - Driven mode operation may introduce limit cycle instability.
    - Cannot use DDS.
    - Cannot use Direct Digital Conversion
- AM-PM conversion is high when
  - Amplifier not operating in Class A
    - High phase dependence on power.
  - I/Q modulator with feedback may introduce limit cycle instability.
    - Cannot use I/Q modulation.

Using DDS in LLRF Modulator

- Advantages of DDS applicable to LLRF control
  - -All digital, no analogue degradation
  - -Perfect I/Q channel balance
  - -Can generate extremely precise quadrature signals
  - -High frequency bandwidth
  - -Sawtooth generator
- Advantages of DDS not applicable to LLRF control
  - ü Very fine frequency resolution
  - ü No phase discontinuity
  - ü Frequency agile
- Disadvantage of DDS applicable to LLRF control
  - -Spurs from
    - DAC nonlinearity
    - Finite word length
      - Output
      - Phase truncation
  - -Requires high performance clock
  - -Not suitable for self-excited mode operation.

Selection Table

	VHF/UHF operation (30MHz – 3GHz)	Tight phase tolerance	Lorentz force detuning (self-excited mode)	Driven mode operation	High AM-PM conversion (Class C amplifier)
Direct digital conversion	Need Phase locked down converter	Sample clock jitter	No frequency info	ü	ü
Hybrid I/Q demodulator	ü	ü	No frequency info	ü	ü
Hybrid Amp/phase demodulator	ü	ü	ü	ü	ü
DDSM	High clock frequency	spurs	Slow response	ü	Use Amp/Phase Instead of I/Q
I/Q modulator	ü	ü	ü Zero-th order correction	ü	Limit cycle oscillation
Amp/Phase modulator	ü	ü	ü	Higher PM-AM conversion	ü

Signal Processing: FPGA vs DSP

- FPGA-lots and lots of logic gates
- Faster
  - No microcode
  - Higher clock speed
- Dedicated hardware for each task
  - Each task is assigned its own resources and runs concurrently.
- Difficult to program
  - Steeper learning curve

- Suitable for system with data rate exceeding few MHz and requires little program branching

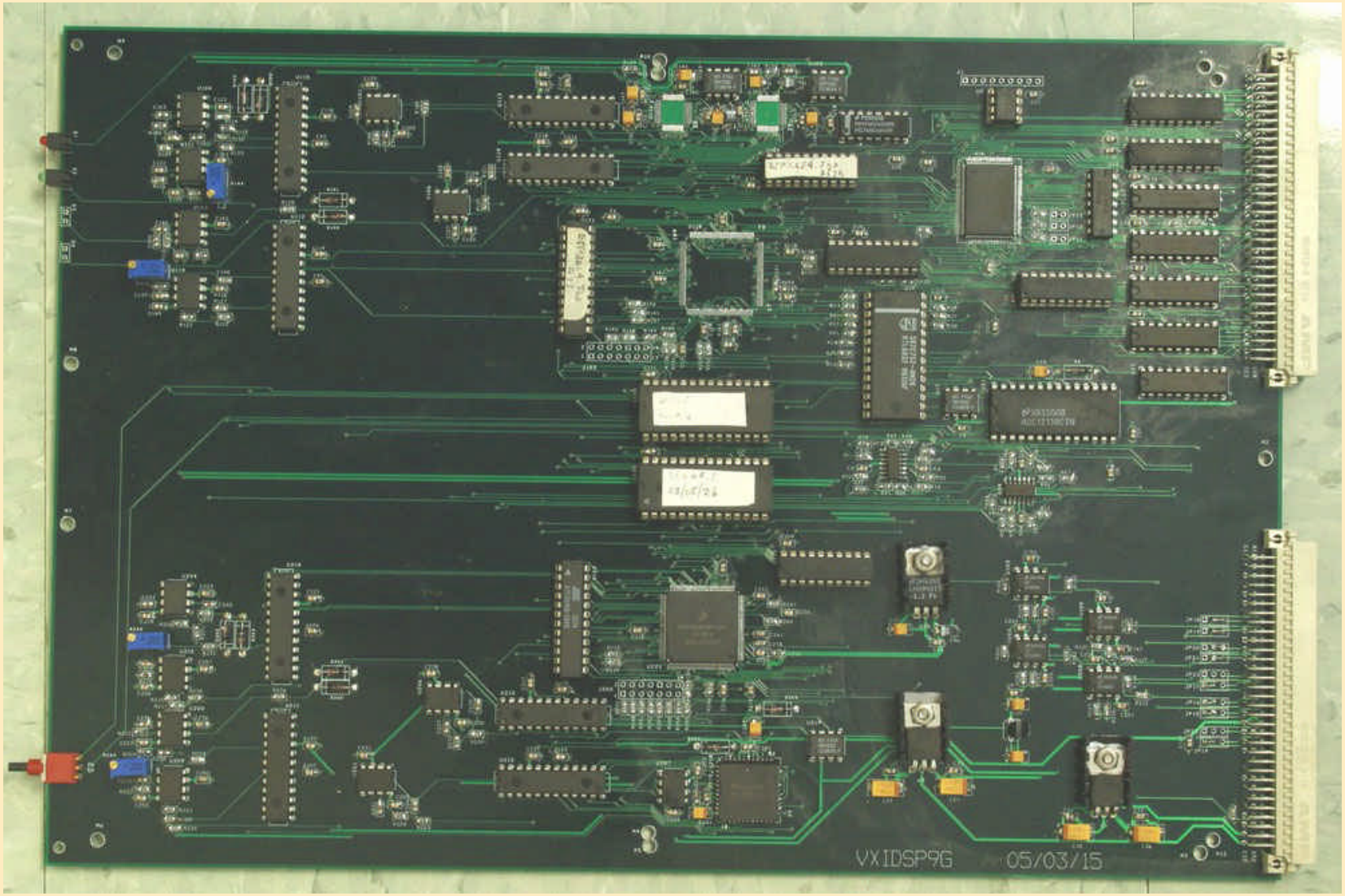
- DSP-specialized microprocessor
- Designed for complex math operations
- Program branching and decision making
- Slower
  - uses microcode
  - Uses shared resource
  - lower clock speed
- More efficiency use of resources
  - Program branching
- Easier to program
  - Steep learning curve

– Suitable for system requiring complex math operation and program branching

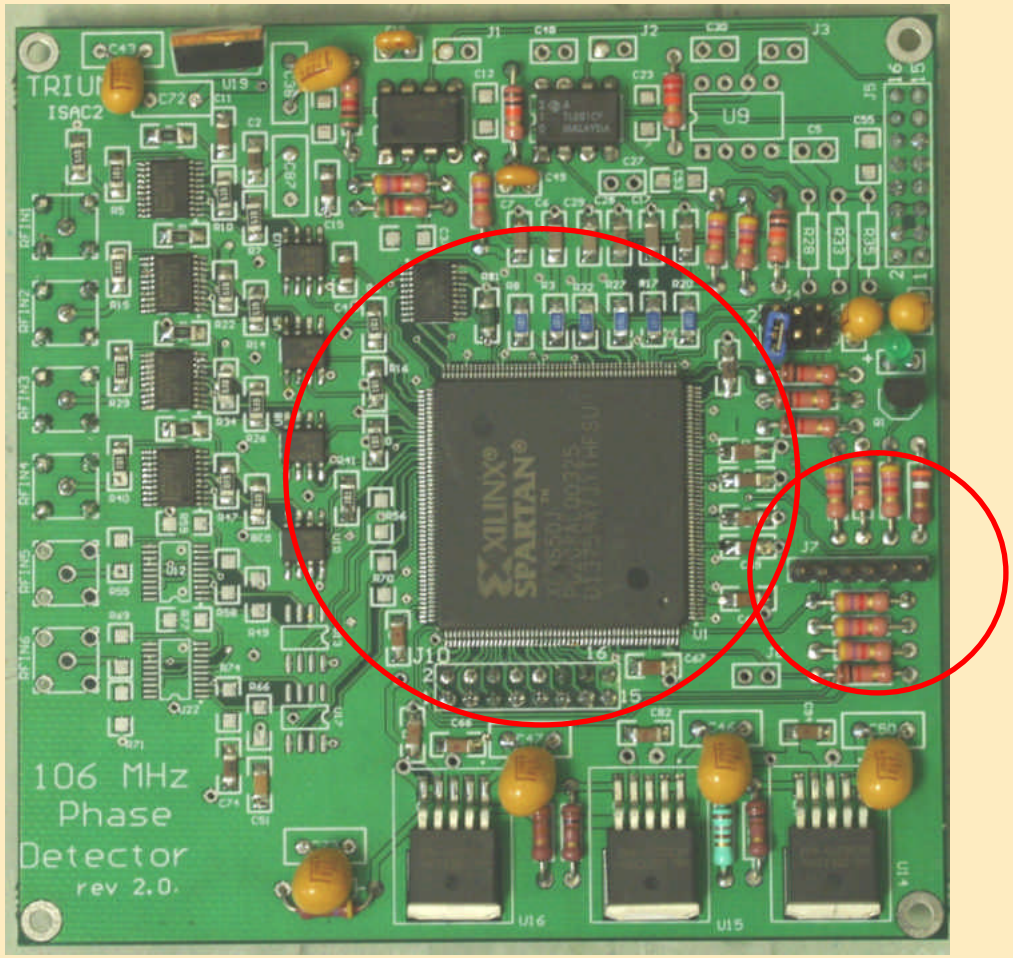
FPGA and DSP represent two very different approaches to signal processing – each good at different things. There are many high sampling rate applications that an FPGA does easily, while the DSP could not. Equally, there are many complex software problems that the FPGA cannot address.

As a result, the ideal system is often to split the work between FPGAs and DSPs.

TRIUMF ISAC VXI DSP board



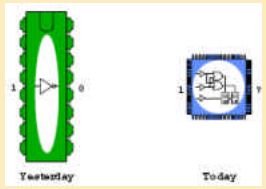
TRIUMF ISAC 2 FPGA phase detectors

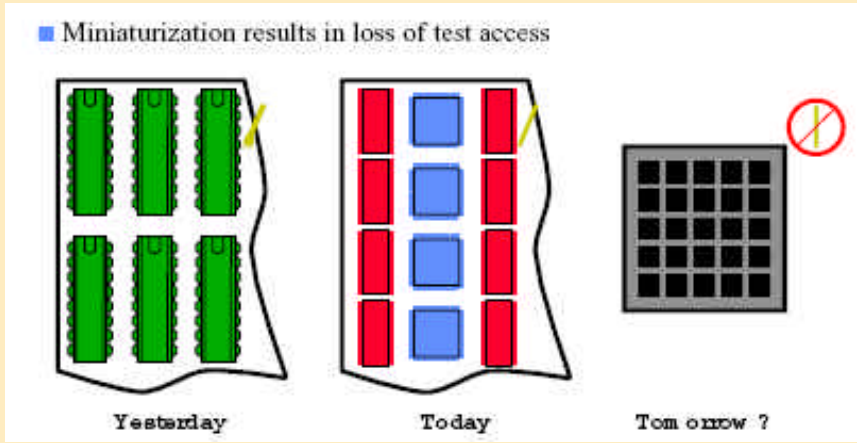


Hardware Self Diagnostic

Self-Diagnostic
A growing problem

- Chips are getting more complex with many I/Qs and different functions within a chip.
  - Test points are not available to functions inside a chip.
- More and more components are being packed into the same area.
  - Difficult to insert a test probe into the board.

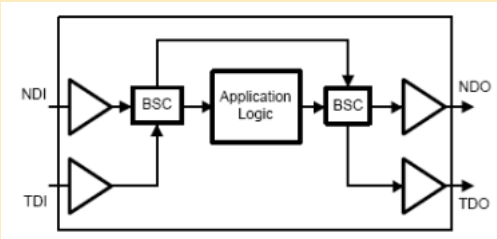


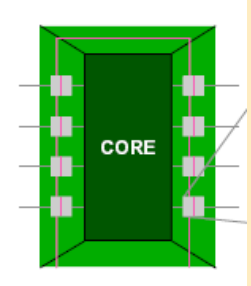


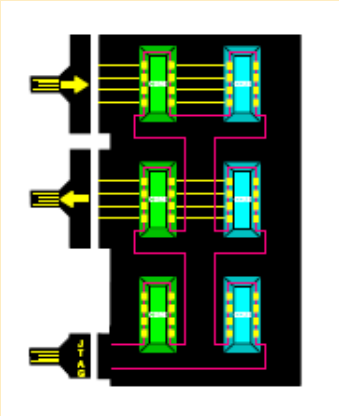
Self-diagnostics

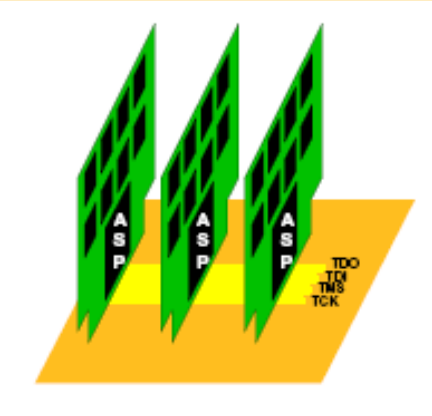
Joint Test Action Group (JTAG)

- IEEE 1149.1 standard entitled **Standard Test Access Port and Boundary-Scan Architecture** for test access ports used for testing integrated circuits and printed circuit boards using boundary scan.
- Use 4 serial lines to scan almost every chip on a board.









JTAG Boundary Scan

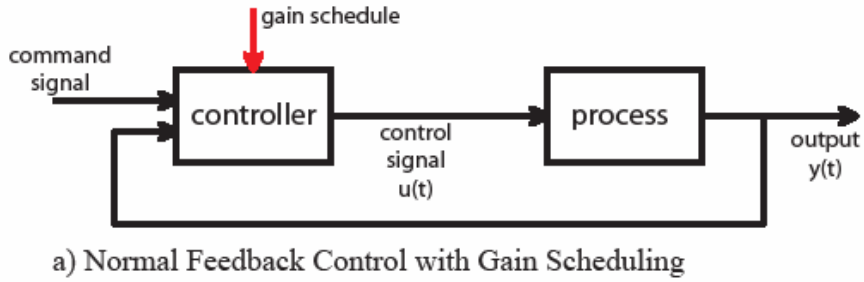
- Scan access to chips, boards and systems
  - Design verification
  - Debug
  - Hardware/software integration
  - Commissioning test
  - Field diagnostics
  - Field firmware upgrade
  - Remote diagnostic
  - Remote firmware upgrade
- JTAG makes self-diagnostic much easier but need software support.

Adaptive controls

Who needs them?

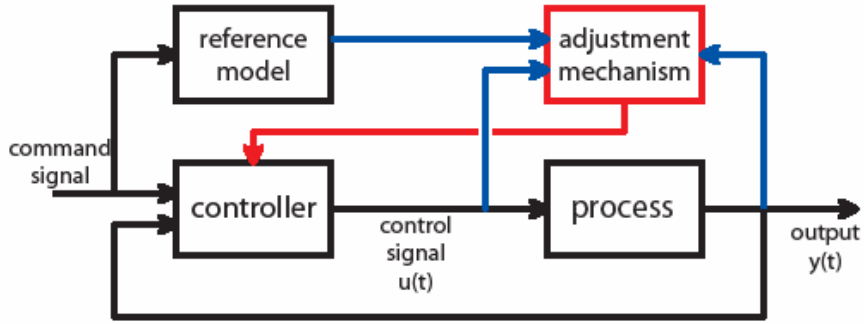
- Different operating conditions
  - Beam loading
  - Different operating frequencies
- Different operating modes
  - Pulse/CW
  - Tuner acquisition and tracking
- Component aging
  - Tube amplifiers

Normal and Adaptive Controls



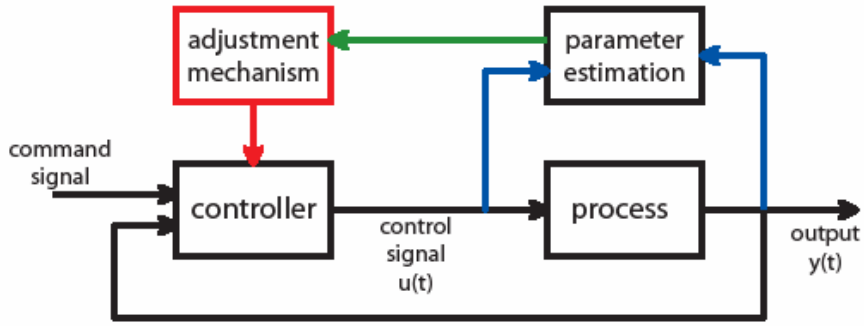
a) Normal Feedback Control with Gain Scheduling

Cavity field control



b) Model Reference Adaptive Control

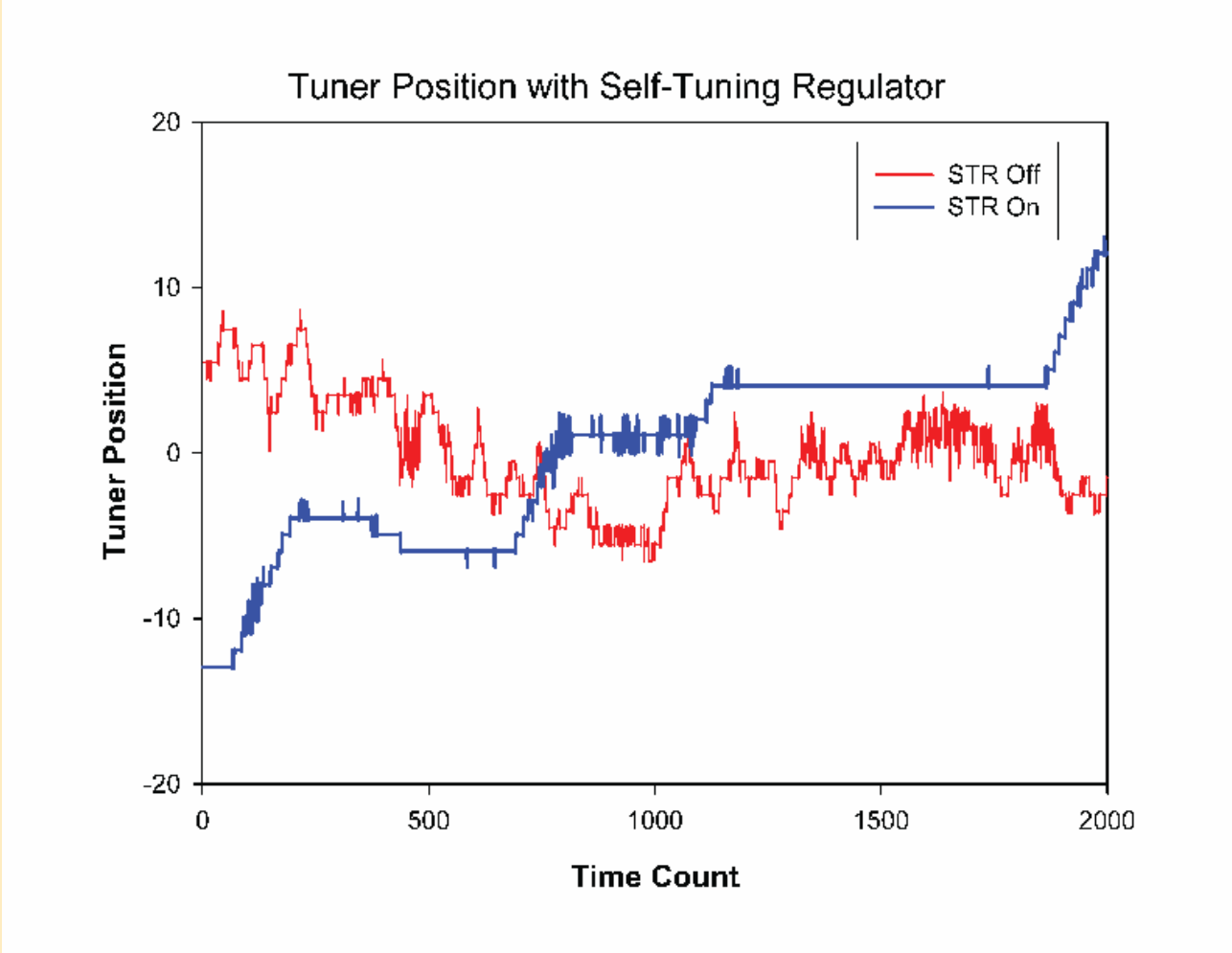
Cavity resonance control
Acquisition phase



c) Self TuningRegulator

Cavity resonance control
Tracking phase

Performance of Self-Tuning Regulator in TRIUMF ISAC 2 cavity



Advances in software
Multi-tasking
Multi-threading

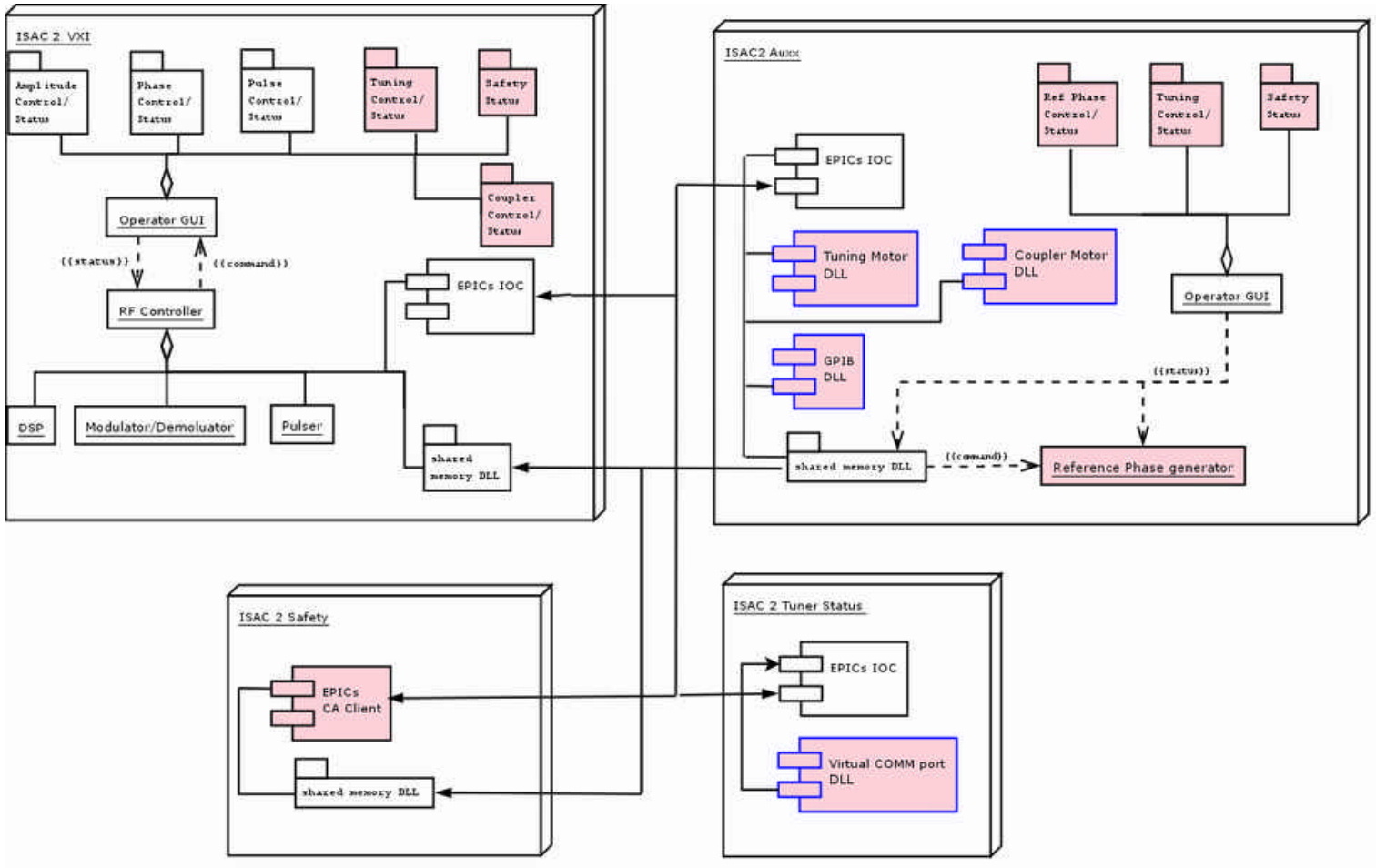
Advantages of Multithreading

- When a program is broken up into threads, each unit is less complex than the whole. As a result, the program is generally simpler, more maintainable and scalable than if it was not threaded.
  - A supervisory control consists of several independent tasks that runs in parallel.
- Prevent Blocking – Synchronous calls are assigned separated threads. The rest of the program does not need to wait.
- Increase Responsiveness- Interrupt driven asynchronous calls are assigned different priorities. Time critical calls are assigned highest priority.
  - Highest priority – Exception handling
  - High priority – Operator interface
  - Normal priority – scheduled tasks (read/write Status)
- Maximize Multiprocessor Performance- different threads are running in different processors.

Disadvantages of Multithreading

- Debugging & testing
  - It is impossible to simulate real time events.
  - Event interaction is difficult to test.
  - Debugging code can affect timings.
- managing concurrency
- porting existing code

Multi-tasking and Multi-threading in TRIUMF ISAC 2 Low Level RF Control



Conclusion

•Advances in hardware and software enable LLRF controls to be built using mostly digital component
•Fully digital system sometimes is not feasible. Certain systems require the use of hybrid system
•Self diagnostic made easily with JTAG. New designs should incorporate JTAG in the system level.
•Use of adaptive control can enhance tuner performance.
•Use of multi-threading in a true multi-tasking OS make the LLRF control much more time-responsive.