

CERN'S LEIR DIGITAL LLRF: SYSTEM OVERVIEW AND OPERATIONAL EXPERIENCE

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Abstract

The Low Energy Ion Ring (LEIR) is an accumulation and acceleration ring in the Large Hadron Collider (LHC) ion injector chain. After its successful start in 2005, it has been running in three operational campaigns. The LEIR low-level RF (LLRF) system is the first all-digital LLRF to operate in a CERN circular machine. Its capabilities include beam control tasks as well as dual-harmonic cavity voltage/phase servoing. All the system control parameters are fully configurable, remotely and in-between cycles; extensive built-in observation capabilities and diagnostics are available. The system is flexible, powerful and extremely reliable. This paper outlines the main building blocks and operational features, along with results obtained during the first years of operation.

INTRODUCTION

LEIR [1] is a 78 m long accumulation and acceleration ring in the LHC ion injector chain. It began operation in 2005 with O^{4+} particles then switched to Pb^{54+} ; the use of lighter ions is also foreseen. LEIR turns low-intensity ion pulses injected from CERN's Linac3 into high-density bunches which are accelerated from 4.2 MeV/u to 72 MeV/u. Two Pb^{54+} operational schemes are specified: EARLY and NOMINAL. In the EARLY scheme one Linac3 pulse is accelerated at harmonic one and $2.25 \cdot 10^8$ ions are extracted. In the NOMINAL scheme, five Linac3 pulses are accumulate and accelerated at harmonic two; $9 \cdot 10^8$ ions are extracted. The revolution frequency (f_{REV}) range for Pb^{54+} operation is 0.361 MHz (capture) to 1.423 MHz (extraction). The synchrotron frequency (f_s) range is 600 Hz to 2 kHz. The acceleration phase lasts about 1 s, with a maximum dB/dt of 1.5 T/s. LEIR is reliable and its performance is reproducible: this is partly due to its new low-level RF (LLRF) system.

SYSTEM OVERVIEW

The LEIR LLRF is the first all-digital LLRF system to operate in a CERN circular machine. It is dual harmonic and acts on the single, non-tunable, wide-band, Finemet-based [2] cavity in the ring. The rather high f_s calls for a high beam phase loop bandwidth; the wide f_{REV} sweep requires a special sampling frequency treatment. Initial test results on a different machine are given elsewhere [3].

System Architecture

Figure 1 shows the system architecture and input/output signals. The main building blocks are the Digital Signal Processor (DSP) carrier board and three different types of daughtercards: the Master Direct Digital Synthesizer (MDDS), the Slave Direct Digital Synthesizer (SDDS)

and the Digital Down Converter (DDC). Each DSP carrier board hosts two daughtercards, making the system flexible and modular. All blue-drawn modules and the three daughtercards are specific to the LLRF system: they are built, programmed and maintained by the RF group. Three DSP carrier boards, called DSPA, DSPB and DSPC, co-operate to implement the LLRF functionalities. They exchange data via ADI-proprietary fast digital links (linkports™) and receive input signals as well as machine-related timings from the Rear Transition Modules (RTMs) and from the on-board daughtercards. The timing pulses are generated by standard Controls Timing Receivers (CTRV). The DDC daughtercard performs digitisation, low-pass filtering and decimation. The SDDS generates RF analogue signals of programmable f_{REV} harmonic and phase. Data acquisition and control are done in {I,Q} coordinates. The Cavity Control Interface (CCI) implements the interface with the High-Level RF (HLRF) system. The MDDS generates a clock (MDDSC) at a high, power-of-two harmonic of f_{REV} . This signal clocks all daughtercards and its harmonic number is changed within each cycle to maintain the daughtercard clock in the 40 to 80 MHz range. The MDDSC is single- and double-tagged to synchronise changes system-wide. It is distributed via the Tagged Clock Fanout (TCF) module. Real-time (RT) processes running on the Power PC (PPC) board implement the LLRF-to-controls interface.

System inputs and outputs are also shown in Figure 1. DSPA receives Σ and Δ signals from two Transverse Pick-Ups (TPU), to calculate the radial position. It also receives the B_{up} and B_{down} trains, which give the bending magnetic field B variation in units of 10^{-5} T, to implement the frequency program. DSPA generates RF trains at programmable harmonics. DSPB receives the Phase PU and the extraction reference signals to implement the phase and extraction synchronisation loops, respectively. DSPC receives two harmonics of the gap return signal and supplies two analogue RF signals, one per controlled harmonic of the cavity. These are sent to the CCI board to be analogically summed and sent to the HLRF.

System Capabilities

The available capabilities are frequency program, radial loop and RF trains generation for DSPA; phase and extraction synchronisation loops for DSPB; cavity voltage and phase loops at RF harmonics one and two for DSPC. The SDDS DAC's current references are real-time switched to allow a high dynamic range control. The cavity is short-circuited by a gap relay when no voltage is applied to it, thus preventing the beam from self-bunching owing to the cavity impedance.

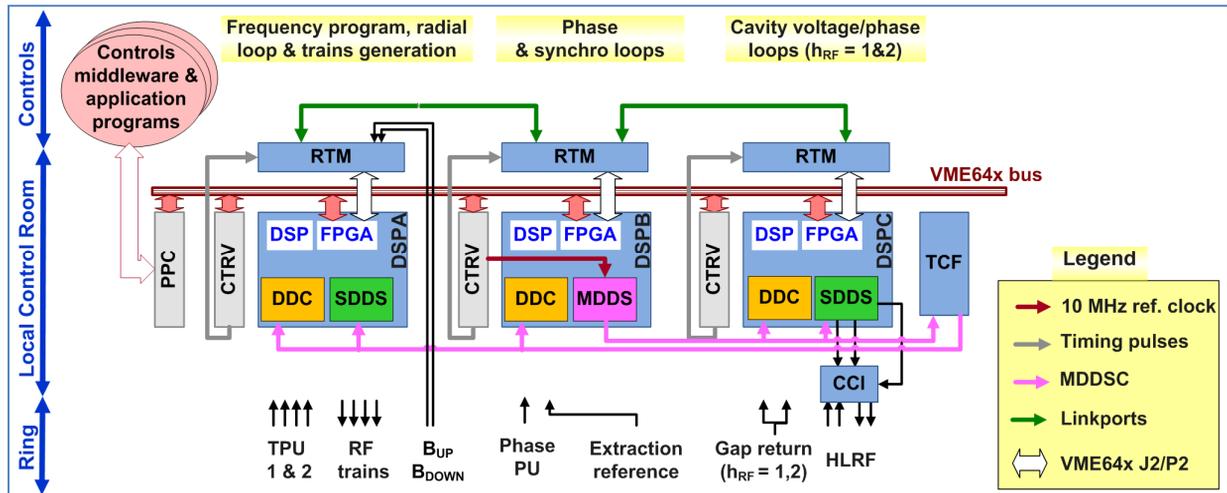


Figure 1: LEIR LLRF - schematic view. Keys: MDDS – Master Direct Digital Synthesiser (DDS); SDDS - Slave DDS; DDC – Digital Down Converter; CCI – Cavity Control Interface; MDDSC – Tagged Clock; TCF – Tagged Clock Fanout; TPU –Transverse Pick-Up; HLRF – High-Level RF; CTRV – Timing Receiver Module; PPC – Power PC; B_{up} , B_{down} – measured magnetic field.

The sampling period is 15 μ s for beam phase, extraction and cavity voltage loops; it is 120 μ s for the radial loop. The phase loop is AC-coupled, with a cut-off at 10 Hz. Frequency-dependent rotation of the beam phase and cavity signals is implemented by software. All the system's control parameters are fully configurable, remotely and in-between cycles; extensive built-in diagnostics and observation capabilities are available.

HARDWARE

The DSP motherboard is a 6U, double-slot VME board with a 32-bit slave interface. It hosts four Field Programmable Gate Arrays (FPGAs), one floating-point ADSP21160 DSP and two memory blocks, visible from the VME bus. The RTM is a 6U VME board located in the rear part of the crate; it interfaces with the DSP motherboard via the VME64x J2/P2 connector. The CCI is a NIM module interfacing with the SDDS via a parallel digital link. The MDDSC carries the AD9858 1 GHz DDS; the MDDSC can reach 160 MHz and is distributed via Firewire cables and connectors. The four-channel DDC carries four 14 bit, 80 MHz AD9245 ADCs. The four-channel SDDS carries four 14 bit, 125 MHz AD9754 DACs. One Stratix EPS20 FPGA is hosted by each daughtercard and implements the signal processing. The LEIR HLRF is described elsewhere [2].

SOFTWARE

FPGA

The DSP carrier board FPGA code implements addressing and simple signal processing functionalities. The DDC FPGA code includes a programmable, decimating Cascaded-Integrator-Comb (CIC) filter, thus minimising the group delay. The SDDS FPGA implements cavity-related safety logic. The MDDS FPGA carries out MDDSC programmable tagging.

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DSP

The interrupt-driven DSP code implements all beam and cavity loops, as well as extensive diagnostics data acquisition and alarms, software timings and vector-based reference functions. Three separate codes are deployed, one for each DSP carrier board. Each code implements the board specific functionalities as well as common functions, such as the daughtercard interfacing and the software timings or reference function generation.

Front-end

The many processes are split into a server part, interfacing to the controls middleware, and a RT part, managing the VME hardware. The processes are triggered by interrupts derived from machine-related timings.

Application Programs

The LLRF system is fully integrated within the controls infrastructure and several application programs are used for parameters setup and display. Plots from some of these applications are shown in Figure 2 (virtual scope plots) and Figure 3 (Tomoscope plot). Other applications include for instance synoptics to define RF-specific parameters, such as the shape loop correctors, and to display alarms and diagnostics information.

OPERATIONAL EXPERIENCE

LLRF Performance

The LLRF system has operated successfully in four operational campaigns so far. Beam capture at beam harmonic one or two, double-harmonic acceleration and synchronized extraction have been routinely carried out. The system has shown to be flexible as well as reliable: these features are extremely useful especially in view of the high beam availability required by LHC operation.

Figure 2 shows machine (upper plot) and LLRF-generated (lower plot) data for a NOMINAL beam cycle. The multiple-injections are clearly visible on the upper plot; the lower plot shows the radial position steered to zero mm, the cavity-to-beam phase and the magnetic field obtained by summing B_{up} and B_{down} trains.

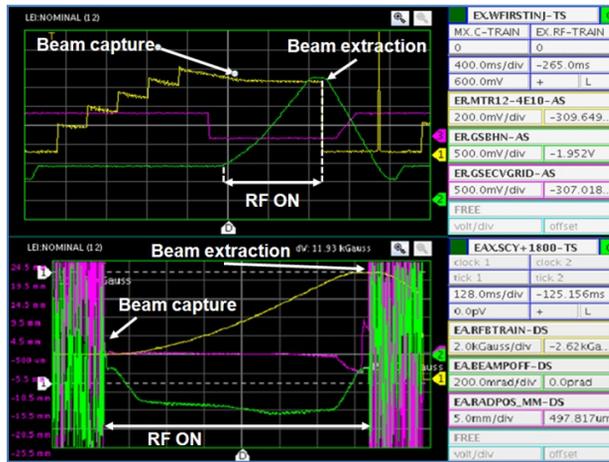


Figure 2: Upper plot: beam intensity (yellow), magnetic field (green). Lower plot: radial position (violet) cavity-to-beam phase (green), magnetic field (yellow).

Dual Harmonic Operation

Dual harmonic operation aims at improving the bunching factor, i.e. the ratio between average and peak beam current. It flattens the bunch, thus reducing the transverse space charge tune shift. This is required by the high intensity associated to the NOMINAL scheme: here capture and acceleration at beam harmonics two plus four are needed. Figure 3 shows the Tomoscope plot [4] of a beam accelerated with double-harmonic. The picture was taken during the acceleration and the second harmonic component was slightly magnified for the set-up phase.

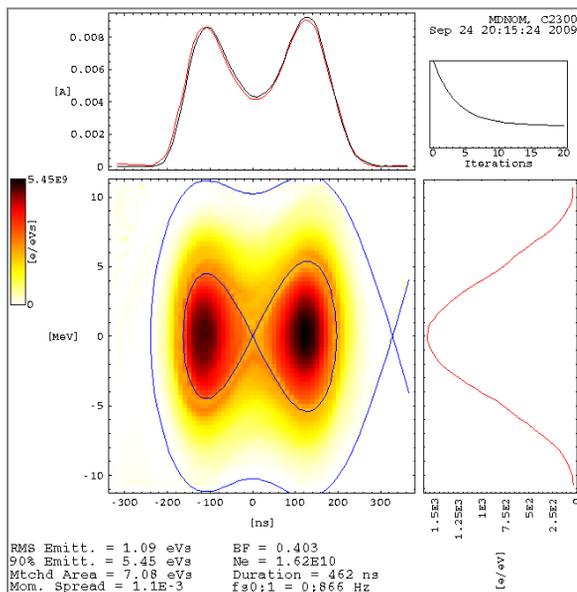


Figure 3: Tomoscope plot for double-harmonic operation.

Synchronisation at Extraction

The deployed extraction synchronisation process consists of two steps: a synchronisation in frequency followed by a synchronisation in phase. In the first step, the beam is brought to a pre-determined beating frequency with respect to the reference signal. In the second step, the difference between the phases of the beam and reference signals is brought to zero. The synchronisation phase loop remains active until the beam is extracted, thus guaranteeing that the two signals remain synchronised. The extraction reference corresponds always to the LEIR beam harmonic 1. Figure 4 shows the last part of the beam cycle for an EARLY user; the synchronisation process starts at time 1650 ms and the beam is synchronised after about 20 ms. The flexibility of the LEIR LLRF system allows one to select different synchronisation algorithms on a per-cycle basis; faster schemes are under study.

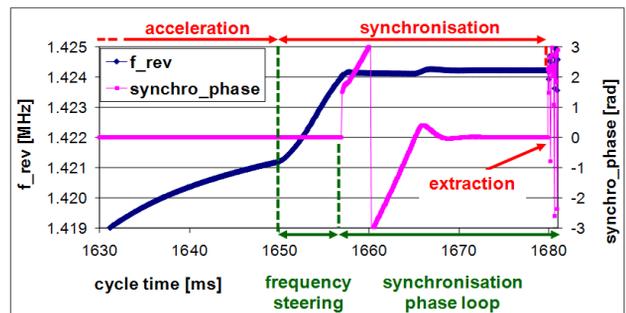


Figure 4: extraction signals - synchronisation phase (pink) and f_{REV} (blue).

CONCLUSIONS AND OUTLOOK

The LEIR LLRF has been successfully operating since 2005. It has proven to be powerful, flexible and reliable. The LEIR LLRF system is important not only “*per se*” but also as the pilot project to extend the same digital technology to other CERN synchrotrons. A project to renovate the four-ring PS Booster was launched in 2008 and plans and initial results reported [5].

REFERENCES

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