DEVELOPMENT OF GATED TURN-BY-TURN POSITION MONITOR SYSTEM FOR THE OPTICS MEASUREMENT DURING COLLISION OF SUPERKEKB

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Abstract

Gated turn-by-turn monitor system to measure optics functions using non-colliding bunch has been developed for SuperKEKB accelerators. With the fast, glitch canceling beam switch, beam position of the target bunch will be measured without affecting the fine COD measurement using narrow-band detectors. The gate timing and the bunch position detection are controlled by the Spartan-6 FPGA. The performance of the system, such as the gate timing jitter, data transfer speed from the system to EPICS IOC and the noise effect to the downstream narrow-band detector are reported.

INTRODUCTION

The upgraded electron-positron collider SuperKEKB is currently being constructed. About 40 times larger luminosity than that of KEKB, 8 x 10^{35}/cm^2/s, is designed to be achieved by employing so called nano-beam scheme, that is to reduce the vertical beam size at the interaction point (IP) by the low emittance lattice and strong final focusing, and doubling the beam currents in both ring while keeping the normal bunch length. In the real operation, it is essential to keep both the x-y coupling and the vertical dispersion with lowest limit to get the designed beam size at IP. Since the disturbance in betatron function yields both rapid reduction of the dynamic aperture and the increase of the vertical emittance, measurement and correction of the beta-beating is also very important.

In KEKB, we had measured the betatron functions and x-y couplings by the single-kick method with non-colliding, low beam current conditions (~30 mA) [1,2]. The dispersion functions had been measured by shifting the RF frequency on the same low beam current conditions. For the SuperKEKB, we plan still to use the similar methods to measure the fine optics functions with a little bit larger beam current, typically 100 mA for better accuracy. To realize the designed optics, it is also desired to measure the optics functions, especially betatron functions and x-y couplings, during collision with existing huge beam current without disturbing the collision. It is obvious we will not be able to use the single kick method under such conditions with large beam current. We might be able to measure the betatron phase advance and x-y couplings by exciting a bunch with betatron frequency and measure the amplitude and phase of the oscillation using turn-by-turn monitors (TbT). Nevertheless there lie several difficulties with the method. Since we always need strong transverse (horizontal and vertical) bunch-by-bunch feedback in both ring to stabilize the coupled-bunch instability under large beam current, it is fairly difficult to excite and measure betatron oscillation. Also huge beam-beam tune spread due to collision should suppress betatron oscillation strongly.

In KEKB, we had prepared a non-colliding bunch, without transverse feedback as a pilot bunch just after the main colliding bunch train (4 ns or 6 ns) to measure betatron tunes during collision. For SuperKEKB, we plan to excite the pilot bunch with the betatron frequency (horizontal or vertical) using PLL excitation function of iGp12 digital feedback filter [3] and measure the oscillation of the pilot bunch at selected BPMs using fast gated turn-by-turn monitors. The design and the performance of the TbT monitor systems are reported. Table 1 shows the related parameters of the SuperKEKB rings (LER and HER).

Table1: Main Parameters of SuperKEKB Rings

	HER	LER
Energy (GeV)	7	4
Circumference(m)	3016	
Beam current (A)	2.6	3.6
Number of bunches	2500	
Single bunch current (mA)	1.04	1.44
Bunch separation (ns)	4	
Bunch length (mm)	5	6
RF frequency (MHz)	508.887	
Harmonic number	5120	
β* at IP hor./ver. (mm)	25/0.30	32/0.27
Hor. emittance (nm)	4.6	3.2
X-Y coupling (%)	0.28	0.27
Vertical beam size at IP (nm)	59	48
Rad. damping time T/L (ms)	58/29	43/22
Number of BPMs	466	444
Number of TbT monitors	135	135

DESING AND PERFORMANCE OF THE GATED TURN-BY-TURN MONITOR

The turn-by-turn monitors will be inserted between the BPM heads and the normal narrowband beam position

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detectors and will be placed in the same local control rooms around the rings. Therefore the required characteristics of the system will be as follows:

- It should not disturb the measurements of normal narrowband detectors too much. Noise from the monitor, especially switching noise from the fast gate should be suppressed as much as possible.
- The rise and fall time of the gate need to be short enough to distinguish the bunch signal to cope with the minimum bunch separation of 4 ns. Also the isolation to the turn-by-turn line should be large enough to reject the large power (70dB larger) coming from colliding bunches.
- The system should be compact, all-in-one package to save the mounting space and the fabrication cost.

The block diagram of the gated turn-by-turn monitor system is shown in Fig. 1. It has four independent channels corresponding to four BPM electrodes. Each channel has a fast gate switch, 508 MHz band-pass filters (BPF), low noise amplifiers (LNA, HMC616) with total gain of 40 dB, a logarithmic amplifier (ADL5513), a peak-holding circuit with reset timing input, and a 14 bit ADC (ADS850). All the timing generation and the data process is done by the Spartan-6 FPGA (XC6SLX100T-3FGG484) with 128 MB DDR3 SDRAM. The data and the command is transferred through Gigabit Ethernet interface. All the system is installed in a 1U size box as shown in Fig. 2.

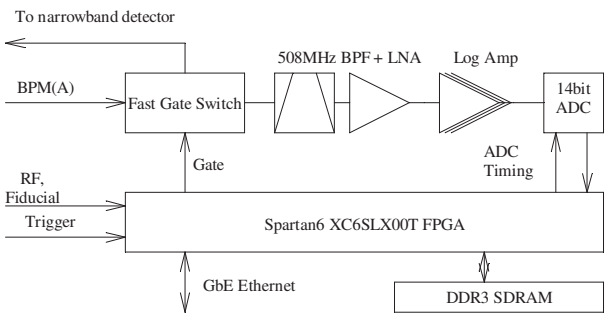

Figure 1: Block diagram of the gated turn-by-turn detector.

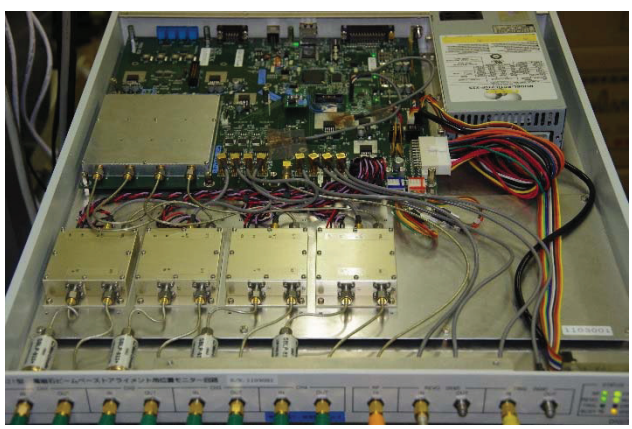

Figure 2: Photo of the Type-1421 gated turn-by-turn monitor (prototype).

Fast Gate Switch

Hittite HMC232LP4 has been selected as a SPDT IC. As the measured switching noise was large, typically 70 mV peak to peak, and the isolation was not so fantastic, less than 67 dB, we have employed a switching-noise cancelling method [4] which combines 4 SPDT ICs and three 180-deg hybrids as shown in Fig. 3.

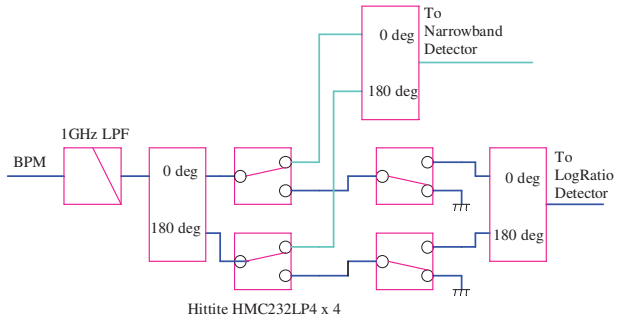

Figure 3: Block diagram of a fast noise-cancelling switch.

The switching noise is subtracted using two pairs of 180-deg hybrid, while BPM signal is summed with the same polarity to reduce the insertion loss. For the turn-by-turn measurement, two stages of the SPDT switch are used to

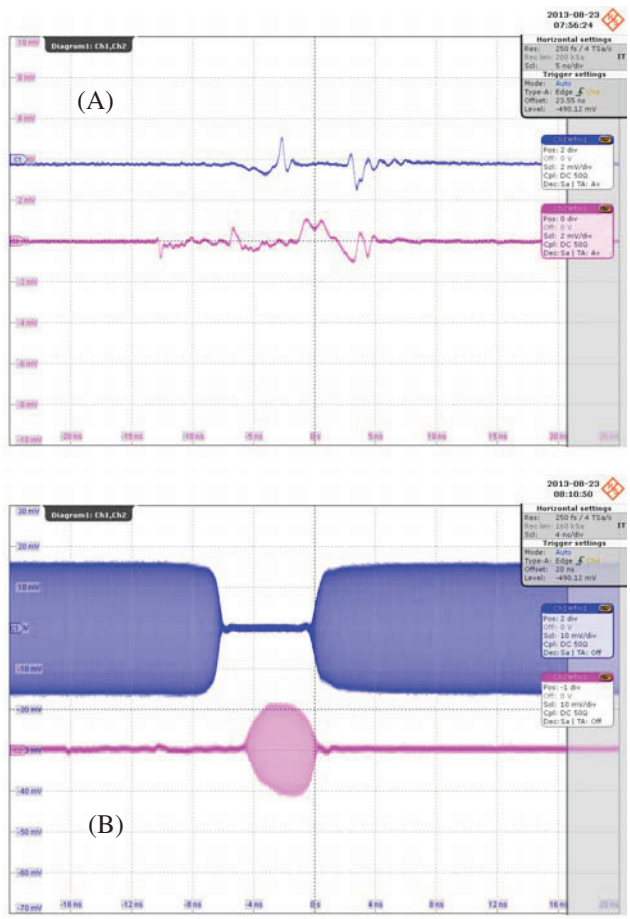

Figure 4: (A) Switching noise; upper trace: to narrowband detector, lower trace: to TbT detector. (B) Switch response for 4 ns gate input with the RF input level of -20 dBm.

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enhance the isolation. Figure 4 shows the switching noise and rise/fall time of the switch. The noise has been well suppressed down to 2 mVpp in both channels. The rise and fall response is about 0.6 ns and is short enough for 4 ns bunch separation. The measured insertion loss and the isolation around 508 MHz to narrowband channel is 2.7 dB and 63 dB, respectively, and those to TbT channel is 4 dB and 80 dB, respectively.

Gate Timing Jitter

Four gate signals to the fast gate switches are created in the Spartan-6 FPGA from ring RF signal and the fiducial. For a better timing jitter, external D-FFs are used to resynchronize the timing signal to RF timing. Also, digital delay chips (EP195) are used to adjust fine gate timing with a step of 10 ps. The width of the gate is also created in the FPGA using RF timing. The switch can be (a) bunch extraction mode, (b) inverse of the bunch extraction mode (a); most of the signal goes to TbT channel, (c)Off; all signal goes to narrowband channel (d) DC on; all signal goes to TbT channel.

The timing jitter has been measured using histogram function of a sampling scope with a bandwidth of 20 GHz by comparing the RF signal and the gate signal. Figure 5 shows distribution of the mean position and the jitter width in standard deviation. The jitter is around 3.2 ps and the mean timing offset stays within 20 ps, which is of course small enough for our purpose.

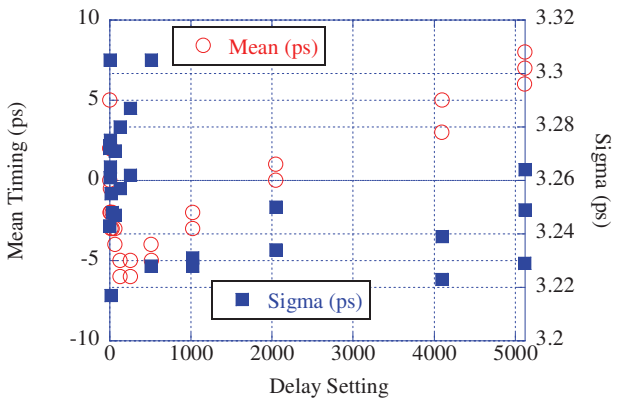

Figure 5: Distribution of mean delay position relative to RF timing (left) and jitter in standard deviation (right) with delay setting (2 ns step, from 0 to 5119).

Linearity and Dynamic Range

Since the system is expected to be usable to measure the injection orbit, the minimum bunch charge to be detected is less than 0.5 nC, while the nominal bunch charge will be around 15 nC during collision. We have examined the response of the BPFs and the same logarithmic-amplifier with 20 dB LNA using a test BPM installed in PF-AR where the bunch charge was 69 nC and the size of the BPM chamber and the button head are similar to those of normal SuperKEKB LER BPM. Figure 6 shows the output of the Log amplifier with two kinds of BPF, wide-band, low Q filter with bandwidth of 24 MHz and a narrowband filter with bandwidth of 5 MHz. Considering the chamber size of the various monitor chambers in SuperKEKB rings, the minimum charge with the largest BPM (diameter of 150 mm) corresponds to -43 dB and the maximum charge with smallest BPM (diameter of 90 mm) corresponds -8 dB. As it is possible to limit VBW to reduce the scattering of the output after log-amplifier in case of narrowband filter, we have decided to use narrowband BPFs with two stages of LNAs, with total gain of 40 dB.

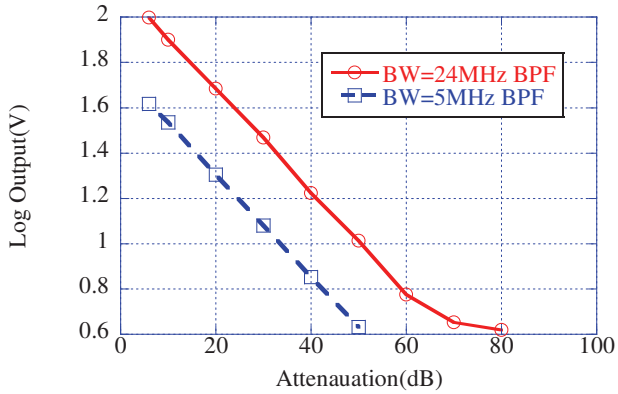

Figure 6: Log-amplifier response of a single bunch charge of 69 nC.

Fine response of the system has been measured with 508.886 MHz CW as input and fast gate switch as inverse bunch extraction mode(b) as shown in Fig. 7 where the standard deviation has been calculated for the input of 2048 turns of data.

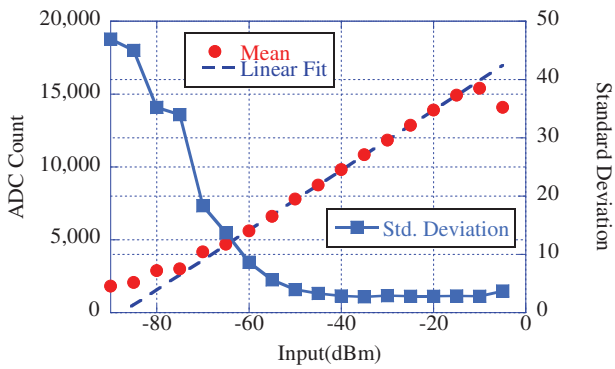

Figure 7: ADC counts and its standard deviation for CW RF input.

The standard deviation of the ADC for the RF input from -50 dBm to -10 dBm is roughly 3 counts. In case of LER normal BPM, it corresponds to about 30μm. In reality, as we will make FFT for many turns of position and the result of FFT is not so sensitive to random jitter of the data, much larger standard deviation might be acceptable.

Board Control and Data Transfer

Giga-bit Ethernet connection is used to control the system. On the Spartan6 FPGA, MicroBlaze is used to handle the command from the server and to transfer the data to the server. Several status monitors such as the input status of RF clock, Fiducial and trigger, voltage of power supplies, temperatures including FPGA have been working.

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Also, 16-bit I/O of LvTTL level can be used to control other devices. The 4-ch raw data (14 bit) and rough X-Y position data (IEEE single floating format) are stored on the DDR3 SDRAM. The maximum number of position data stored on the memory is about 1M turns, which corresponds to 10 s in Super KEKB. Part of the SDRAM is used by MicroBlase system itself.

For the control server, CentOS 6.4-x64 on Xeon E3-1220v2 (3.1GHz 4 core) with 16 GB memory is used. We have installed EPICS system (R314.12.1)[5] with ASYN driver (asyn4-21) on the server. Also Control System Studio (CSS) has been installed for the graphical user interface on the test bench. We plan to install the server to all the local control stations (20 stations around the ring), which will be needed to handle about 12 to 16 TbT systems in the final configuration. Though we plan to process the data on the server, to calculate the position using calibration data, or to make FFT to get betatron phase advance between TbTs, the processing speed will not be the rate-limiting step to the whole optics correction procedure if the data transfer speed is not so slow, because of much complicated and time-consuming processing to estimate and correct the optics error.

The data transfer rate has been measured and been found unexpectedly slow on the prototype system. We have used 2nd GbE port of the server to connect the TbT system through GbE switching Hub where no other connection existed. To transfer 0.5 M turns of data of 4-channes, it took about 44 s. Even by taking into account the data structure, the data transfer rate is only 2 Mbit/s. Though for injection tuning, typically less than 32 turns of data transfer, or short data around 4k, that slow transfer might be acceptable, it is surely stupid to wait longer transfer time during operation. As it is suspected that the MciroBlaze is the main time-limiting principal, we are now working to implement SiTCP [6] where the data transfer rate of almost 900 Mbit/s might not be so difficult.

Noise to Narrowband Detector

The switching noise added on the narrowband line is confirmed to be negligibly small compared to the beam signal from BPM using a spectrum analyser. It is nevertheless worried that this system might affect the narrowband detector on the VXI crate because of fairly lower level of the detection, typically -60 dBm for 508 MHz or 1071 MHz beam signal. As the RF level of data receiver on the board for 508 MHz RF clock is almost 0 dBm, clock distribution lines or fiducial lines might radiate unwanted RF or 2xRF E-M wave. We have checked the rough radiation level of the first prototype using a spectrum analyser with an antenna with good sensitivity around 508 MHz. Though the radiation level was much lower than other common devices such as power amplifiers or frequency dividers with the form factor of NIM, we will add additional shielding to suppress the leak signal. In addition, by installing the system in the different rack separately from the rack where the VXI systems have been installed, we expect further isolation though the cable length between the TbT system and the VXI narrowband system becomes much longer than the case of installing the TbT system near the VXI system.

FUTURE DEVELOPMENT

We are now installing the SiTCP to jump-up the data transfer speed. To store the MAC address on an EEPROM with SPI-IF, some modification on the board will be needed. Also, we will fix other mistakes on the board on this occasion. With SiTCP, it might be possible to omit the MicroBlaze system which introduce unnecessary difficulty such as the complexity on the boot ROM to the system. As it might be convenient to store several parameters such as delay setting of each fast switch on EEPROM and automatically set when booted, we will also add the record function of the parameters to EEPROM. Though the system has JTAG IF accessible without opening the box, it is not good idea to upgrade the FPGA firmware of many TbT systems using each JTAGs at local control rooms. We are implementing the firmware update method through Ethernet connection.

SUMMARY

We have designed and tested the turn-by-turn BPM detector with fast gate switches to extract the beam signal of the pilot bunch without disturbing the COD measurement using a narrowband detector placed downstream of the system. The residual noise of the gate switch is small enough and is expected not to disturb the downstream system. The timing control using FPGA has shown excellent performance. Jitter of the turn-by-turn position has estimated to be small enough for optics measurement. As the data transfer rate is not excellent, we plant to achieve very fast transfer rate using SiTCP technology.

The technology of fast gate switch with noise cancelling has been developed by Prof. T. Naito and Prof. T. Ieiri. We would like to express our sincere application to Prof. T. Obina for the support on the EPICS system and SiTCP system. We thank our colleague of SuperKEKB beam instrumentation for numerous support on the development.

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