

THE CSS STORY

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Abstract

Control System Studio (CSS) is designed to serve as an integration platform for engineering and operation of today's process controls as well as machine controls systems. Therefore CSS is not yet another replacement of existing operator interfaces (OPI) but a complete environment for the control room covering alarm management, archived data displays diagnostic tools and last not least operator interfaces. In addition we decided to use CSS as the platform for the whole engineering chain configuring EPICS based process control databases, configuring and managing the I/O, editing state notation programs, configuring role based access rights and many more. Due to the ease of use of CSS as an Eclipse based product, we decided to use the CSS core also for all our stand alone processes. This helped us to reduce the diversity of running products/ processes and simplified the management. In this presentation we will describe our experience with CSS over the last two years. How we managed the transition from old displays to new ones, how we changed our alarm/ message philosophy and last not least which lessons we learned.

INTRODUCTION

The development of a new tool set was initiated by the new project at DESY – the European XFEL. This project will lead us through the next decades to come. All existing hard and software for cryogenic and utility controls had to go through a verification process to decide whether components can pass 'as is' or whether they have to go through a process of refurbishment or even new design.

For the existing operator tools it was soon clear that they have to be replaced by a new tool set.

NEW TECHNOLOGIES FOR NEW OPERATOR TOOLS

To prepare the new tool set for the future it was decided to use Java as the programming language. The next question to be answered was: Which development environment tool shall be used? This covers also the question about the core technologies to be used. Two candidates were investigated: Eclipse and NetBeans.

At the time when Eclipse 3.1 was launched it was chosen for the CSS core technologies. Many more basic technology decisions had to be made. These were identified in a workshop about three years before the first beta release of CSS.

INITIATING COLLABORATION

As a result of the workshop the CSS collaboration was started between the initial partners DESY and SNS. In addition two companies were involved in the exploration of new technologies. But what is the best way to explore the new fields? How can one set up a contract with a company when the details cannot be specified? We had to walk on new ground with respect to contracting and project management. New techniques known from extreme programming were used to setup and run these development projects.

WATERFALL OR XP?

This is not a question any more. Waterfall specifications are by definition always out of date and are outdated. But which kind of extreme programming shall be followed? A very basic concept is working in iterations. Iteration steps are small they last only a few days or weeks. The work to be done in these steps is defined in tasks. The results are checked after each iteration step. Especially when new technologies must be explored it is important to stay in close contact and verify that the team is still on the right path. Waterfall – or long iteration steps will fail in this respect.

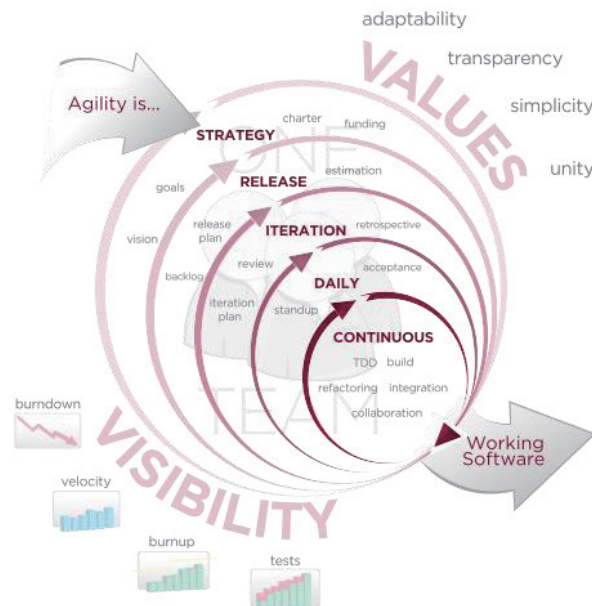


Figure 1: The Agile Methodology ©

Web2cToGo: BRINGING THE Web2cToolkit TO MOBILE DEVICES

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Abstract

The Web2cToolkit is a collection of Web services. It enables scientists, operators and service technicians to supervise and operate accelerators and beam lines through the World Wide Web. The toolkit includes a synoptic display viewer and editor, an archive viewer, a messenger service, a logbook facility, an administration manager and an HTTP gateway to control systems. Recently, a novel view (Web2cToGo) has been added which is especially designed for mobile devices such as tablet computers or smartphones running iOS, Android or other mobile operation systems. Web2cToGo is a frame which embeds instances of all kinds of Web2c tools. It provides a single-sign-on user authentication and authorization procedure. Web2cToGo supports single- or multiple-touch user gestures and is available as a platform-independent browser-based Web application or as a platform-dependent native app. This paper describes the conceptual design of Web2cToGo and the technologies used behind the scenes as well as the experiences gathered so far. It presents an outlook of on-going developments including user-device interaction based on voice recognition.

INTRODUCTION

The Web2cToolkit [1] [2] is a collection of Web services including

- (1) *Web2c Synoptic Display Viewer*: Interactive synoptic live display to visualize and control accelerator or beam line equipment,
- (2) *Web2c Archive Viewer*: Web form to request data from a control system archive storage and to display the retrieved data as a chart or table,
- (3) *Web2c Messenger*: Interface to E-Mail, SMS and Twitter,
- (4) *Web2c Logbook*: electronic logbook with auto-reporting capability,
- (5) *Web2c Manager*: administrator's interface to configure and manage the toolkit,
- (6) *Web2c Editor*: graphical editor to generate and configure synoptic displays, and
- (7) *Web2c Gateway*: application programmer interface (HTTP-gateway) to all implemented control system interfaces.

Web2cToolkit is a framework for Web-based Rich Client Control System Applications. It provides a user-friendly look-and-feel and its usage does not require any specific programming skills. By design, the Web2cToolkit is platform independent. Its services are accessible through the HTTP protocol from every valid network address if not otherwise restricted. A secure single-sign-on user authentication and authorization procedure with encrypted password transmission is provided. Registered and so-called privileged users have

more rights compared to ordinary users (read-only permission).

The Web 2.0 paradigms and technologies used include a Web server, a Web browser, HTML (HyperText Markup Language), CSS (Cascading Style Sheets) and AJAX (Asynchronous JavaScript And XML). The interactive graphical user interface pages are running in the client's Web browser. The interface is compatible with all major browser implementations including mobile versions. The Web2cToolkit services are provided by Java servlets running in the Web server's Java container. The communication between client and server is asynchronous. All third-party libraries used by the Web2cToolkit are open-source.

The Web2cToolkit provides interfaces to major accelerator and beam line control systems including TINE [3], DOOCS [4], EPICS [5] and TANGO [6]. The toolkit is capable of receiving and processing JPEG-type video streams.

CONCEPTUAL DESIGN OF Web2cToGo

Web2cToGo is a novel Web2cToolkit service especially designed for mobile devices such as tablet computers or smartphones running iOS, Android or other mobile operation systems. Web2cToGo is a frame which embeds instances of all kinds of Web2cToolkit services.

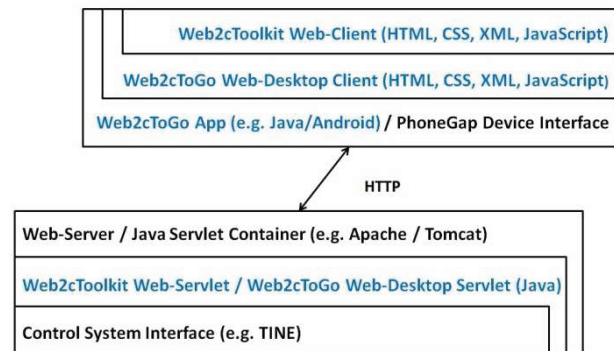


Figure 1: Web2cToGo client-server architecture.

Web-Desktop

The Web2cToGo service consists of the Web2cToGo mobile app and the corresponding Web2cToGo servlet (Fig. 1). By design an app is a platform-dependent application. However, the Web2cToGo app consists only of a few lines of native code creating a component capable of parsing and executing platform-independent HTML- / CSS-tags and JavaScript code snippets implementing the Web2cToGo Web-Desktop Client.

EPICS CHANNEL ACCESS USING WEBSOCKET

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Abstract

Web technology is useful as a means of widely disseminating accelerator and beam status information. For this purpose, WebOPI was implemented by SNS as a web-based system using Ajax (asynchronous JavaScript and XML) with EPICS [1]. On the other hand, it is often necessary to control the accelerator from different locations as well as the central control room during beam operation and maintenance. However, it is not realistic to replace the GUI-based operator interface (OPI) with a Web-based system using Ajax technology because of interactive performance issue. Therefore, as a next-generation OPI over the web using EPICS Channel Access (CA), we developed a client system based on WebSocket, which is a new protocol provided by the Internet Engineering Task Force (IETF) for Web-based systems. WebSocket is a web technology that provides bi-directional, full-duplex communication channels over a single TCP connection. [2] By utilizing Node.js and the WebSocket access library called Socket.IO, a WebSocket server was implemented. Node.js is a server-side JavaScript language built on the Google V8 JavaScript Engine. [3] In order to construct the WebSocket server as an EPICS CA client, an add-on for Node.js was developed in C/C++ using the EPICS CA library, which is included in the EPICS base. As a result, for accelerator operation, Web-based client systems became available not only in the central control room but also with various types of equipment.

INTRODUCTION

One of the advantages of an EPICS-based system is the unified communication protocol between the front-end controller and client systems provided by the CA (Channel Access) protocol. Thus, even when various types of controllers were used as control systems, all the client systems such as the OPI (operator interface) could be developed on the basis of the CA protocol without hardware dependencies. In general, a method that used the CA libraries or display manager supported by EPICS collaboration, such as CAJ/JCA, CA-Python, MEDM/EDM, and CSS (Control System Studio) [4], was adopted for the development of the GUI in the EPICS-based system. On the other hand, the engineers at SPring-8 proposed the development methods for the main OPI using WebSocket and conducted a prototype implementation [5]. The prototype system was constructed using a MADOCA (message and database oriented control architecture)-based system that was

developed at SPring-8. It was different from the EPICS-based system. Since the web application with real-time have many advantages, we started to develop WebSocket server corresponding to EPICS CA, and implemented Web applications using WebSocket for the EPICS-based control system. The traditional Web application lacked the interactivity needed to operate some of the hardware for the accelerator control system. By utilizing WebSocket technology, it is possible to solve the problems of Web-based OPI, such as the interactive response.

WEBSOCKET PROTOCOL

WebSocket is a new protocol for achieving the bidirectional communication between a Web server and Web browser. In the beginning, WebSocket was part of HTML5. It was formulated as an RFC6455 by IETF in Dec. 2011. An overview of the protocol is as follows.

1. A Web browser sends a handshake request to the server for connecting to the WebSocket.
2. The server returns the handshake response after approval.
3. After the establishment of the handshake, the protocol switches to the WebSocket, and then the bi-directional communication occurs between the Web server and Web browser.

WebSocket makes interactive response realizable and thus compensates for the disadvantage that could not be eliminated in traditional HTML. Thus far, various types of Web services in EPICS-based systems have been implemented. However, there were only implemented in Web-based systems, where a quick response and monitoring are unnecessary such as in archive viewers and electric-log systems. This is because it is difficult for a Web-based OPI to realize a real-time response similar to native applications such as EDM/MEDM/CSS, even if Ajax technology is utilized. Since it becomes bi-directional transmission between a server and clients has become possible, the aforementioned problem is solved by WebSocket. In practice, we confirmed sufficient interactive response in a 100 ms cycle using WebSocket on the Web browser, and it had a performance similar to that of native EPICS applications such as EDM. Furthermore, since periodic polling is not necessary like Ajax, it becomes possible to reduce network traffic. WebSocket does have a problem with Internet Explorer 9 (IE9), which is one of the main browsers, because a WebSocket connection is unavailable. However, this problem may be resolved in IE10, which is the next

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Qt BASED GUI SYSTEM FOR EPICS CONTROL SYSTEMS*

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Abstract

The Qt-based GUI system developed at the Australian Synchrotron for use on EPICS control systems has recently been enhanced to including support for imaging, plotting, user login, logging and configuration recipes. Plans are also being made to broaden its appeal within the wider EPICS community by expanding the range of development options and adding support for EPICS V4. Current features include graphical and non-graphical application development as well as simple “code-free” GUI design. Additional features will allow developers to let the GUI system handle its own data using Qt-based EPICS-aware classes or, as an alternative, use other control systems data such as PSI’s CAFE.

INTRODUCTION

The Qt-based GUI system, known as QE framework or simply QE, is a layered framework based on C++ and Qt for accessing EPICS data using Channel Access (CA). It is used on several beamlines at the Australian Synchrotron. Channel Access is one of the core components of an EPICS system allowing a CA client application to access control system data which may be located on different hosts throughout a network [1]. While CA is the default means to access EPICS data, its use is not trivial. A significant understanding on how this component works is required to read or write data. The complexity of setting up and terminating CA requests leaves room for error. The QE framework handles much of this complexity including initiating and managing a channel. Applications using QE can interact with Channel Access using Qt-based classes and data types. CA updates are delivered using Qt signals and slots mechanism. It provides access to EPICS data at several levels including programmatic reading and writing of data, EPICS-aware widgets such as push buttons, sliders and text widgets for developing GUI applications [2]. When these plugins are used within Qt Designer, GUIs interacting with EPICS can quickly be assembled without the need for any code development by meaning of simple drag & drop operations.

FRAMEWORK OVERVIEW

The QE framework allows access to Channel Access graphically through Qt-based widgets or through Qt friendly data objects. The data objects manage Channel Access connections and provide a simple, comprehensive, object oriented view of the CA data and related attributes. The QE graphical widgets and supporting QE data objects

form a hierarchy of classes that is open at all levels to the developer. Appropriate use of these classes is shown in Table 1. Also, the framework includes an application, QEGui, which is available to present control centric Qt user interface files.

Table 1: QE framework classes and their functionality.

Classes	Functionality
Data objects:	Provides a convenient object oriented way to access the CA library. Hides CA specific complexity and provides read/write conversions to and from EPICS data types where required. Adds Qt features such as signals and slots to handle data updates. These classes are used programmatically.
QEObject	
QEInteger	
QEString	
QEFloating	
Standard widgets:	Graphical objects that allow users to interact with CA data using simple and familiar graphical controls. These classes may be used programmatically or within Qt Designer.
QEComboBox	
QEForm	
QEFrame	
QEGroupBox	
QELabel	
QELineEdit	
QEPushButton	
QERadioButton	
QESlider	
QESpinBox	
Extended widgets:	Graphical objects that allow users to view CA data through a broad range of display models and support sophisticated control system user interface design. These classes may be used programmatically or within Qt Designer.
QEAnalogProgressBar	
QEBitStatus	
QEConfiguredLayout	
QEFileBrowser	
QEImage	
QELink	
QELog	
QELogin	
QEPeriodic	
QEPlot	
QEPvProperties	
QERecipe	
QEScript	
QEShape	
QEStripChart	
QESubstitutedLabel	

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DATA LOGGING SYSTEM UPGRADE FOR INDUS ACCELERATOR

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Abstract

An accelerator has various subsystems like Magnet Power Supply, Beam Diagnostics and Vacuum etc. which are required to work in a stable manner to ensure required machine performance. Logging of system parameters at a faster rate plays a crucial role in analysing and understanding machine behaviour. Logging all the machine parameters consistently at the rate of typically more than 1 Hz has been the aim of a recent data logging system upgrade.

Nearly ten thousand parameters are being logged at varying intervals of one second to one minute in Indus accelerator complex. The present logging scheme is augmented to log all these parameters at a rate equal to or more than 1 Hz. The database schema is designed according to the data type of the parameter. The data is distributed into historical table and intermediate table which comprises of recent data. Machine control applications read the parameter values from the control system and store them into the text files of finite time duration for each sub-system. The logging application of each sub-system passes these text files to database for bulk insertion. The detail design of database, logging scheme and its architecture is presented in the paper.

INTRODUCTION

Indus-1 and Indus-2 Synchrotron Radiation Sources (SRS) housed in Indus complex are cyclic particle accelerators that accelerate electrons up to 450 MeV and 2.5 GeV respectively [1]. These are supported by Microtron injector, Booster Synchrotron and various transport lines. In a multi accelerator complex like this, involving various complex subsystems, an effective system for comprehensive parameter data logging is considered essential.

Ideally, data logging system should contain all the information necessary to provide an accurate representation of the state of system parameters at any given time. The existing data logging system acquires and stores all the subsystem parameters at varying time interval of one second to one minute. Although this strategy has worked satisfactorily but this data logging scheme does not scale well as the number of control parameters grow and it begins to strain network and storage capabilities. This becomes a bottleneck in efficient operational diagnosis of all sub-systems in Indus accelerator. So an up gradation is aimed to design a data logging scheme that can provide a platform to log all the machine parameters at the same rate at which all the parameters are acquired from the field i.e. at 1Hz.

Hence, a new data logging approach of gathering the time series data in text files in the form of strings with delimiters along with the timestamp is adopted [2]. Besides this some major modification at software level has been introduced to achieve fast data logging of all the parameters at 1 Hz.

HARDWARE AND SOFTWARE ARCHITECTURE

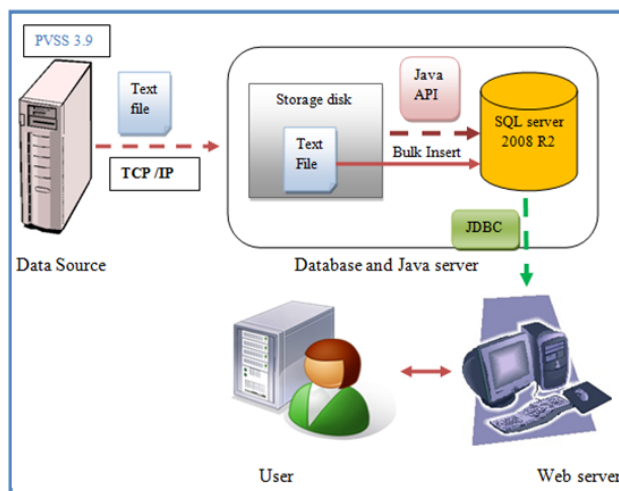


Figure 1: High level layout of data logging architecture.

The data collection process of Indus SRS machine is based on three tier architecture. The top layer architecture is shown in Figure 1. In the Indus control systems, middleware collects and processes the data from the field devices and sends it to the Indus control server based on the PVSS [3] industrial SCADA system. The PVSS control server continuously puts the data into text files with the timestamp for time span of five minutes and copies the text files (data files) to Java application server over TCP/IP. This process is repeated with time for each subsystem. It also deletes the previous text files only on receiving the successful acknowledgement of copy operation from Java server. Hence the control application running on PVSS control server also prevents the data loss in critical situations of logging failure by retaining the data in text files.

For each sub-system of Indus-2, Java application interface exists between PVSS control server and database server. The Java application periodically checks for recently received data file from the PVSS server and pass on the data file name to database server through a stored procedure call. These stored procedures after receiving the data file information, perform the bulk insert operation into corresponding subsystem database.

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CONTROL SYSTEM STUDIO ARCHIVER WITH PostgreSQL BACK-END: OPTIMIZING PERFORMANCE AND RELIABILITY FOR A PRODUCTION ENVIRONMENT*

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Abstract

Archiving systems based on relational databases provide a higher flexibility with regard to data retrieval and analysis than the traditional EPICS Channel Archiver. On the other hand they can suffer from poor performance compared to the Channel Archiver for simple linear data retrieval operations. However, careful tuning of the database management system's configuration can lead to major performance improvements. Special care must be taken to ensure data integrity following power outages or hardware failures.

This contribution describes the hardware and software configuration of an archiving system used in the production environment at the S-DALINAC. It covers performance and reliability aspects of the hardware as well as tuning of the Linux operating system and the PostgreSQL server.

INTRODUCTION

Archiving systems that collect and store data from an accelerator control system play an important role in modern control system environments. They can e.g. help to identify broken hardware, decreasing performance of components or wrong operation of systems by an operator. Thus archiving systems with high availability are demanded. Since wrong or inconsistent data from an archiving system can lead to wrong decisions by the operators it is also important to ensure data integrity. On the other hand data from the archive should be (read-only) accessible from many different applications ranging from simple spreadsheet applications to mathematical software for sophisticated data analysis. These requirements make relational databases (RDBs) a reasonable choice as a storage back-end.

The archiving system of the S-DALINAC is based on the Control System Studio (CSS) Archive Engine. This service collects data from control system channels and writes it to different RDB back-ends (MySQL, Oracle or PostgreSQL). PostgreSQL 9.1 running on Debian Linux has been chosen as a back-end because it is a powerful open-source RDB solution that comes without license fees.

Archiving systems usually have to manage a growing amount of data making read and write performance an important issue. In the following we describe how to tune an archiving system for maximum performance while ensuring data integrity.

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DISK PERFORMANCE AND RELIABILITY

Disk access is the most important factor for the performance of a database system that deals with much more data than can be stored in main memory. While modern disk drives can deliver data rates of more than 100 MB/s for sequential reads and writes they can be very slow when they have to deal with random access patterns. Heavy random access workload can occur if data is read from an archive by multiple clients using indexes. Thus database disks have to be optimized for high random access performance.

Write Caching

To improve access time all recent hard disk drives use integrated write-back caches and techniques to speed up disk access by optimizing the order in which read and write commands are executed to reduce the amount of drive-head movement. To insure data integrity database management systems (DBMS) flush operating system write caches after each database commit to make sure all relevant data has been stored on disk before marking the transaction as complete. Write-back caches on the disk drive itself are not flushed and thereby can lead to data loss and corruption of the database files in case of a loss of power. To avoid this, disk write caches have to be disabled for a database server.

Unfortunately switching off this cache severely reduces write performance. Part of this performance loss can be regained by using an appropriate operating system I/O scheduler that sorts the commands before sending them to the disk. But frequent flushing limits the possibilities for optimizations. A solution that provides better performance is using a hardware RAID controller with a battery backup unit. These controllers contain a non-volatile write-back cache that is powered by a battery in case of power outages. Data still in this cache when a loss of power occurs is written to disk after power resumes. Note that disk write caches often have to be disabled explicitly using the configuration tool of the RAID controller.

In contrast to hard disks, solid-state drives provide very high random access performance, but usually their write-back cache is volatile and cannot be disabled making them a bad choice if data integrity is a concern. Write caching is also an issue if a DBMS runs in a virtual machine because reliably flushing data to disk is impossible with most of today's virtualization products. Thus a physical machine is required for the RDB back-end of an archiving system.

FAST DATA ACQUISITION SYSTEM FOR BOOSTER SUPPLIES READBACK

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Abstract

Booster synchrotron at RRCAT is used to inject electron beam in Synchrotron Radiation Sources - Indus-1 & Indus-2. Booster gets 20 MeV beam from Microtron, ramps up its energy to 450/550 MeV which is then extracted for injection in Indus-1/Indus-2. The Ramping cycle repeats every second. For this, various magnet power supplies are fed reference voltage & current waveforms synchronously and accordingly they feed the magnets with current for ~800 msec. A system was required to synchronously capture data of all power supplies to on cycle to cycle basis. Global machine data monitoring system polling data at 1 Hz cannot acquire sufficient points to do this. So a VME and PC based system has been developed for parallel and fast capture of data from 13 such power supplies.

INTRODUCTION

There are 13 power supplies in the booster which participate in the ramping process to increase electron beam energy from 20 MeV to 450/550 MeV. Successful operation of booster depends upon the synchronous, reliable and reproducible performance of these power supplies. The development of fast, synchronous data acquisition system provides simultaneously captured waveform data sets for all the power supplies. This data provides quantitative measurement of power supply performance regarding the reproducibility of ramp waveforms and tracking between them. The hardware has been developed on VME platform consisting of CPU (68040), 12 bit ADC cards and control card. User can select- permit to capture, start delay, samples and time interval between samples. Advantages are - Isolated, simultaneous capturing on 13-channels, capturing synchronized with an event and selectable capturing-rate and samples. The CPU board on the VME runs RTOS OS-9 and control program on PC is developed using LabVIEW.

SCHEME OF THE DATA ACQUISITION SYSTEM

The implemented scheme has two-tier architecture. The first layer has a PC and the second layer has a VME station. The two communicate over Ethernet using TCP/IP sockets. A control program in LabVIEW® runs on the PC. The VME-station has a CPU board, 13 ADC boards and a Control board as shown in Figure 1.

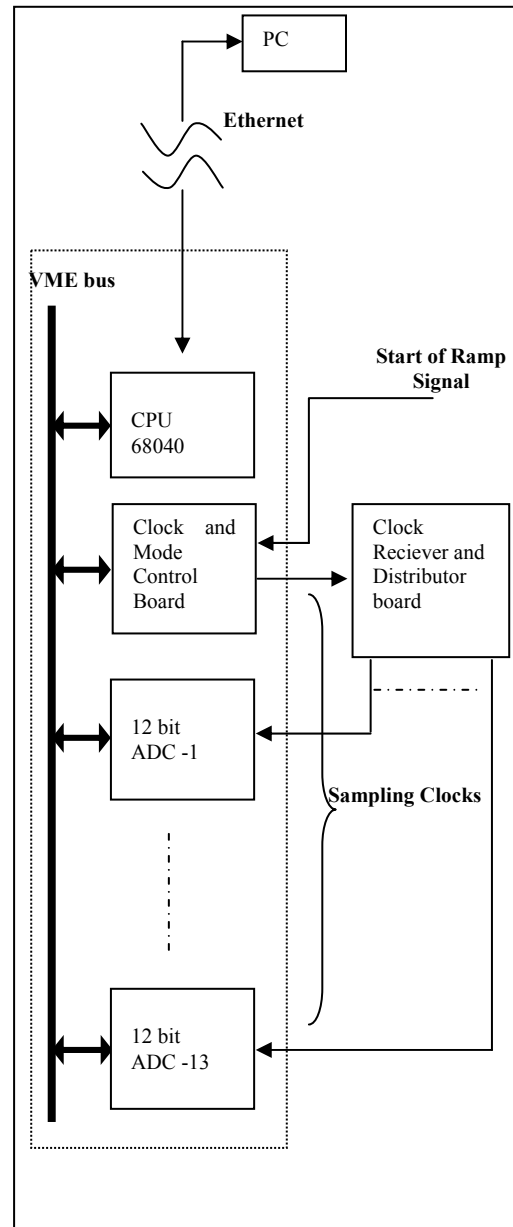


Figure 1: Scheme of Data Acquisition System.

The ADC board has a 12-bit sampling ADC with conversion rate of 100 KSPS and analog input range of 0-10 V. There is also a FIFO memory of size 8 K words on each ADC board. The board converts the input analog signal and stores the digitized data in this memory in response to an external trigger. The data that is captured in FIFO is read by the CPU.

There is a Clock and Mode 'Control Board' in the VME station. The CPU writes/ reads on this board to set the

EMBEDDED CAMAC CONTROLLER: HARDWARE/SOFTWARE CO-OPTIMIZATION FOR HIGH THROUGHPUT

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Abstract

Advances in technology have resulted in availability of low-power, low form-factor embedded PC based modules. The Embedded CAMAC Controller (ECC) is designed with ETX (Embedded Technology eXtended) standard Single Board Computer (SBC) having PC architecture with Ethernet connectivity. The paper highlights the software and hardware design optimizations to meet high throughput requirements of multi-parameter experiments and scan mode accelerator control applications. The QNX based software is designed for high throughput by adopting design strategies like multi-threaded architecture, interrupt-driven data transfer, buffer pool for burst data, zero memory copy, lockless primitives and batched event data transfer to host. The data buffer and all control logic for CAMAC cycle sequencing for LIST mode is implemented entirely in hardware in Field Programmable Gate Array (FPGA). Through this design, sustained throughput of 1.5MBps has been achieved. Also, the host connectivity through Ethernet link enables support for multi-crate configuration, thus providing scalability. The ECC has been installed for accelerator control at FOTIA BARC, Pelletron and LINAC-Pelletron, TIFR and for multi-parameter experiments at NPD, BARC.

INTRODUCTION

PC compatible architectures have become a popular choice for embedded systems because of easy availability of low powered, low form-factor embedded PC based modules. Also, a large base of knowledge and resources exist for these architectures. An Embedded PC meets special needs of mechanical design, power consumption, product lifetime, customized software and professional support. All these readily available features of Embedded PC-based technology coupled with optimum hardware and software design allowed to develop an Embedded CAMAC Controller (ECC) for high throughput requirements of multi-parameter experiments. The paper discusses various design optimizations in the hardware and software of ECC.

EMBEDDED CAMAC CONTROLLER

Embedded CAMAC Controller [1] has been designed to cater to the needs of process control systems and high throughput of large nuclear physics experiments. Control applications need more number of physically distributed crates with regular scanning of all the parameters, the

control being with a centralized computer, whereas nuclear physics experiments need a high throughput with a large number of parameters in one or more crates.

The Single Board Computer (SBC) of ECC interfaces with PCI-CAMAC Interface logic through PCI controller (see Fig. 1). The ECC allows interaction with remote host by means of standard Ethernet services, such as TCP socket based communication protocol. The processor runs a version of QNX optimized for low memory footprint. The FPGA holds List buffer, Data buffer and all control logic for CAMAC cycle sequencing. Three modes of operation have been supported:

- **Single Cycle mode:** In this mode, single ECC command is executed in every cycle.
- **Scan mode:** In scan mode of operation, a list of CAMAC commands is sent to the ECC and is executed at regular intervals, and is suitable for control applications.
- **List mode:** The list mode is optimized for multi-parameter experiments. In this mode a list of CAMAC commands is stored in Field Programmable Gate Array (FPGA) which is executed on every Look At Me (LAM) from signal acquisition module.

SALIENT FEATURES: HARDWARE

- List sequencing mode with 1.1 μ s CAMAC cycle for multi-parameter experiments
- Scan mode with a period of 50msecs for control applications
- Trigger source: LAM / External event / Timer
- Ethernet connectivity for remote and multi-crate configurations.
- Built-in test features with CAMAC data way display

List Mode Optimization

ECC operates in List mode for multi-parameter experiments. There are three lists of NAF commands in multi-parameter mode of acquisition; EVENT_LIST, INI_LIST and SCALER_LIST. The INI_LIST is executed once at start of acquisition to initialize the ECC. EVENT_LIST of up to 256 CAMAC commands is executed upon generation of LAM and data is stored in FIFO buffer. In List mode processing, once the setup is complete and acquisition is started, the host does not intervene other than to stop the acquisition. In this mode, all acquired event data are stored in communication

CLIENT SERVER ARCHITECTURE BASED EMBEDDED DATA ACQUISITION SYSTEM ON PC104

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Abstract

The data acquisition system is designed on embedded PC104 platform Single Board Computer (SBC) with running Windows XP Embedded operating system. This is a multi channel system which consists of 12 Bit, 10 MSPS Analog to Digital Converters with on board FIFO memory for each channel. The digital control and PC104 bus interface logic are implemented using Very High Speed Hardware Description Language (VHDL) on Complex Programmable Logic Device (CPLD). The system has provision of software, manual as well as isolated remote trigger option. The Client Server based application is developed using National Instrument CVI for remote continuous and single shot data acquisition for basic plasma physics experiments. The software application has features of remote settings of sampling rate, selection of operation mode, data analysis using plot and zoom features. The embedded hardware platform can be configured to be used in different way according to the physics experiment requirement by different top level software architecture. The system is tested for different physics experiments. The detailed hardware and software design, development and testing results are discussed in the paper.

INTRODUCTION

The main objective to develop this system is to provide PC based simple and easy solution for low channel data acquisition requirement to support the basic physics experiments carried out by the students. These experiments often require few channels with high sampling rate with short acquisition time. To avoid using high end resources for data acquisition application for small experiments, the system is developed which requires very minimum resources and knowledge to operate it. The Client Server architecture based embedded data acquisition system is developed on PC104 [1][2] platform which houses inside standard industrial 6U, 16T enclosure which requires minimum space to install and operate. As far as resources concerned, It requires only Ethernet local area network connectivity for full fledged operation. The basic data acquisition hardware consists of 5 channels with simultaneous sampling pipelined ADCs, which are capable of doing sampling from 1KHz to 10MHz. Each channel consists of 64K location of FIFO memory. The hardware design is very flexible and all data acquisition parameters are software controlled. The system can be operated in manual as well as external trigger mode and it also accepts external clock. The basic system level operational block diagram is shown in Figure 1.

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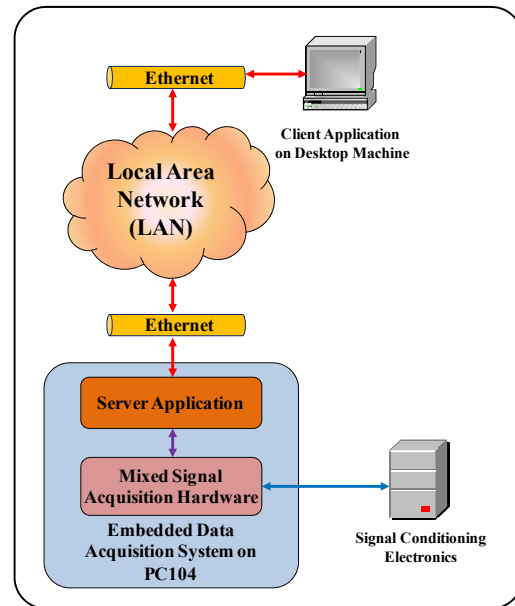


Figure 1: Basic system block diagram.

HARDWARE

This embedded board is designed and assembled in-house and it contains PC104 based Single Board Computer which is procured commercially. The designed and developed board contains analog, digital and mixed signal components. The board is designed and fabricated on four layered PCB. The hardware level block diagram and the selected components are shown in Figure 2.

- Analog front end is designed with AD524 [3] high bandwidth Instrumentation Amplifier followed by AD8041 high speed ADC driver which translates the signal level to dynamic signal range of pipelined ADC AD9220.
- Each channel contains dedicated FIFO memory of size 64K which has total three memory status flags i.e. half, full and empty which can be used for status monitoring and control purpose.
- All digital operational logic like hardware initialization, clock control, ADC and memory control, PC104 bus signal decoding are implemented in Xilinx Complex Programmable Logic Device (CPLD), which is written in VHDL.
- The acquisition module supports internal as well as isolated external clock and trigger.
- The system contains Advantech make PCM-3353F [4] Single Board Computer which runs on Windows XP Embedded Operating System installed on 4GB size of compact flash card.

A LARGE CHANNEL COUNT MULTI CLIENT DATA ACQUISITION SYSTEM FOR SUPERCONDUCTING MAGNET SYSTEM OF SST-1

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Abstract

The magnet system of the Steady-state Superconducting Tokamak-1 at the Institute for Plasma Research, Gandhinagar, India, consists of sixteen Toroidal field and nine Poloidal field Superconducting coils together with a pair of resistive PF coils, an air core ohmic transformer and a pair of vertical field coils. These coils are instrumented with various cryogenic grade sensors and voltage taps to monitor its operating status and health during different operational scenarios. A VME based data acquisition system with remote system architecture is implemented for data acquisition and control of the complete magnet operation. Client-Server based architecture is implemented with remote hardware configuration and continuous online/ offline monitoring. A JAVA based platform independent client application is developed for data analysis and data plotting. The server has multiple data pipeline architecture to send data to storage database, online plotting application, Numerical display screen, and run time calculation. This paper describes software architecture, design and implementation of the data acquisition system.

INTRODUCTION

The Steady-state Superconducting Tokamak (SST-1) is a medium size fusion device to study the plasma behaviour in steady state operation of 1000s [1]. SST-1 magnet system consists of sixteen Toroidal field (TF) and nine Poloidal field (PF) Superconducting coils, together with a pair of resistive PF coils, an air core ohmic transformer and a pair of vertical field coils [2]. These magnets need to be monitored during all operational scenarios like cool down, ramp up, flat top, plasma breakdown, dumping/ramp down and warm up. More than 500 sensors, like temperature sensors, voltage taps, venturi flow meters, hall probes, pressure sensors, and displacement transducers are mounted on the magnet system and its auxiliaries. These sensors produce very low level signals and so they impose very strict requirements on the signal conditioning and acquisition electronics [3]. Magnet Data Acquisition System (DAS) is required to amplify and filter the signal, digitize the signal, acquire and store it, display the data in engineering units and communicate with other subsystems, all in real time. To satisfy all these requirements, a complete VME bus-based real time data acquisition system is designed and implemented for SST-1 magnet system. The hardware consists of 64 bit backplane VME chassis, SBS-

VG4 crate controller with PowerPC-755 processor from SBS technologies, Analog input module IP330 and Analog output module IP 220 from ACROMAG, 6U AVME 9660 carrier board with four daughter card slots from ACROMAG, Digital I/O module VMIVME-2528 from VMIC and a GPS timing module BC635VME from Symmetricom Inc.

PROJECT SCOPE

The VME based DAS is suppose to monitor different sensors mounted on the SST-1 magnets and its auxiliaries, continuously and reliably during different phases of SST-1 magnet operation. The total numbers of required channels are more than 500 in numbers which are required to be monitored continuously over long duration during an experimental campaign. Table 1 shows typical distribution of data acquisition channels for magnet systems with different sensors and its primary application. Sensor signals are coming from the different signal conditioning cards mounted in the instrumentation racks in the magnet control room [4] and are interfaced with VME IOs through signal connection box. Figure 1 shows the functional block diagram of VME DAS with its associated hardware subsystems.

Table 1: Channel distribution for Data Acquisition system

No.	Sensor	Channels	Application
1	Temperature Sensors	150	Cryogenic Temperature Measurement
2	Voltage-tap channels	224	Quench detection and magnet voltages
3	Hall probes	16	Magnetic field direction and intensity measurements
4	Flow meters (Venturi)	32	Flow measurements
5	Absolute Pressure	16	Helium Pressure measurement
6	Displacement transducers	12	Displacement measurement in cold mass
7	Strain gages	8	Stress measurement on magnets
8	Joint Resistance Measurement	102	Inter-pancake and Inter-coil joint resistance measurement

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SERIAL MULTIPLEXED BASED DATA ACQUISITION AND CONTROL SYSTEM

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Abstract

Data acquisition and control system consists of analog to digital converter (ADC), digital to analog converter (DAC), timer, counter, pulse generator, digital input / output (DIO) depending upon requirement. All the system components must communicate with personal computer (PC) for data and control signal transmission via one of the communication protocol like Serial, Parallel, USB, GPIB. Serial communication is advantageous over other protocol due to several reasons, like long distance data transmission, less number of physical connection, ease of implementation etc. The developed Serial Multiplexed based Data Acquisition and Control System, which can control different modules like ADC, DAC, DIO, Timer card using single serial port. A LabVIEW based program is developed for the individual communication of each module.

INTRODUCTION

The basic data acquisition and control system consists of different types of application module like ADC, DAC, timer, counter, pulse generator, DIO etc. The module is selected depending upon the requirement. The modules are individually controlled with personal computer (PC) for data and control signal transmission using one of the communication protocol. If communication is done using different protocol for different modules in system requires knowledge of different communication protocols, communication hardware and large number of connection with the PC.

In order to overcome the above mentioned difficulties, we developed Serial Multiplexed based Data Acquisition and Control System (SMDACS). In house developed system consists of different application modules and a controller module. The application modules are controlled by controller module having serial connectivity. The control program for each application module is developed in Lab-VIEW environment.

FUNCTIONAL DESCRIPTION

A block diagram of SMDACS is shown in Fig. 1. The system consists of different application modules which are installed on back panel (mother board) of the system. The physical address for the application module is set on mother board from 000 to 111. When system is switched ON, the application module read the physical address and saves in local register of microcontroller. While transferring command for Read / Write, the logical address is sent first. The microcontroller in application module compares logical address and physical address.

The module program command sequence is executed in the application module whose logical address and physical address matches. All the commands are treated as either read or write considering as receive or send by PC. Data and commands are sending or receive by the PC to the application module via serial interface. The application module can be installed in one to eight locations while controller is placed on ninth position. The application module has no physical position limitation, i.e., any module can be installed in any position except the controller module.

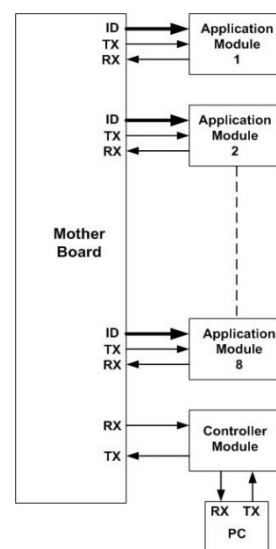


Figure 1: Block diagram of developed SMDACS.

Figure 2 shows the developed SMDACS assembly. The assembly consists of 3U size, nine slot chassis. The chassis as controller module, application module, back panel and in-built power supply. The right-most module is the controller module. Each application module communicates with the controller module using back panel 15 pin D-type for transmit, receive and power. Three pins of the 15-pin D-type connector are used for physical address of the module. The application module is used physical address for data and control information transmission. Each application module consists of logic gates, microcontroller (AT89C52) and other related components.

Controller Module

Controller module is the heart of the system. It is the interface module which transmits data and control signals between PC and application module. Front panel of the module has power indicator and a data transmission indicator. It has an external trigger which is used as bus

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VEPP-2000 LOGGING SYSTEM*

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Abstract

The electron-positron collider VEPP-2000 has been constructed in the Budker INP at the beginning of 2007 year. The first experiments on high-energy physics has been started at the end of 2009. The collider state is characterized by many parameters which have to be tracked. These parameters called channels could be divided into continuous (like beam current or beam energy) and pulsed. The main difference is that the first one related to the moment of time while the second one to the beam transport event. There are approximately 3000 continuous channels and about 500 pulsed channels at the VEPP-2000 facility. The Logging system consists of server layer and client layer. Server side are a specialized server with an intermediate embedded database aimed at saving data in case of external database fault. Client layer provide data access via API, CLI and WUI. The system has been deployed and is used as primary logging system on VEPP2000.

VEPP-2000 PROJECT

VEPP-2000 is a new collider with luminosity up to $10^{32} \text{cm}^{-2} \text{s}^{-1}$ and the beam energy up to $2 \times 1 \text{ GeV}$ [1, 2].

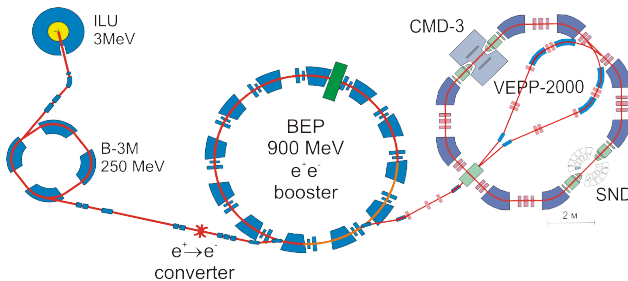


Figure 1: VEPP-2000 facility layout.

This project is a development of a previous facility of VEPP-2M which has worked at BINP over 25 years in energy range up to 1.4 GeV in c.m.s. and has collected of about 75 pb^{-1} integrated luminosity. New collider uses the existing beam production chain of accelerators: ILU – a pulsed RF cavity with a voltage of 2.5 – 3 MeV, a 250 MeV synchrotron B-3M and a booster storage ring BEP with the maximum project beam energy of 900 MeV (see Figure 1). The lattice of VEPP-2000 has a two-fold symmetry with two experimental straight sections of 3m length, where Cryogenic Magnetic Detector [3] and Spherical Neutral Detector [4] are located. Two other long straights (2.5m) are designed for injection of beams

and RF cavity, and 4 short technical straight sections accommodate triplets of quadrupole.

The closed orbit steering and gradient corrections are done with 1-2% coils placed in the dipole and quadrupole magnets.

Beam diagnostics is based on 16 optical CCD cameras that register the synchrotron light from either end of the bending magnets and give the full information about beam positions, intensities and profiles. In addition to optical BPMs, there are also 4 pick-up stations in the technical straight sections and one current transformer as an absolute current monitor.

The magnetic field of 2.4 T in the bends is required to reach the design energy of 1 GeV in the constrained area of the experimental hall.

CONTROL SYSTEM (SOFTWARE)

Modern accelerator facility is a complex system both physical and technical meaning. It consists of many subsystems and units, which are difficult to automatize.

Collider state is characterized by many parameters which have to be tracked. These parameters could be divided into two groups: continuous (like beam current or beam energy) with typical speed of change from two time at second up to one time at ten minutes and pulsed which are related to some event (e.g. beam transport event called “Shot”). There are approximately 3000 continuous channels and about 500 pulsed channels at VEPP-2000 facility.

Control system is multilayer distributed system with specialized hardware server at lower layer, client program at upper and utility server between them. It was build according to the concept of independent subsystem control. Such approach allows us to create a small program with strictly divided responsibility.

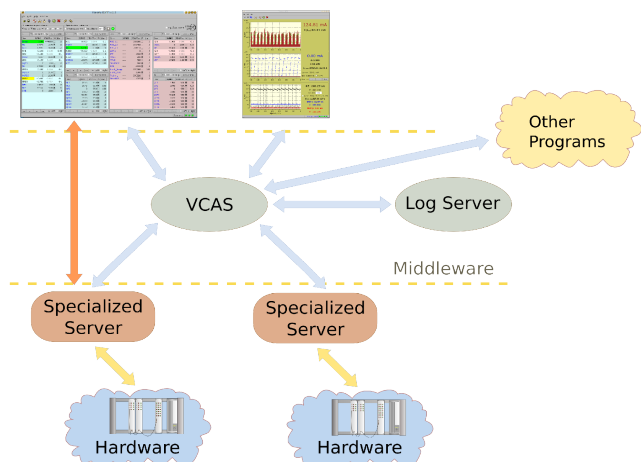


Figure 2: Control system schema.

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DEVELOPMENT OF DATA ACQUISITION SOFTWARE FOR VME BASED SYSTEM

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Abstract

A Data Acquisition system for VME has been developed for use in accelerator based experiments. The development was motivated by the growing demand for higher throughput in view of the increasing size of experiments. VME based data acquisition system provides a powerful alternative to CAMAC standards on account of higher readout speeds (100 ns/word) resulting in reduced dead time. Further, high density VME modules are capable of providing up to 640 channels in a single VME crate with 21 slots. The software system LAMPS, earlier developed for CAMAC based system and used extensively in our laboratory and elsewhere has been modified for the present VME based system. The system makes use of the VME library to implement Chain Block Transfer Readout (CBLT) and gives the option of both Polling and Interrupt mode to acquire data. Practical throughput of ~250 ns/word in zero suppressed mode has been achieved.

INTRODUCTION

With increase in size of Nuclear physics experiments, a secular trend toward higher throughput bus standards has been observed. VME [1] - an acronym for VERSA Module Euro card - provides a powerful alternative to the CAMAC standard on account of higher readout speed (100ns/word) leading to significant reduction in dead time. High channel density VME modules significantly bring down the expenses involved in acquisition of data per channel. Further, usage of optical fiber link makes sure that the interconnect technology doesn't become a bottleneck during data transfer. LAMPS [2] software, earlier developed for CAMAC based system, has been modified for VME based acquisition system. It currently supports CAEN [3] V785 ADC, V775 TDC and V862 QDC and V830 scalar modules. Practical throughput, using VME data acquisition system and LAMPS, of ~250ns/word in zero-suppressed mode has been achieved.

ARCHITECTURE

System Architecture

The VME data acquisition system (see Figure 1) consists of VME digitizer modules plugged into the VME backplane, controlled by master module. VME master module (V2718) is a VME to PCI (Peripheral Component Interconnect) Optical Link Bridge, housed in a 1-unit wide VME 6U (19" x 10.5" x 19.5") module. Master module is controlled using a computer equipped with PCI optical controller card (A2818), capable of transferring data at 80 Mbytes/second. The connection between the master module and controller card takes place through an optical fiber cable.

CAEN digitizer modules for VME provide features like zero suppressed readout and overflow suppression. Zero suppression, once enabled, prevents conversion of value which is lower than user defined threshold. Overflow suppression, once enabled, aborts the memorisation of data which constitutes an ADC overflow.

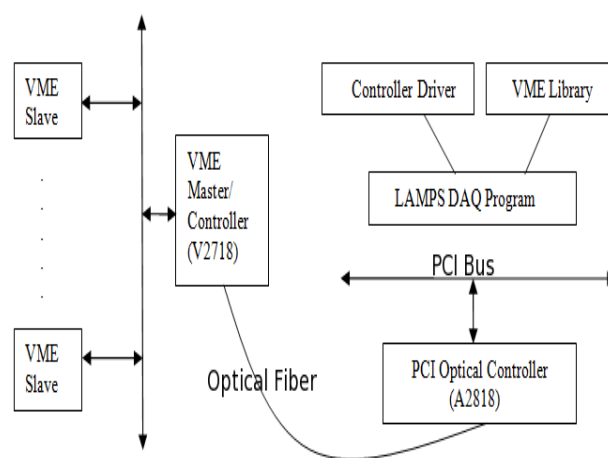


Figure 1: VME Data Acquisition system: System and Software Architecture.

The maximum VME address space is made of 2^{64} bytes for VME64 standard. Each slave occupies a portion of this space. Geographical addressing and address relocation methods for setting base address are absent in VME64. Thus, base address for slaves has been set at hardware level by means of rotary switches. Various registers of VME slave can be accessed, thereafter, by adding relevant offset to the module's base address.

LAMPS program

LAMPS is a data acquisition and analysis package that supports, apart from VME, a number of CAMAC controllers. It has been written in C and user interface has been implemented using GTK.

It allows for online spectra building (see Figure 2) and can also be used for offline data analysis. It provides, inter-alia, tools for performing calibration, peak fit, peak search, quick fit and obtaining the area and centroid of a spectrum region.

It runs under Linux and can also be made to execute on Microsoft Windows through Cygwin [4]. It is designed for large scale experiments and is in use at BARC-TIFR Pelletron laboratory, since August 2002.

MICROCONTROLLER BASED DAQ SYSTEM FOR IR THERMOGRAPHY BY HOT AND COLD WATER FLOW

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Abstract

There are many Non Destructive Techniques used in science and industry to evaluate the properties of a material, component or system without causing damage. Infrared Thermography (IR) is one of them. Different types of IR thermograph is used for different purpose. We are using hot and cold-water flow IR Thermography method to evaluate the Performance of Plasma Facing Components (PFC) for Divertor Mock-up [1].

The Set-up is designed in such a way that hot and cold water can flow in both direction inside mock-up, like left to right and right to left using electric pumps. Eight numbers of Solenoid Valves have been used for selection of Water Flow Direction, thermo-couples for temperature measurement of water, IR camera to take the images and many others devices. This needs a very good and versatile DAC system. We have developed a DAC system using micro controller and LabVIEW for the acquisition of various parameters and controlling & synchronization of other system. Development of DAC is described in this paper.

INTRODUCTION

The main aim of this IR thermography is to evaluate the quality of the braze joints between PFC tiles and the copper alloy (CuCrZr) heat sink. Figure 1 shows the schematic of PFC test mock-up and experimental arrangement for IR-NDT. PFC is placed in front of IR camera at a particular distance such that the FOV (Field of View) of IR camera can cover array of tiles. The IR camera captures thermal evolution at the tile surface and transfers the information to the computer for data storage device for further processing. We have developed an IR thermography to test the PFC components by Hot and cold water flow method. This paper described the DAQ for hot and cold water IR thermography by using micro-controller 8051 and Lab VIEW.

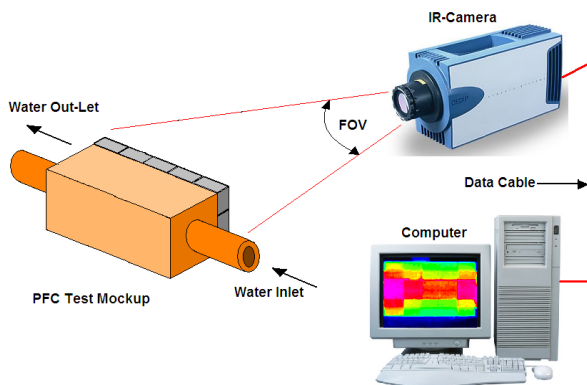


Figure 1: Schematic of IR-Thermography.

HOT & COLD WATER FLOW LOOP SETUP FOR IR-NDT OF PFCs

A schematic diagram of water flow loop facility to be developed for IR-NDT of PFCs is given in the figure-2. The setup is designed in such a way that hot as well as cold water can flow in both direction inside PFCs, like Left to Right and Right to Left.

Eight numbers of water valves have been used for selection of hot & cold water and also used to alter their flow directions. Flow rate is controlled by VFD. A digital water flow meter is located at the out-let of the water pump for measuring the flow rate of water passing through it. Two numbers of 1.5 kW electric water-heaters are used to heat the water in hot water reservoir. Four numbers of thermocouples are used to monitor the temperature of water at various locations. A water cooler is used to provide cold water. Table 1 shows the selection procedures for Hot & Cold water and their flow directions.

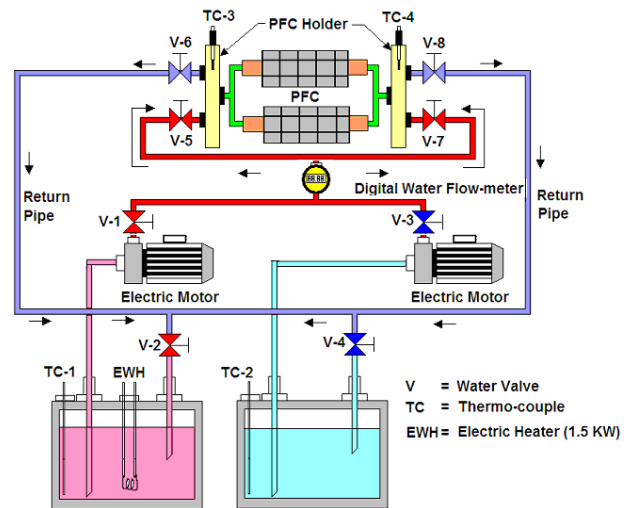


Figure 2: Hot and Cold water flow loop setup.

BLOCK DIAGRAM OF DAQ

Block diagram of micro controller based DAQ System is shown in Figure 3. We have used microprocessor 8051. Serial communication RS-232 is used between PC and micro controller. Solenoid driver circuit is used to operate the solenoid valves. Variable frequency driver is used to run the water pumps at different pressure require for IR thermo-graphy. A signal is given to VFD from micro controller to operate the water pump and same signal is also applied to IR camera to store the images. A flow chart is shown in Figure 4.

SMART STRUCTURED MEASUREMENT PROCESS FOR VERSATILE SYNCHROTRON BEAMLINE DATA AT ANKA

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Abstract

An unstructured measurement process might deliver the needed quantity of primary data for an experiment. But the achievement of the scientific results depends more and more from the offered opportunities of embedding these measurement data into its specific context with a metadata description and a complete life cycle management.

Obviously the design of a measurement process influences the potential applicability of an experimental setup for its scientific purpose and of course its options to fulfil a contemporary data management. ANKA's Tango based environment offers in principal varying approaches with different implementation efforts and coverage of scientific or information technology requirements.

At ANKA we have set up a smart structured measurement process which stand out due to its seamless integration into the overall data management, the support of recent control concepts for fast data generation as well as its support of well time-tested SPEC based scan systems. The presented measurement process focuses to the minimal implementation for all involved components without a break of well accepted habits.

INTRODUCTION

Currently at synchrotrons used control systems like EPICS, TACO, or TANGO [1] are focusing to the problem of retrieving and delivering digitized data from the measurement process at the experimental stations as well as at all peripheral equipment.

The growing amount of available digitized measurement data, which is organized by hand in a first straight forward approach, led to a situation which does not permit an automated data management. Solutions for crosslinking and archiving them are strongly demanded. Some effort is done - not only in the synchrotron community, e.g. LSDF[2] and HDRI[3] - to implement an extended data management to these scientific data.

The new at ANKA introduced smart concept offers the base for the implementation of the desired automated overall data management with minimised efforts.

The experimental beamline stations at ANKA were originally designed on the basis of SPEC [4] (see Fig 1, part A). In this context the SPEC output defines which meta- and measurement data will be saved in an ASCII-file. Measured data is collected from fast (~ms) directly by spec driven devices (green part in Fig. 1) or other slow speed-triggered-TANGO-devices (blue part in Fig. 1). As SPEC can be used as TANGO server and client at the

same time [5] it is used as a *user interface* as well as a *scan server* for X-ray beamline experiments.

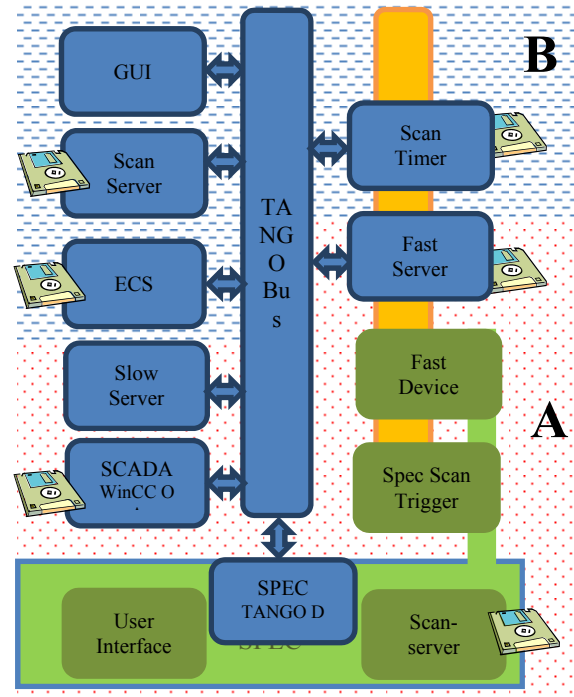


Figure 1: The logical beamline layout (The realised part A and the currently developed extension in part B).

Autonomous devices outside SPEC are partially synchronized and triggered by an electrical signal based trigger and gating system (yellow in Fig. 1). The disadvantage of this scenario is that each device is generating its own unmanaged data file separately. Also the WinCC OA [6] overall SCADA system collects asynchronously and independently peripheral data in parallel. WinCC OA was extended by TANGO server and client capabilities [7].

The resulting already three data sources (symbolised as disks in Fig. 1, part A), indicates a strong evidence that there is a reasonable demand for an *experiment coordination service* (ECS).

The role of such an ECS in the experiment workflow is in general not a new idea and was in our case already implicitly present by the coded scheme of SPEC. The sequential synchronous nature of that data acquisition approach so far was the major reason to separate it from spec and set up a special dedicated ECS device server.

The key for interlinking the retrieved information is the *metadata*. Therefore the objective will be achieved by a careful attention to the dedicated retrieval and processing

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POST-MORTEM ANALYSIS OF BPM-INTERLOCK TRIGGERED BEAM DUMPS AT PETRA-III

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Abstract

PETRA-III is a 3rd generation synchrotron light source dedicated to users at 14 beam lines with 30 instruments. This operates with several filling modes such as 60, 240 and 320 bunches with 100mA or 40 bunches with 80mA at a positron beam energy of 6 GeV. The horizontal beam emittance is 1nmrad while a coupling of 1% amounts to a vertical emittance of 10pmrad. During a user run unscheduled beam dumps triggered by Machine Protection System may occur. In many cases the reason can be identified but in some it remains undetected. Though the beam is lost some signature is left in the ring buffers of the 226 BPM electronics where last 16384 turns just before the dump are available for post-mortem analysis. Scrutinizing turn by turn orbits and the frequency spectrum measured at a BPM can improve understanding of such a beam loss and may help to increase the efficiency of operation by eliminating the sources. Here we discuss in detail the functionality of a Java GUI used to investigate the reasons for unwanted dumps. In particular, the most effective corrector method is applied to identify correctors that might have perturbed the golden orbit leading to violations of the interlock limits.

INTRODUCTION

PETRA-III [1] is a 3rd generation synchrotron light source commissioned with positron beam energy of 6 GeV and 100mA stored current at betatron tune values (36.12, 30.28). The horizontal beam emittance is 1nmrad while a coupling of 1% amounts to a vertical emittance of 10pmrad. The machine is dedicated to users for experiments from 14 beam lines with 30 instruments. This operates with several filling modes, such as 60, 240 and 320 bunches with 100mA or 40 bunches with 80mA. During the normal user operation, there are unscheduled beam dumps triggered by Machine Protection System (MPS) [2, 3]. These triggered dumps may be before or some times after the loss of beam. The loss of beam after the beam dump by MPS is understood as the reason as implied by the protection system. But the loss of beam before the beam dump by MPS or sudden fall of beam current and subsequently filled up by top up are unexpected. In these cases the reason is not identified or some cases it is undetected. But, though the beam is lost, it left some signature on its post-mortem data. From these data proper scrutinization of turn by turn orbits and the frequency spectrum measured at a BPM can improve understanding of such a beam loss and may help to increase the efficiency of operation by eliminating the

sources of disturbance. For these purposes, there are 226 Beam Position Monitors (BPM) distributed in 2303.952m ring to monitor the transverse orbits by Libera System[4]. These BPMs are connected with a Ring Buffer where continuously 16384 latest turns of data for each BPM is stored in Libera. When the Libera server receives a beam dump signal from MPS, it dumps 16384 turns of orbit data for each BPM to an Archive Server with an event time stamp for post-mortem analysis. It is worth to mention that the revolution frequency of PETRA III is 130.121 kHz. Though there are 226 BPMs, all are not activated to trigger a MPS signal. The BPMs in damping wiggler sections in West and North, the BPMs in DBA sections are activated with lower and upper limit of orbit deviations in transverse plane. If the orbit deviations are beyond these limits at any of such special BPM then Libera initiates an interlock event to MPS to fire a beam dump signal. As mentioned above the post-mortem data not only contains orbits but includes these interlock orbit bounds and the Σ -signal of beam intensity. These post-mortem data are huge and contains a lot of information which we want to extract and analyze in this paper using a Java Graphics User Interface (GUI) Web application.

The GUI is developed in Java. It requires JRE 6+ or Java Web Start 1.5+ to run with a memory of 1024MB. It uses FORTRAN subroutine MICADO[5] of CERN library of MADx program for its most effective orbit corrector [MEOC] method. The FORTRAN subroutine is called via a Java Native Interface (JNI) written in C. To run in every computer, where FORTRAN library routines are not available, this code temporarily copies FORTRAN runtime library files (.DLL) into TEMP directory of the user. The post-mortem data are downloaded iteratively from the Archive Server [6-8]. Due to heavy demand on this server, sometimes maybe bit difficult to retrieve data. If occasionally null data is retrieved then one has to read the event once again.

Here we describe the beam dump events for the tripping of corrector magnets, wrong setting of power supplies, failure in RF system temperature regulations, unclosed injection kicker bumps etc. The main features are looking into the frequency spectrum [9] of turn by turn orbits of a particular BPM; the MEOC method is applied to identify correctors that might have perturbed the golden orbit leading to violations of the interlock limits at an active BPM. Due to transient malfunction of a magnet, the orbit will grow and surpass the interlock limits at some special BPM and the beam will be dumped by MPS. In post-mortem analysis this change in orbit can be corrected by a few correctors using MICADO to investigate the cause of beam loss in transverse plane.

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DESIGN AND IMPLEMENTATION OF LABVIEW™ BASED GUI FOR REMOTE OPERATION AND CONTROL OF EXCIMER LASER FOR PLASMA WAKEFIELD ACCELERATION EXPERIMENT

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Abstract

The paper describes the development of a GUI based control software for control/operation, maintenance and data logging of a Coherent CompexPro 102 Excimer Laser (ArF, 193 nm) using LabView™ instrument control software.

INTRODUCTION

The Coherent COMPexPro102 Excimer laser (Fig.1) is an ArF gas based UV laser operating at a wavelength of 193 nm. This laser uses Ar, F₂, Ne, and He gases for its operation. The laser can deliver a maximum energy of ~ 200 mJ at 15 ns pulse width and capable of operating at a pulse repetition rate of 1-20 Hz. The laser is normally controlled using a tethered control panel which has a cable length restriction of around 3 meters. In order that the laser can be controlled and monitored remotely, it is essential that a GUI based interface be developed. The block-diagram of system showing the gas feed system, the I/O system and the energy meters is shown in Fig.2.

Currently, the operation of the laser is carried out manually using the wired keypad. The main motivation of the development of this GUI is for easier user convenience as well as for future use when the laser will be used to generate lithium photo-ionized plasma for the plasma wakefield accelerator experiment system. In the experiment, the laser operation will be carried out remotely and the laser system will be integrated with the accelerator system operations *via* LabView™ instrument

control software. The GUI of the laser will be integrated with the GUI's of other components of the experiment

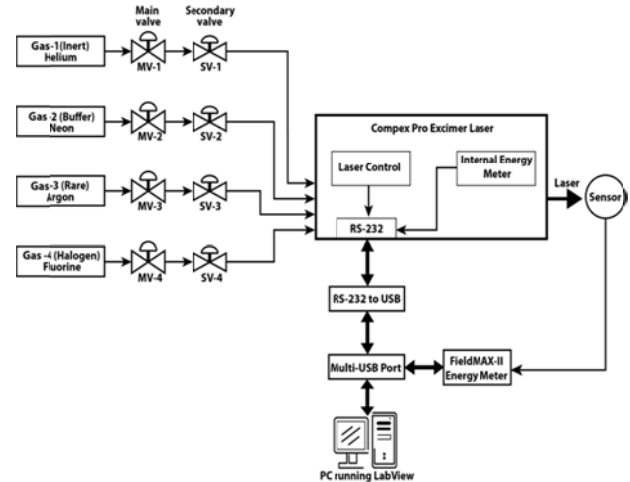


Figure 2: Schematic diagram of the excimer laser system showing the gas lines, I/O interfaces and energy calibration layout.

such as accelerator operation, precision heater controls for the plasma chamber, vacuum /gas fill systems as well as data acquisition equipment, thus providing a single window control of the whole experimental system. Routine laser operation (setting of parameters and running of laser), maintenance operations like gas fill and energy calibration, logging of laser parameters etc., which are currently being carried out manually will be automated using the GUI.

This paper presents the development of the module for the excimer laser, *i.e.*, the required LabVIEW™ virtual instrument modules, GUI interfaces and the required display screens for laser control, parameter display, gas fill operation as well as documentation/logging of the operational parameters of the laser system. The paper also presents the development of a completely automated module for calibration of the internal energy meter of the excimer laser with a calibrated external laser energy meter (Coherent FieldMax-II). This procedure is necessary as the performance and calibration of the internal energy meter which is used by the laser system to stabilize its laser output can vary over a period. This one-switch, automated operation provides a linear-fitted calibration of the internal energy meter with that of a pre-calibrated commercial energy meter. This procedure is



Figure 1: The Excimer laser system.

STARS ON ANDROID

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Abstract

STARS (Simple Transmission and Retrieval System) [1, 2] is a message transferring software for small-scale control systems with a TCP/IP socket, and it works on various types of operating systems. STARS is used as a beamline control system for controlling the optical devices (mirrors, monochrometers, etc.) for beamlines at the Photon Factory.

We have succeeded in running a STARS GUI client on Android using the STARS Java interface library. This achievement has brought with it the capability of developing a user-friendly GUI terminal using smartphones or tablet devices. Such a GUI terminal will help beamline users check movement near optical devices.

OVERVIEW OF STARS

STARS consists of a server program (STARS server) and client programs (STARS clients). Each client is connected to the server through a TCP/IP socket, and communicates using text-based messages (Fig. 1).

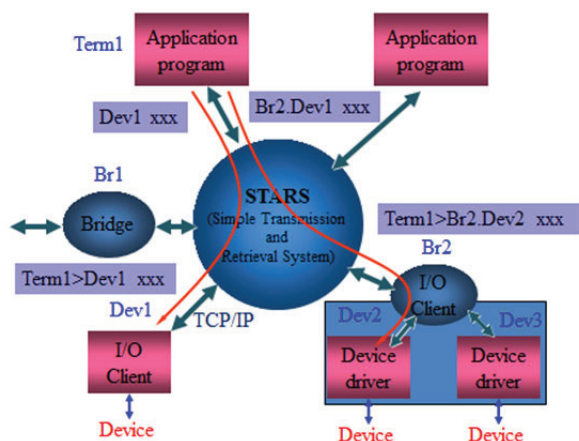


Figure 1: Message transfer between STARS clients and a STARS server.

Each client program has its own unique node name, and it sends text-based messages using the destination node name to the server, which then delivers the messages to the destination client. Through this extremely simple solution, STARS is able to provide basic control system functionality.

The STARS server program was written in Perl, and it can therefore run on various operating systems.

BEAMLINE CONTROL SYSTEM USING STARS

STARS has been installed in more than 20 beamlines of the Photon Factory as a beamline control system.

Before STARS was developed, the beamlines of the Photon Factory used various control systems (e.g., the originally developed software, LabVIEW, or SPEC) and the hardware was controlled using a software directory. At that time, staff members had to prepare their own hardware driver for each control system. Since the installation of STARS, however, hardware drivers are now developed by a “beamline control group,” and the beamline control system using STARS provides a common interface to GUI programs, etc., (Fig. 2) for handling the beamline components. This interface can also be accessed by various data acquisition systems.

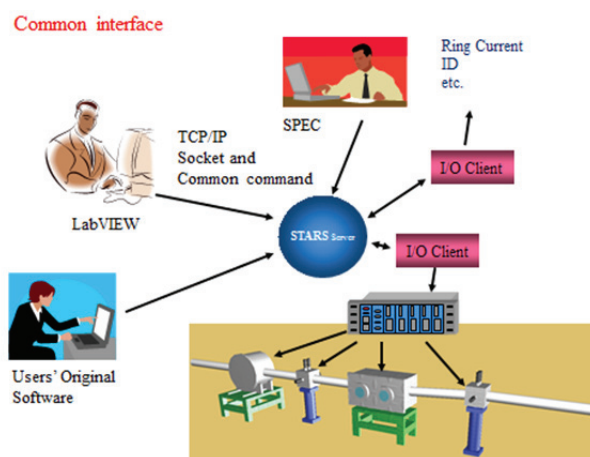


Figure 2: Common interface for handling beamline components using STARS.

Several types of driver software for beamline devices and common GUI programs have recently been developed at the Photon Factory.

STARS JAVA INTERFACE FOR ANDROID

STARS client programmers are required to use TCP/IP sockets and handle text-based messages, and although beginners may find it difficult, it is very easy for programmers with prior knowledge of TCP/IP socket programming to develop a STARS client. STARS is equipped with interface libraries for certain programming languages (Perl, VB, C# [3], C [4], and Java). Programmers need not be concerned with TCP/IP socket programming using these interface libraries. We modified a few parts of the source code for the STARS Java interface for Android.

DEVELOPMENT OF CLIENTS USING STARS JAVA INTERFACE FOR ANDROID

Development Environment

We used Eclipse for the development of the STARS client program for Android. Eclipse requires the

DEVELOPMENT OF EPICS CHANNEL ACCESS EMBEDDED ACTIVEX COMPONENTS FOR GUI DEVELOPMENT

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Abstract

The paper describes the integration of Experimental Physics & Industrial Control System (EPICS) Channel Access (CA) protocol and Microsoft ActiveX technology towards developing a generalize operator interface (OPI) building facility for Windows platform. EPICS is used as the development architecture of the control system in Superconducting Cyclotron (SCC). Considering the operators' familiarity and compatibility with third party software, it was decided to use MS-Windows platform at operator interface level in SCC during commission. Microsoft Visual Basic (VB) is used on trial basis as OPI building platform to incorporate user specific features e.g. file system access for data storage and analysis, user authentication at OPI level etc. A set of EPICS Channel Access embedded ActiveX components is developed to ease the programming complexity and reduce developmental time of the OPI for Windows platform. OPIs, developed using these components and containing hundreds of process parameters, are being used reliably over a considerable period of time.

INTRODUCTION

The $K_{\text{bend}}=520$ Superconducting Cyclotron, under commissioning activity at the centre, is expected accelerate heavy ion beams to energy up to 80 MeV/A for fully stripped light heavy ions and about 10 MeV/A for heavy ions. The Microsoft Windows XP was considered as the best suited platform at operation console level during the commissioning phase due to its compatibility with third party software, commonly used Microsoft tools and operators' familiarity. EPICS [1], a standard open-source dual layer software tool for designing distributed control system, is adopted to implement the in-house supervisory control software in SCC. The lower layer of EPICS i.e. Input Output Controllers (IOC), are realised mostly on Linux platform of various flavours to minimise compatibility issues and maximise operational reliability against malwares. There are standard EPICS tools e.g. EDM, MEDM etc. for developing OPIs in general for Linux platform. But porting these X windows based OPIs to windows platform require third party X server e.g. Exceed, Xming etc with expertise during installation. The users, ranging from operators to physicists to system personnel, have the requirements e.g. data archiving into local file for offline / online analysis, authentication based service, integrity with third party system etc. during commissioning phase. As the overall control system was not grown up to its fullest and there are no standard facilities/methods available in the standard OPI tools to

meet those custom requirements. Hence a methodology was required to be devised to meet specific requirements of this heterogeneous system. Developing OPIs for Windows platform integrated with standard Windows facilities, meeting user requirements, was the best option. The development of OPIs for Windows platform involved selection of developmental tools among the popular ones e.g. Microsoft Visual C or Visual Basic or National Instrument's LabVIEW, and Borland's Delphi and C++ Builder etc. The CA functionalities were to be incorporated for data access by integrating the CA library with developmental tool. This method, however, required us to understand each development tool's requirements for accessing C language function calls and maintaining this extra layer of code [2]. This results into longer developmental time and larger coding with associated complexity, efforts for testing and debugging for individual OPI.

Microsoft ActiveX technology is chosen to creating reusable, platform-independent, distributed, object-oriented binary software components with encapsulated CA functionalities. Microsoft Visual Basic (VB) is chosen as the OPI development platform considering its object oriented structure, rich GUI library and less complicated coding style. A number of different options currently exist for building CA clients on the Microsoft Windows platform [3]. These include Easy Channel Access (EZCA) [3], ActiveX CA, Simple CA (SCA) [2], Java CA (JCA), CA Java (CAJ) [4], and calling native code in CA via C++. EZCA is chosen to implement CA functionalities. Several CA ActiveX components, commonly used in OPI, are developed and are being used to develop OPIs in considerably reduced time frame.

EASY CHANNEL ACCESS (EZCA[†])

The EPICS channel access API was designed to implement a high performance network protocol including such features as data and connection call-backs, event notifications and smart aggregation of data requests [2]. EZCA is designed to provide an easy to use interface to CA [3]. The library composed of around twenty five API functions supporting CA functionalities e.g. data access (process value, precision, control limits, graphical limits etc.), error handling, grouping, monitors, and tuning. The data types supported by the library are byte, string, short, long, float and double. As VB is selected as developmental tool, EZCA is chosen due to its readily available VB interface supporting, not full but, necessary and sufficient CA functionalities. Although the tuning parameters of EZCA i.e. timeout and retry-count, are provided for improving reliability, the default parameter values are found to be suitable for our purpose.

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[†]Thanks to Nicholas T. Karonis, ANL for EZCA support.

DEVELOPMENT OF FAST CONTROLS FOR BEAM WIRE SCANNER FOR SuperKEKB

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Abstract

Recent development towards the data acquisition system of the wire scanner (WS) systems of the SuperKEKB injector linac (LINAC) and beam transport lines (BT's) is described. A VME based system, comprised of charge sensitive ADC (CSADC) board, scaler board, DAC board and Event receiver board, has been installed. The primary aim of the system is to utilise global linac event timing system for synchronized and mode-dependent data acquisition. A set of EPICS device driver has been developed for new hardware e.g. CSADC, scaler and DAC boards. The combination of latest versions of firmware and EPICS device driver for Micro Research Finland (MRF) Event receiver board is also evaluated and further incorporated in this system. The application software is developed for simultaneous acquisition of multiple beam mode data during multimode injection of the LINAC. The developed system is tested successfully after integrating with the existing wire scanner driving mechanism. The system enables the beam size measurements at four consecutive locations that derive Twiss parameters and ensure the reliable beam transport to four downstream storage rings.

INTRODUCTION

The KEK 8-GeV linac injects electron and positron beams with different characteristics into four storage rings: KEKB high-energy ring (HER), KEKB low-energy ring (LER), Photon Factory (PF) and PF-AR [1] [2]. The distance from the linac to the injection points of various storage rings is about 1km. A well controlled stable operation is required to maintain high luminosity. A wire scanner (WS) is useful for non-destructive monitoring of the beam profile for such long beam lines. A set of four WS are used for beam emittance and Twiss parameter calculation in optics matching. There are seven such matching sections in LINAC and BT's. The design of WS's and its measurement software were reported elsewhere [1, 3, 4].

At present, the WS's data acquisition system is comprised of CAMAC based front-end hardware e.g. CSADC, Scaler and DAC. A VME based supervisory system, running EPICS IOC on VxWorks 5.5, is used to control the pulse motor based WS system and Photomultiplier Tube (PMT) high voltage. An independent application program is used to acquire data from CAMAC hardware and save it in a memory based table. The supervisory system acquires the data from the table. The data acquisition process is synchronised with

the beam pulse by an independent gate generation system. Since LINAC is used for injecting beam of different characteristic into three storage rings (HER, LER and PF) simultaneously [5], hence a system synchronised with LINAC timing system, may be useful to acquire various beam mode data simultaneously. A VME based system, as shown in Fig.1, is developed to utilise timing system events for WS data acquisition. The speed of the wire is also changed while scanning the beam for obtaining maximum data points in minimum scanning time.

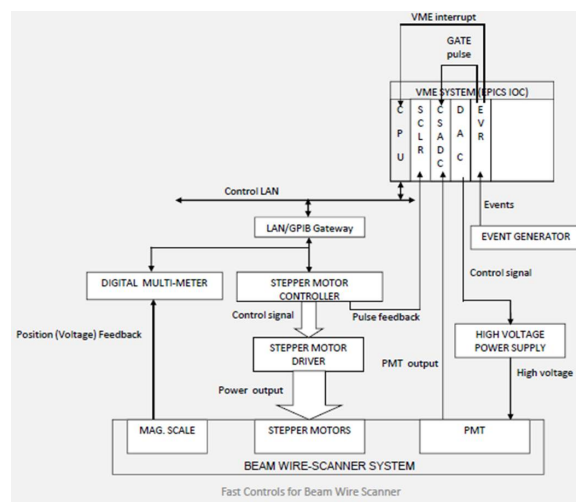


Figure1: Hardware architecture of the system.

HARDWARE

The new system is comprised of Motorola MVME-5500 CPU, Hoshin V004 Scaler, Hoshin V005 CSADC, PVME DAC, Agilent LAN/GPIB converter and Micro Research Finland Event Receiver (EVR). The system is connected to LINAC timing system using single mode optical fiber through EVR. The EVR is used to generate gate pulse for CSADC synchronised with incoming events from global event generator of the timing system. The movement of the wire is controlled through pulse motor controller using LAN/GPIB converter. A GPIB based multi-channel digital voltmeter is used measure the absolute wire position through potentiometric arrangement. The DAC is used to control the PMT bias voltage.

SOFTWARE

The Experimental Physics & Industrial Control System (EPICS), a standard open-source dual layer software tool for designing distributed control system, is adopted to

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GRAPHICAL USER INTERFACE (GUI) FOR TESTING CAMAC MODULES

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Abstract

A new program (GUI) for testing CAMAC modules (CAMAC ADC, DAC, Input Gate, Output Register) is developed using LabVIEW and dynamic link libraries (DLLs). On start-up, the program initializes the CAMAC Controller via PCI bus interface, thus enabling communication with CAMAC modules. It can test CAMAC modules through different controls like slider bars, buttons etc. and display status of individual channels with soft panel meters and LEDs. The GUI is extremely useful in troubleshooting hardware problems of CAMAC modules and also in developing new modules.

CAMAC TEST SET-UP DESCRIPTION

The CAMAC modules test program (GUI) is written in LabVIEW and has one page for testing CAMAC ADC/DAC modules and other page for testing CAMAC Input/output Gates. Figure 1 shows the basic block diagram of CAMAC Test set-up. The GUI communicates with the dynamic link libraries (DLL) which in turn call the PCI driver (associated with PCI Interface card). Separate DLLs are used to implement CAMAC read command and CAMAC write command. The DLL initiates the PCI Interface card to communicate with CAMAC controller via parallel bus interface. The CAMAC controller accepts command from PCI Interface card and passes that command to CAMAC modules via CAMAC bus. If it is a "CAMAC WRITE" command then the module receives data from PC in appropriate register (channel number called sub address). If it is a "CAMAC READ" command then the module sends data (from appropriate channel number) to PC via CAMAC Controller.

The CAMAC ADC/DAC page has user interface to enter station number N (where the module to be tested is present). The DAC has 8 channels and hence 8 slider bars are used to control each channel's voltage output from 0 to 10 V. If it is a 12-bit CAMAC DAC module located in slot number 12 and we want to set 5V at channel number 6, then station number entered into GUI is 12 and sixth slider is used to set 5V. 0 to 10 V is converted into 0 to 4095 (as DAC is 12 bit). 5 V is converted into 2047 by the slider control. This data is passed to CAMAC Controller which passes this to station number 12 (it also sets sub-address as 5 for channel number 6). The ADC has 16 channels and hence 16 meters are used to display individual channels voltage. The range of each meter is from 0 to 10 V. Each channel converts analog input (range 0 to 10 V) into digital number (0 to 4095) and this number is read by the CAMAC controller from ADC module's appropriate channel register and send to PC via PCI Interface card. The LabVIEW program will convert

this digital number into analog voltage (0 to 10V) and display it on respective channel meter. The page for CAMAC ADC/DAC module testing can test one ADC and one DAC module simultaneously.

The CAMAC Input/output gate page has user interface to enter station number (N). The Output Gate has 24 channels with each channel controlling an isolated relay contact. Whenever the channel receives logic '1' i.e 5 V input the relay operates and connects the output contact. Hence if we want to turn on the contact at 8th channel number, we have to press the eighth button (which when pressed turns green). Internally the GUI program converts this information into binary 24 bit word in which the eighth bit will be '1' and all other bits will be '0'.

Figure 2 shows us the snapshot of GUI program in LabVIEW which controls Output register and displays status of Input Gate. It also displays the internal logic value of Output Register which the user has changed. This internal register is first written by CAMAC Controller and then read by the LabVIEW program and displayed as 24 LEDs (instead of 24 bits).

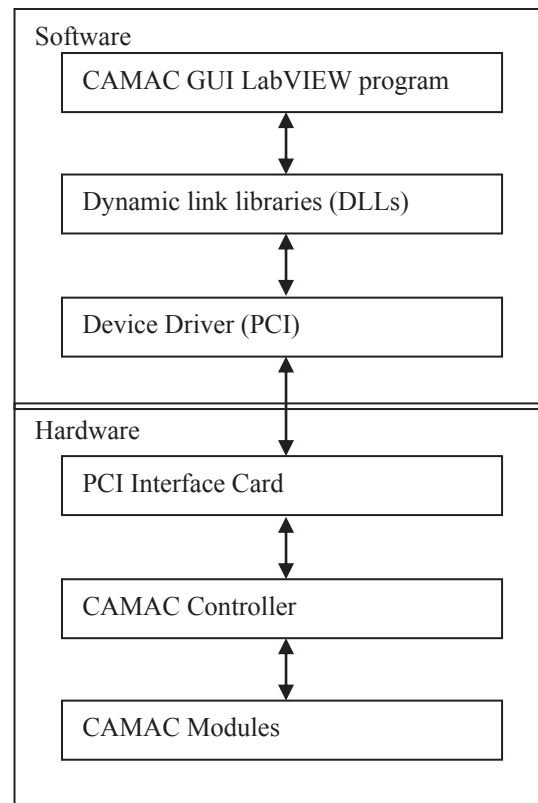


Figure 1: CAMAC Testing Set-up Block Diagram

RE-ENVISIONING THE OPERATOR CONSOLE FOR DHRUVA CONTROL ROOM

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Abstract

Control Room design is undergoing rapid changes with the progressive adoption of computerization and Automation. Advances in man-machine interfaces have further accelerated this trend. This paper presents the design and main features of Operator consoles (OC) for Dhruva control room developed using new technologies. The OCs have been designed so as not to burden the operator with information overload but to help him quickly assess the situation and timely take appropriate steps. The consoles provide minimalistic yet intuitive interfaces, context sensitive navigation, display of important information and progressive disclosure of situation based information. The use of animations, 3D graphics, and real time trends with the benefit of hardware acceleration to provide a resolution-independent rich user experience. The use of XAML, an XML based Mark-up Language for User Interface definition and C# for application logic resulted in complete separation of visual design, content, and logic. This also resulted in a workflow where separate teams could work on the UI and the logic of an application. The introduction of Model View View-Model has led to more testable and maintainable software.

INTRODUCTION

With years of Dhruva reactor operation, a need for up gradation of some of the instrumentation was felt in the data acquisition and processing systems, due to either obsolescence or for augmenting the facilities provided by the existing systems. Hence, taking due care of the retrofitting problems, some PC based systems have been implemented and others are being implemented in Dhruva. The Operator Consoles for these systems in Dhruva Control room have been upgraded with the latest UI design trends and technologies and created intuitive and flexible UX models. The computer based user interfaces with consistent and large screen overview displays have been introduced which has replaced the existing recorder-based displays.

DHRUVA OPERATOR CONSOLES

The Operator Consoles has been developed for continuous monitoring of nuclear, process parameters, radiation parameters and relevant status signals of Reactor Trip Logic System, Alarm Annunciation System, Emergency Core Cooling System and Start-up Logic System. The OCs acquire the data from the corresponding embedded systems via dual redundant Ethernet links. The primary function of OCs is data reception, storage and display in various formats.

They provide:

- Multiple views of plant state for quick assessment of situation.
- Alarm Visualization (Analysing, organizing, filtering, viewing alarms)
- Archival of Periodic Data, Alarms, Diagnostics with a data life cycle of 5 years.
- Logging and reporting with data export to Excel.
- Real-time and historical data trending.

DESIGN APPROACH

The OC has been designed keeping in mind the common requirements across systems of similar categories while allowing the UI to be tailored to specific requirements of the system. This has resulted in a common OC platform. Variability between these applications were analysed and addressed through configuration points. A flexible XML schema was designed to describe configuration information related to UI. Windows Presentation Foundation (WPF) helped in separating design and code, and provided comprehensive binding framework, command infrastructure, specialized layout builders for flexible UI creation. Loose coupling of the View from the supporting logic and data (Model) was achieved through the Model-View-View Model (MVVM) pattern. Asynchronous invocation, thread pooling and object pooling resulted in efficient use of multi-core hardware to achieve the required performance. Use of lightweight embedded relational storage engine resulted in high performance concurrent storage and retrieval system.

The design of UI was mainly focused to achieve visually appealing, feature oriented, intuitive, and less cluttered graphical user interface. The rest of the paper describes the UI concepts that were used for building the user interface of Operator Consoles.

Separation of Concerns

Model-View-ViewModel (MVVM), a design pattern for UI development consists of three conceptual parts - Model, View and ViewModel. The Model is the data, completely UI independent that stores the state and does the processing. The View consists of visual elements. The ViewModel is an abstraction of the view, but it also provides a specialization of the Model that the View uses for data-binding. This resulted in complete separation between visual design, content, and logic. The separation of concerns enabled UI Unit-testing, designer-developer workflow and decoupling. The layers could be developed and changed independently of one another, resulting in parallel development. View-Model classes are easy to unit-test since they have no specific dependencies on visual elements.

EMBEDDED PC BASED CONTROLLER FOR USE IN VME BUS BASED DATA ACQUISITION SYSTEM

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Abstract

An embedded PC based Controller module, named System Controller Module (SCM), has been developed at Reactor Control Division (RCnD), BARC. This module uses standard PC-104 bus based CPU module integrated with a protocol translator card to provide an interface between the CPU module and VME bus. The signal interface between PC-104 bus of CPU module and translator card is achieved through stackable connectors. SCM can be interfaced with 16-bit slave I/O modules on VME bus for Data Acquisition and Control. This development provides low cost PC based platform for developing I/O intensive embedded system requiring high processing power. SCM module is fully compatible with PC architecture and is available in Double Euro modular form factor. Module has self diagnostics features to test software integrity using onboard watchdog timer. The module provides dual Ethernet link for communication. The SCM has been assembled, integrated and successfully tested along with VME based high speed data acquisition system (Machinery Protection System), which has been developed in RCnD for condition monitoring of rotating machines. SCM acts as a configuration controller and data manager for this system.

INTRODUCTION

There are many different industrial buses and technologies used for different applications. VME is one of the popular 16/32/64 bit backplane bus [1] which has been used in many applications like control, aerospace, military etc. Embedded systems utilizing PC-104 bus based modules are also widely used in many data acquisition applications because of its features like small structure size, self-stacking, PC platform, high quality and low cost. Using these two widely used technologies, System Controller Module has been developed, which uses PC-104 bus based CPU module along with VME interface with standard VME based I/O modules for data acquisition and control. The VME interface is achieved by using a Protocol Translator Card, also known as Protocol Interface Card, which provides protocol interconnection between PC-104 bus signals and VME bus signals. The SCM has been designed, assembled, and successfully tested along with a VME based data acquisition system (Machinery Protection System).

VME BUS STRUCTURE AND CHARACTERISTICS

VME bus is one of the most popular standard bus because of its mechanical and electrical robustness. A large number of commercial products are available for this open standard. A product designed using the VME bus standard can be easily interfaced with off the shelf standard products. The VME bus standard specifies a high-performance backplane bus. The VME bus supports 8-, 16-, 32- or 64 bit data transfers over a non-multiplexed data and address highway. The transfer protocols are asynchronous and fully handshaken. The mechanical specifications of boards, backplanes, subracks, and enclosures are based on IEC 297 specification, also known as the Eurocard form factor [1].

The mechanical structure of a VME bus system consists of a backplane on which system bus resides. The backplane has 21 slots where CPU boards, memory boards or I/O boards connect to the system bus.

PC-104 BUS BASED MODULES

PC architectures are popular in both general purpose and dedicated (embedded) applications [2]. But because of the large form factor of PC motherboards and I/O cards, its application in embedded systems is limited. The embedded PC-104 bus uses the PC card specification but changes the form factor. The specification defines a new mechanical foot print and card power requirements. The PC-104 bus is an adaptation of the ISA bus for embedded computing use. It uses the same signals as ISA, but uses a smaller connector and cards that are stackable, which eliminates the need for a backplane. Use of PC-104 bus-based CPU modules in embedded systems provides PC hardware and software platform and ensures upgradability and protects against chip obsolescence [3]. PC-104 bus supports 8- and 16-bit data transfers.

The PC-104 bus based CPU module used in System Controller Module consists of 300 MHz Geode processor and 256 MB of SDRAM system memory. It provides 10/100 Mbps dual Ethernet port which can be used for high speed data communication. It also provides standard interface for I/O devices like USB, CRT, TFT, Mouse and Keyboard. It implements a Watch dog timer for software and hardware integrity. PC-104 module provides PC-104 expansion interface which is utilized for development of a Protocol Interface Card to facilitate VME interface.

DESIGN OF INTERFACE

The PC-104 bus based CPU module along with the Protocol Interface Card forms the System Controller

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A LOW-COST HIGH-PERFORMANCE EMBEDDED PLATFORM FOR ACCELERATOR CONTROLS

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Abstract

Over the last years the mobile and hand-held device market has seen a dramatic performance improvement of the microprocessors employed for these systems. As an interesting side effect, this brings the opportunity of adopting these microprocessors to build small low-cost embedded boards, featuring lots of processing power and input/output capabilities. Moreover, being capable of running a full featured operating system such as GNU/Linux, and even a control system toolkit such as Tango, these boards can also be used in control systems as front-end or embedded computers. In order to evaluate the feasibility of this idea, an activity has started at Elettra to select, evaluate and validate a commercial embedded device able to guarantee production grade reliability, competitive costs and an open source platform. The preliminary results of this work are presented.

INTRODUCTION

During the last years the requirements of particle accelerator control systems moved from the traditional distributed architecture, based on modular but complex platforms, such as VME, to even more distributed systems based on simple embedded devices [1,2,3]. The ever-growing performances of the modern hand-held oriented system-on-chip devices allow nowadays to fulfil these requirements. Desirable characteristics are:

- a large set of Input Output (I/O) subsystems (GPIO, SPI, UART, PWM, ...);
- remote control/communication interfaces;
- multiple communication protocols (UDP, TCP/IP, field-bus based);
- full Operating System (OS) support, with multitasking, multi-user, real-time capabilities;
- hardware, software and documentation support by either the manufacturer or a dedicated third part player;
- long term commercial availability and support;
- flexibility and modularity to cover a wide range of different fields of application;
- competitive cost-performance ratio;
- competitive development and maintenance costs;
- deterministic (real-time) capabilities.

Commercial-off-the-shelf (COTS) products that can match most, even if not all, of the described features are now available. Adopting the “system integrator” point of view, the available devices can be classified into the following levels:

- SOC (system on chip) level;

- SOM (system on module) level;
- SOB (system on board) level.

Design complexity, available resources and manpower are practical reasons that lead to choose the easiest, fastest and most effective solution: find the most suitable commercial SOB and customise it in order to fit the specific requirements.

MARKET SURVEY

A market survey has been carried out to find COTS products to compare, taking into account performance, reliability, lifetime and, last but not least, cost. This preliminary step has led to three product platforms: the iMX by Freescale [4], the OMAP and the Sitara by Texas Instruments (TI) [5].

The Freescale iMX53 “QSB” board has turned out to be a clean design, quite powerful for an embedded board, allowing the native porting of the Tango control system framework [6] in use for the FERMI@Elettra project [7]. On the downside, lacking a simple way to reach the I/O connector, the flexibility of the platform hasn't been satisfactory.

On the TI side, the “Beagle” family boards have been evaluated with good and encouraging results.

THE “BEAGLE” PLATFORM

Formally announced by Digi-Key [8] on July 28th, 2008, the “Beagle” project has been immediately able to collect the attention of a large community of developers whose main interest is focused on real and complete open source projects [9]. The Beagle family includes, at present, three different SOB's:

- the BeagleBoard, the first member of the family, a fully featured, low-power, high-performance Single Board Computer (SBC) based on TI OMAP3530 SOC, designed for user-oriented applications;
- the BeagleBoard-xM, the evolution of the BeagleBoard, based on OMAP compatible TI DM3730 SOC;
- the BeagleBone (Fig. 1), the most recent board of the family, based on TI Sitara AM335x SOC, designed for machine and/or industrial-oriented applications.

The BeagleBoard and the BeagleBoard-xM are, in principle, very similar to the iMX53 QSB board. This means that they are powerful devices from the computational point of view but, due to design decisions, they feature a small expansion connector, too limited to be used in an industrial oriented platform.

A WIRELESS CONTROL SYSTEM FOR THE HTS-ECRIS, PKDELIS AND LOW ENERGY BEAM TRANSPORT

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Abstract

The 18 GHz High Temperature Superconducting ECR ion source at the Inter University Accelerator Centre (IUAC), New Delhi is the first High Temperature ECR Ion source designed for operation on a 400 kV high voltage platform as part of the High Current Injector development programme. For automation of source operation and control of source parameters, a wireless control system has been developed. Connection to the Ethernet based central control system has been provided.

INTRODUCTION

The 18 GHz High Temperature Superconducting ECR ion source (ECRIS), PKDELIS[1, 2], is designed to inject multiply charged ion beams into the superconducting linear accelerator. The HTS-ECRIS is driven by an 18 GHz, 1.8 kW klystron and has been recently upgraded with an additional frequency by incorporating a TWT amplifier for alternate frequency injection and for double frequency operation [3]. The low energy beam transport section consists of the HTS -ECRIS, beam extraction system and a large acceptance mass analyser followed by a diagnostic system consisting of double slits, beam profile monitors and faraday cups [4]. The control system has been designed keeping standardization and reliability of the complete system. Module backplane, isolation channel, IO hardware and embedded hardware are industrial strength, fail-safe, reliable and widely supported. Speeds of module backplane, IO hardware and isolation channels are sufficient for feeding the control and automation requirements. Incorporation of spark protection and safety interlock systems are additional requirements for smooth operation of the complete system. Fieldbus technology offers several benefits in an ion source control application. An RS-485 MODBUS/RTU module backplane can be implemented using a single twisted pair and connect seamlessly to a wireless isolation channel, forming an industrial strength system. Simplicity of this bus helps ruggedness and easy maintenance. Multiple sourcing of industrial strength ADCs, DACs, DIO, relays and thermocouple modules is supported. Large amount of software development bus has been implemented as module backplane. This network, spread across the isolation channel (Radio Modems), appears as a local RS-485 MODBUS to the control computer on the ground. Such direct integration support for both Windows and LINUX systems is available. An RS-485 MODBUS/RTU twisted pair local of the isolation channel makes control parameters available in real time. The system has proven to be simple, rugged, robust economical and reliable. Common

electrical isolation channels in ion sources are fibre optic links. However, a radio channel can maximize reliability and minimize downtime due to total absence of any mechanical contacts and make source operation easy and convenient. Commercially available ISM band 2.45 GHz CDMA radio modems have high data integrity and reliability. The TWT amplifier and associated function generator provide only GPIB channel for control. These systems are connected using a GPIB to RS-232 conversion and connection via a Radio Modem. An additional software module for interfacing to the GPIB functions via the converter is then required. The central control system of IUAC runs a high level protocol using an Ethernet TCP/IP based central control scheme. A distributed control topology is used to enable control from the control room of IUAC. Several enhanced control functions are available in the local mode. Local control also supports enhanced graphics and GUI based control functionality. The system has been running for more than five years with reliable operation.

DESCRIPTION

A block diagram of the system architecture is shown in Figure 1. Radio modem links RM1a-RM1b and RM2a-RM2b provide the basic isolation channels for systems of the source on a 400 kV high voltage platform. The RM1a-RM1b link provides control of all the parameters. The RM2a-RM2b link is for the GPIB based second link for the TWT amplifier and the function generator associated with it. The ground potential systems have more flexibility due lack of the limitation of the isolation channel. A non-isolated RS485 MODBUS serves this purpose. The MODBUS parameter scan program scans the bus for all the parameters at a regular interval. The scaling and linearization is done individually and the parameters are displayed graphically as well on GUI objects.

Interlocks are provided via PLCs as they provide the most modern and reliable mode of interlock. They can also be connected to the control system to provide the interlock status. They also provide connectivity using standard protocols.

SOFTWARE SYSTEM

A simplified block diagram of the software is shown in Figure 2. The program uses GUI for display of control and read-back parameters. Graphical plots provide histories of vital parameters like gas pressure, vacuum levels at various positions in the beam-line, drain currents from power supplies etc. Addition of auto-scan and interlock features has been implemented. To support Ethernet based control protocol, a service interface has

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DEVELOPMENT OF AN ETHERNET ENABLED MICROCONTROLLER BASED MODULE FOR SUPECONDUCTING CYCLOTRON ECR BEAM LINE CONTROL

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Abstract:

An Ethernet enabled control and data acquisition module is developed for remote control and monitoring of the ECR beam line equipment of the Superconducting Cyclotron. The PIC microcontroller based module supports multiple general purpose analog and digital inputs and outputs for interfacing with various equipments and an embedded web server. The remote monitoring and control of the equipment are achieved through the web based user interface. The user authenticated access to control parameters and module configuration parameters ensures the operational safety of the equipment under control. This module is installed in Superconducting Cyclotron ECR beam line for the control and monitoring of vacuum pumping modules, comprising of pumps, gate valves and dual vacuum gauges. The installation of these modules results in a distributed control with localised field cabling and hence better fault diagnosis.

INTRODUCTION

The Electron Cyclotron Resonance Ion Source (ECRIS) plays a major role in generation and injection of the different ions to be accelerated by the Superconducting Cyclotron. ECR ion source develops multiply charged ions which are transported to the cyclotron through the injection line.

A large number of beam line equipments including various types of magnets, beam diagnostics elements, vacuum system components etc are required to be monitored and controlled for efficient transportation of the ion species. Among these elements, the vacuum pumping modules, though crucial for maintaining high level of vacuum inside the ion source and the injection line, are operated less frequently. Each pumping module again comprises of a scroll pump, a turbomolecular pump, various valves and vacuum gauges which altogether can be considered as a complete unit of one pumping station. Hence a generalised, modular, distributed control and data acquisition system for the pumping stations as well as for other diagnostic elements result into a compact, less complicated and cost effective solution.

Microcontroller is the obvious choice considering its cheaper cost, faster development, and rich in built external interfaces. But the connectivity for data communication to PC is limited to serial interface for the microcontrollers.

In recent time, the Ethernet protocol has been widely adapted for data communication over wide area. Therefore a microcontroller based control and data acquisition module with embedded Ethernet connectivity is the optimum choice for the above mentioned control system.

In this paper, the development of an Ethernet enabled control and data acquisition module with embedded web server is explained along with the hardware and software environment detail. The schematic in Figure. 1 shows the basic architecture of the module.

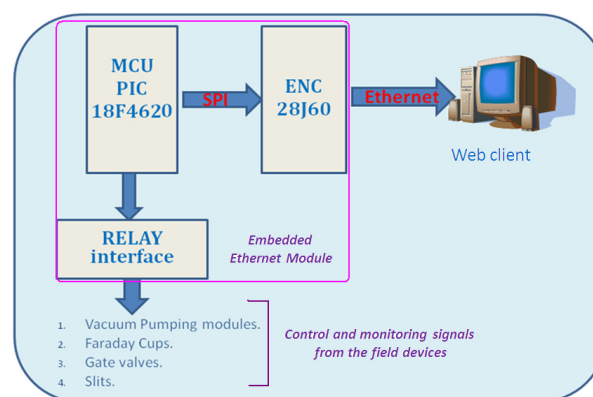


Figure 1: Block schematic of the control architecture.

HARDWARE OVERVIEW

The Ethernet enabled control and data acquisition module is developed for remote control and monitoring of these ECR beam line equipments. An embedded web server along with the other essential hardware makes the module suitable for control and monitoring of the field devices over LAN. The schematic in Figure .1 shows the basic architecture of the module.

Microcontroller

The microchip PIC controller 18F4620 is used as the main controller. It is an 8 bit microcontroller with 64kbytes of Flash, 10 bit, 13 channel ADC, 31 level stack and 36 Inputs and outputs (I/O). The 1Kbyte of EEPROM data memory available in this IC is used to store the configuration data. The Master Synchronous serial port (MSSP) module in this microcontroller supports 3 wire SPI communication, used for communicating with Ethernet controller.

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A NEW SCHEME FOR DIRECT ESTIMATION OF PID CONTROLLER PARAMETERS

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Abstract

This paper presents a novel scheme for the direct estimation of a PID (Proportional Integral Derivative) controller parameters (K_p , T_i , T_d). The proposal discussed here is only applicable to first and second order stable systems. The formulation begins with system parameter identification (Transfer function of the process), which has been obtained using system identification toolbox of MATLAB. The pole zero cancellation technique is applied to estimate PID controller parameters which in turn results into the matched coefficients of the system parameters to the Controller parameters. An additional tuning parameters α is proposed in our method, which provides an additional flexibility of tuning the response time of the controller without disturbing the controller parameters. The proposed scheme is bench marked using real time case of dc motor speed control. The effectiveness and robustness of the proposed auto tuning algorithm are verified by the simulation results.

INTRODUCTION

A Proportional-Integral-Derivative (PID) controller is the most widely used controller in the industry today. The popularity of PID controller is due to its simplicity which uses only three, parameters to tune. Proportional (K_p) term which controls the plant (system) proportional to the input error. Integral (T_i) term which provides the change in the control input proportional to the integral of the error signal and the last one is the Derivative term (T_d) that control the system by providing control signal proportional to the derivative of the error signal. Derivative action is used in some cases to speed up the response time and to stabilize the system behavior [1]. Error value is the difference between the set Reference value and the output value.

Although the PID controller is known to be the simplest and efficient controller, but it requires effective and optimized tuning of the control parameters (K_p , T_i , T_d). Many PID controller tuning methods have been proposed in the literature, some of the popular methods are Ziegler-Nichols tuning, Cohen-Coon tuning, internal model control, direct synthesis method, neural networks based methodologies, relay based auto tuning method and may be much more [2]. In this paper a simple auto-tuning method is proposed which can be applied to most of the stable first and second order systems without having time delay. The proposed tuning method comprises of two parts. First part is used for finding the system transfer function identification. Second part is used for obtaining PID parameter by arranging the parameters in such a way

that the pole of the second order transfer function can be cancelled by the zeros of the PID parameters. In this way by introducing an extra parameter that is gain ' α ' we can optimize the rise time and settling time of the system. This technique basically tunes the PID parameter in a single iteration and thus it is fast and easy to implement. The paper is organized as follows. In section 2 we have discussed how to obtain the transfer function of an unknown system whereas in section 3 the PID tuning methodology is discussed. In section 4 we have presented the real time simulated case study of DC motor speed control that is done in MATLAB Simulink environment. A brief conclusion is presented in section 5.

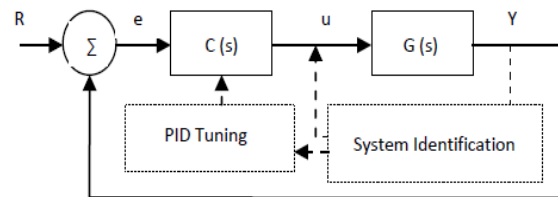


Figure 1: Auto Tuning Scheme of PID Controller.

SYSTEM IDENTIFICATION

The system identification is the method of finding the transfer function of an unknown system by observing the input and output sequences of the system as shown in the figure 1. The transfer function (TF) identification was carried out by using system identification toolbox of the MATLAB. Let the measured input and output sequences are given by matrix:

$$\Psi(k) = \begin{Bmatrix} -y(k-1), -y(k-2) \cdots -y(k-n), \\ u(k-1), u(k-2) \cdots u(k-n) \end{Bmatrix}^T \quad (1)$$

The dynamics of the system is given by:

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, \mathbf{u}; \boldsymbol{\theta}) \quad (2)$$

where \mathbf{x} is the state variable, \mathbf{u} is the input vector and $\boldsymbol{\theta}$ is the parameter vector.

$$\boldsymbol{\theta} = [a_1 \ a_2 \ \cdots \ a_n \ b_1 \ b_2 \ \cdots \ b_n]^T \quad (3)$$

We have to choose the value of parameter vector $\boldsymbol{\theta}$ in such a way so that the difference between $\dot{\mathbf{x}}$ and $\mathbf{f}(\mathbf{x}, \mathbf{u}; \boldsymbol{\theta})$ will impose minimum error. There are several techniques available in literature. MATLAB has in build procedure to find out the TF of the system by measuring input and

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FPGA DATA BLOCK FIFO FOR THE APS ID MEASUREMENT SYSTEM*

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Abstract

A Hall probe insertion device (ID) measurement system has been developed to characterize the IDs at the Advanced Photon Source (APS). The system uses the latest state-of-the-art field-programmable gate array (FPGA) technology to synchronize the position and Hall voltage measurements. Data block first-in-first-out (FIFO) has been implemented to transfer the data from the FPGA to the host computer during measurement. The system is capable of continuous scanning measurements on a full 6-meter bench at 1 msec per data point with a position resolution of 1 micron and Hall voltage precision of 5-1/2 digits.

INTRODUCTION

Insertion devices (IDs) at the Advanced Photon Source (APS) are measured and fine-tuned against their design specifications at the magnetic measurement laboratory [1] before installation into the storage ring. The APS Hall probe measurement system is designed to measure the magnetic field distributions of the IDs. The system has been upgraded with the latest state-of-the-art field-programmable gate array (FPGA) technology to synchronize the measurements of position and Hall voltage.

Since the FPGA hardware has limited onboard memory capacities, data block FIFO has been implemented to transfer measurement data to the host computer efficiently during measurements. The new system is capable of continuous scanning measurements of the IDs at the speed of 20 cm/sec with a spatial resolution of 0.2 mm reliably.

SYSTEM DESCRIPTION

The Hall probe measurement system consists of the following subsystems shown in Figure 1.

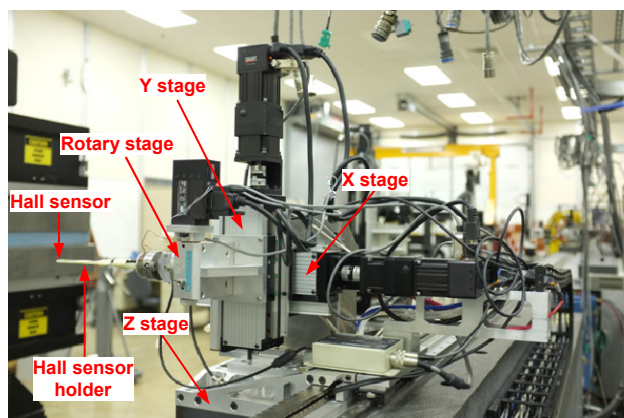


Figure 1: Hall probe measurement system.

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A rotary stage carries the Hall sensor holder. A two-axis (X and Y) linear stage with digital linear encoders supports the rotary stage. All the stages are remotely controlled by servo motors. A (Z) linear carriage with air bearings carries the stages as well as all the pre-amplifiers and electronics moving along the Z direction. The linear carriage is remotely controlled by a linear servo motor. A 7-meter-long granite table with a 6.8-meter linear digital encoder hosts the carriage as well as the cables and air tubes.

A high-precision Hall probe sensor is mounted on the sensor holder. A PXI shelf with a control card hosts the FPGA card and digital multimeter (DMM) card. Software programs are hosted on the control card.

SYSTEM CONTROL, DATA ACQUISITION, AND ANALYSIS

LabVIEW-based system software has been developed to coordinate the stage control and data acquisition. Figure 2 shows the schematic layout of the system control and data acquisition architecture. The system can be accessed via the Internet from anywhere at any time, wired or wireless, through the remote desktop interface.

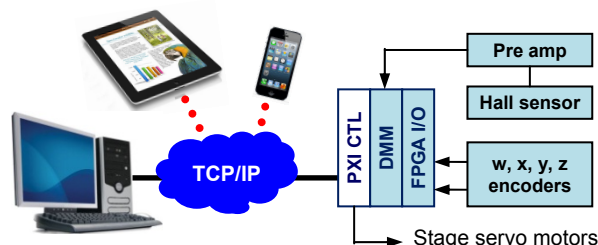


Figure 2: System control and data acquisition architecture schematic layout.

The system software sets the FPGA firmware to monitor the stage digital encoder positions and commands the stage scan across the measurement region. For each measurement point, the FPGA checks if the DMM is ready for measurement. If so, it trigs the DMM to take a Hall voltage measurement and records the position information to its memory; otherwise, it skips the position recording of that point. Once the DMM finishes the measurement, it will flag its state to the FPGA and wait for the next measurement trigger by the FPGA. All the above tasks are carried out on the fly. This approach guarantees that every Hall voltage measurement pairs with its position information no matter how fast the stage moves.

The FPGA onboard memory has been configured into three blocks for data block FIFO. Once the first block is full, a flag is set and the control card starts to read the data in the first block while the second block is recording,

LOW-COST EPICS CONTROL USING SERIAL-LAN MODULE XPort

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Abstract

In J-PARC Main Ring, we are interested in a commercial product, XPort, a low-cost serial-LAN converter module. We have introduced it in two different devices: RF-amplifiers with GPIB, and a NIM module with switches. Control messages are transported over network, and converted into EPICS-style records.

Implementation details and operational experiences are given.

INTRODUCTION

The J-PARC Main Ring (hereafter MR) is a high-power proton synchrotron with beam-energy 30-GeV. Since 2008, various machine upgrades toward higher beam-power have been carried out [1-3]. The control system for MR has been developed based on EPICS (Experimental Physics and Industrial Control System) [4], where EPICS is a toolkit for large accelerator controls developed and supported by an international community [5].

It is often the case that small devices are newly introduced in order to improve accelerator performance. Typical devices are, for example, a power-supply, an electric circuit board, a stand-alone measuring system, and so on. Sometimes they have a poor interface to link to the original control system.

We, J-PARC MR control group, are interested in a commercial product, XPort [6,7]. It is a low-cost serial-LAN converter module. We implemented it into two newly introduced devices: RF-amplifiers and a NIM module with front-panel switches. In both cases, control messages are transported to an EPICS IOC (Input Output Controller) over the network. They are converted into EPICS-style records using EPICS AsyncDriver.

IMPLEMENT XPORT TO DEVICES

What is XPort

XPort is a commercial product provided by Lantronix [4]. It is an embedded device server with various network protocols, such as TCP, UDP, SNMP, TFTP, http, and so on. It has programmable 3 I/O pins, which can be used for serial communication or bi-directional digital I/O signals. The size of XPort is as small as a RJ-45 connector. Thus, it is easy to mount an XPort module on an electric circuit board (Figure 1).

Implement XPort to RF-Amplifier

In order to improve beam quality in MR slow-extraction operation, RF-amplifiers are used to add transverse noises to beam bunches [8,9]. Amplifiers are commercial products with GPIB as a default interface. We asked a company to add an XPort module for remote control. Serial messages of GPIB are simply transported over our control network, using TCP protocol.

Table 1 shows part of supported GPIB commands for the RF-amplifier. We developed EPICS configurations, device-support structures and databases as in Figure 3. Network-serial communication feature of EPICS AsyncDriver is used. Control panel was developed using an EPICS tool, MEDM, as in Figure 2.

Table 1: GPIB commands of RF-amplifier.

Function	Command	Replay message
RF SW ON	"P1"	None
RF SW OFF	"P0"	None
RF SW status	"P?"	"P1" or "P0"
Forward Power	"FMON"	Ex) "2500W"



Figure 1: XPort module mounted on a board.

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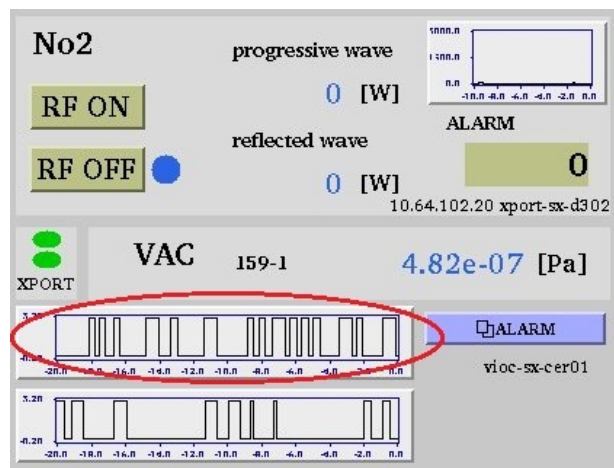


Figure 2: RF-Amplifier control panel.

FACILITY-WIDE SYNCHRONIZATION OF STANDARD FAIR EQUIPMENT CONTROLLERS

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Abstract

The standard equipment controller under development for the new FAIR accelerator facility is the Scalable Control Unit (SCU). It is designed to synchronize and control the actions of up to 12 purpose-built slave cards, connected in a proprietary crate by a parallel backplane. Inter-crate coordination and facility-wide synchronization are a core FAIR requirement and thus precise timing of SCU slave actions is of vital importance.

The SCU consists primarily of two components, an x86 COM Express daughter board and a carrier board with an Altera Arria II GX FPGA, interconnected by PCI Express. The x86 receives configuration and set values with which it programs the real-time event-condition-action (ECA) unit in the FPGA. The ECA unit receives event messages via the timing network, which also synchronizes the clocks of all SCUs in the facility using White Rabbit. Matching events trigger actions on the SCU slave cards such as: ramping magnets, triggering kickers, etc.

Timing requirements differ depending on the action taken. For softer real-time actions, an interrupt can be generated for complex processing on the x86. Alternatively, the FPGA can directly fire a pulse out a LEMO output or an immediate SCU bus operation. The delay and synchronization achievable in each case differs and this paper examines the timing performance of each to determine which approach is appropriate for the required actions.

INTRODUCTION

In the FAIR control system, a data master issues high-level commands to control accelerator devices. The front-end controllers in the system react to relevant commands, issuing appropriate actions to their hardware components. Depending on the action to be taken, there are different timing requirements to be met.

Unlike the control system currently deployed at GSI, commands issued by the data master carry an absolute execution timestamp. The front-end controllers must receive commands early enough that they can schedule their actions to achieve the desired result at the correct time. Unfortunately, executing actions takes a variable amount of time. If the action takes 90-110 μ s to execute, then this places two constraints on the system. Firstly, the data master must issue commands at least 110 μ s ahead of time. Secondly, the system must be able to tolerate that the action could be as much as 10 μ s too early or too late.

Issuing commands too far in advance reduces the responsiveness of the system. Once the data master has issued a command, it cannot be aborted. If the situation changes, perhaps due to interlock or contention from another beam

user, the system cannot react faster than the slowest action already executing. This neglects, of course, other sources of latency in the system, such as network propagation delay, which only exacerbate the problem. It is thus generally desirable to have fast action execution.

Non-deterministic execution time is a potentially much more serious problem. For example, if a kicker executes an action a few nanoseconds too late, the beam might be lost. However, not all actions require the same precision, and it may make sense to trade accuracy for flexibility in some situations.

Fortunately, the most common equipment controller in FAIR, the Scalable Control Unit (SCU), has several possibilities for executing actions. This paper outlines the timing requirements of various accelerator components in FAIR and explores the alternatives which could meet them.

USE CASES

The SCU will be the main frontend controller for the FAIR project. It provides a uniform platform connected both to the timing- and the data network of the facility. In turn, the SCU controls Adaptive Control Units (ACU) [1] slaves of various form factors which provide additional features and the necessary hard- and software interfaces to control the actual accelerator components. This means a wide range of magnet power supplies, Radio Frequency (RF) components and beam diagnosis equipment. The set of executable actions of course varies depending on the connected equipment. A magnet power supply for example will be provided with parameters and timed instructions to source a current ramp to its magnet, an RF generator gets different sets of frequency and phase parameters and the time when it needs to switch between them. The basic concept of the SCU envisions a complete separation of data supply and timing/commands. This way it can make use of higher abstraction levels, i.e. complex software, which brings flexibility, is more comfortable and maintainable, and also use low level hardware implementations to provide fast, deterministic behavior for the precisely scheduled execution of commands. The device controlled in the RF use case is called FPGA Interface Board (FIB) [2]. The kicker modules will be controlled by interface devices called IFK via a MIL-STD-1553 based field bus system.

SCALABLE CONTROL UNIT (SCU)

The SCU is mechanically a stack of up to three separate boards. There is the FPGA base board with an Arria II FPGA, two Small Form-factor Pluggable (SFP) slots, DDR3 RAM, parallel flash and a parallel bus (SCU bus)

DIAMOND LIGHT SOURCE CONTROL SYSTEMS RELATIONAL DATABASE

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Abstract

The functionality of the Diamond Light Source Control Systems Relational Database (RDB) is described in this article. An Oracle-based RDB and web-based GUIs allow recording of system configuration and configuration change management. Information about the hardware components that make up each beamline crate is stored in the RDB; for each item of control equipment, the status, location and name of the person responsible for the item are held. The Diamond Control System is based on EPICS [1] and has of the order of 500,000 process variables. The RDB maintains a record of the names of these PVs and validates new names against the Diamond Naming Convention, allowing consistency of naming style to be maintained and avoiding name duplication.

Machine operational details such as alarm logs are stored in the RDB and viewed using a web browser. All process data recorded by the control software are archived using the EPICS Channel Archiver; the archiver configuration for each technical area is maintained in the RDB. A further application using the RDB is the electronic logbook (eLog) which is used to record activities by Diamond Operations and Beamline groups.

INTRODUCTION

Diamond Light Source (DLS) is a 3 GeV third-generation light source with a 561m storage ring (SR), a full-energy booster (BR) and a 100 MeV pre-injector Linac [2]. The photon output is optimised for high brightness from undulators and high flux from multi-pole wigglers. The current operational state includes 19 photon beamlines, with a further three beamlines in an advanced stages of design and construction. A further phase of photon beamlines has now been confirmed; detailed design and construction of these 10 beamlines started earlier this year.

The Diamond Control Systems Relational Database is based on the following software:

- Database: Oracle 11g Standard Edition;
- Entity Relationship Diagram: ER Studio;
- Language: PHP (Hypertext Preprocessor);
- Web server: Apache;
- Operating System: Red Hat Linux Enterprise Edition 5.

Development of the RDB was carried out in parallel with the Diamond Light Source design, so that it was available to be populated during the Diamond construction phase. Since then, it has undergone continuous development to meet new requirements as these arise.

DIAMOND NAMING CONVENTION

The RDB structure for the validation and recording of database names is shown in Figure 1. A device name can consist of up to a maximum of 17 alphanumeric characters. It can be broken down into 4 or 5 sections. The '-' character is used to delimit the sections and is the only non-alphanumeric character allowed.

The format is as follows:

DD[SSS]-TT-CCCC-NN

Where [...] indicates an optional section.

DD	Domain
SSS	Sub Domain (Optional)
TT	Technical Area
CCCC	Component
NN	Identifier

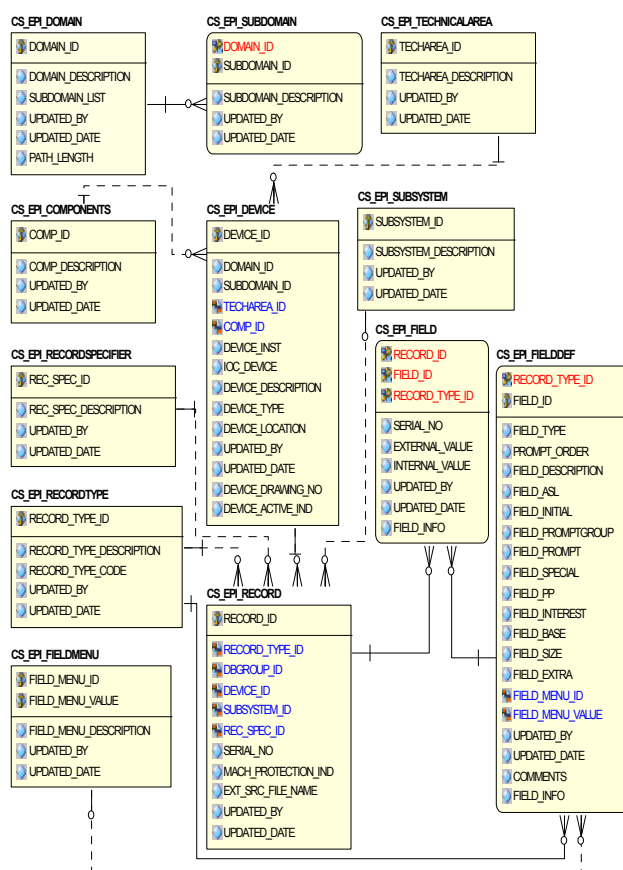


Figure 1: Database design for Naming Convention

The device name DD[SSS]-TT-CCCC-NN uniquely identifies a device, such as a power supply, a gauge, etc. Properties associated with controlling or monitoring that device are identified by extending the device name with record specifiers. These define the signals associated

CURRENT STATUS AND UPGRADE PLAN OF THE DATA-ACQUISITION SYSTEM AT SACLA

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Abstract

User experiments at the SPRing-8 angstrom compact free electron laser (SACLA) facility were recently commenced, in March 2012. We have developed a dedicated data-acquisition system that can be used for user experiments. This system is currently capable of acquiring data from 10 multiport charge-coupled device sensors at a data rate of up to 5 gigabits per second (Gb/s). In this paper, we present an overview of this data-acquisition system.

OVERVIEW OF SACLA

The SPRing-8 angstrom compact free electron laser (SACLA) facility is an X-ray free electron laser (XFEL) facility located at the SPRing-8 site in Japan. This facility is characterized by its compact design; it is about 700-m long and includes the accelerator, undulator, and experimental buildings. To achieve the compact XFEL design, we performed the relevant technical development activities such as of the C-band accelerating cavity, in-vacuum undulator, timing, optics, detectors, and data-acquisition system. A significant advantage of the SACLA–SPRing-8 experimental facility is that we can use two X-rays, one from SACLA and one from SPRing-8, simultaneously. The first self-amplified spontaneous emission (SASE) lasing of SACLA was achieved in June 2011, and X-ray laser beams have been delivered to users since March 2012 [1]. XFEL wavelengths in the subangstrom region (0.6 \AA) have been realized. During the first experimental period from March to July 2012, 25 experiments covering atomic, molecular, and optical physics, ultrafast science, material science, and structural biology were carried out.

OVERVIEW OF THE DATA-ACQUISITION SYSTEM

We have developed a dedicated data-acquisition (DAQ) system that can be used for user experiments at SACLA. The DAQ system consists of a number of components: detectors, a front-end system, data-handling servers, a cache storage system, an event-synchronized database (DB), a high-performance PC cluster (HPC), and a large-bandwidth network. We chose standard interfaces to connect components with each other. To match the needs of future experiments, the DAQ performance will be upgraded by replacing the DAQ system components. Figure 1 shows an overview of the SACLA DAQ system. In this section, we describe the current status of each component.

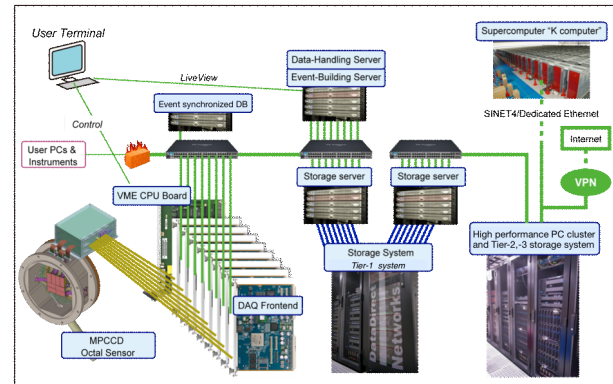


Figure 1: Overview of the DAQ system. The current DAQ system supports up to 10 multiport charge-coupled device sensors.

Multi-Port Charge-Coupled Device Sensors

The multi-port charge-coupled device (MPCCD) sensor is a two-dimensional X-ray detector developed for SACLA experiments [2]. Each pixel of the MPCCD is $50 \times 50 \mu\text{m}^2$ with a 16-bit data depth. A single MPCCD sensor module has 512×1024 net pixels. Inclusive of calibration data, 512×1032 gross pixels per shot are acquired by the sensor at a repetition rate of 60 Hz. MPCCD sensors can be used in one of the following typical configurations: 1 (single), 2 (dual), and 8 (octal) sensors. We decided to use either the single configuration or the octal + dual combined configuration. For the single and combined configurations (1 and $8 + 2$ sensors), data rates are about 500 megabits per second (Mb/s) and 5 gigabits per second (Gb/s), respectively. We have developed downstream components for the DAQ system to satisfy such high data rate requirements.

We chose Camera Link [3] as the digital interface between the MPCCD sensors and the front-end system. By standardizing the front-end interface as the Camera Link, not only MPCCD sensors but other commercial cameras such as IMPERX [4] and OPAL [5] can also be used. The Camera Link interface provides a bandwidth $> 2 \text{ Gb/s}$ (base configuration), which satisfies the data-rate requirements of the MPCCD sensors.

Front-End System

Because the physical range of Camera Link is short (several meters), the front-end system is aimed at receiving and transferring data from Camera Link to Ethernet. We developed two different front-end systems [6]: a PC-based

THE IUAC TANDEM-LINAC CONTROL SYSTEM

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Abstract

The 16MV Tandem Van de Graaff accelerator at IUAC is one of the earliest machines to go for a PC based control system. The PDP11, supplied with it, was replaced by an IBM PC running DOS before the accelerator was commissioned in 1989. The present system, commissioned in 1997 and supports LINAC, runs on a network of PCs under the GNU/Linux operating system. Every parameter to be controlled/monitored is assigned a unique identifier consisting of a Label, Function and Unit. The signals are grouped according to location and they are connected to server PCs using interfaces like CAMAC, VME or custom hardware. The features like a user interface, alarm systems, data logging and partial automation are handled by several client programs, communicating to multiple servers to access the hardware over a TCP/IP connection.

INTRODUCTION

Inter-University Accelerator Centre has a 16 MV Tandem Van de Graaff accelerator and a super-conducting heavy ion LINAC. The Tandem was originally supplied with CAMAC Serial Highway Interface and a DEC PDP11 based control system. The PDP11 was replaced by a PC based system running DOS before the accelerator was commissioned [1]. Later on, the addition of the LINAC demanded features like multiple operator consoles and the ability to run special purpose programs to condition the resonator cavity, automatically setting the amplitude and phase of RF etc. To meet the new requirements, a new control system was developed with the following basic guidelines; low implementation and maintenance costs, reliability, flexibility and scalability. PCs connected over Ethernet, running GNU/Linux operating system, forms the basic computer network required for the system. CAMAC, VME and custom hardware are supported.

DESIGN

The main task of the accelerator control system is to monitor/control signals from various devices like power supplies, vacuum systems, beam monitors and so on. Each device may have one or more analog/digital signals to be controlled or monitored, resulting in a large pool of signals. We have assigned a unique identifier for each signal. Three character strings, Name, Function and Unit, uniquely identify each parameter in the whole system. For example "CPS031", "VC", "KV" identifies the Charging Chain power supply voltage control signal. This nomenclature is followed mainly because our accelerator people were already familiar with it. The signals are grouped according to location and each group is connected to server PC, closer

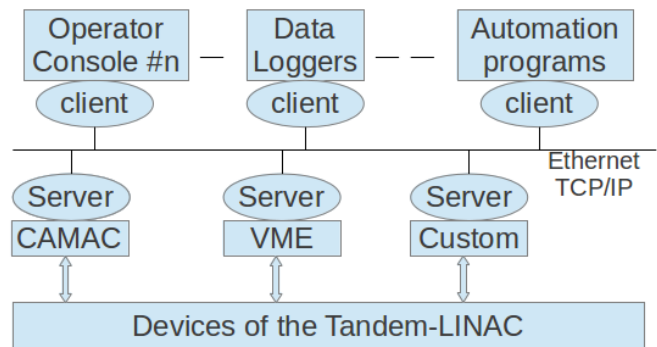


Figure 1: Schematic of Control System Hardware.

to the devices, using interfaces like CAMAC, VME or custom hardware.

The computers connected to the hardware runs a server program supporting the control/monitor of the signals over a TCP/IP connection. Only the unique signal identifier is known outside the server, the hardware details and the complexities of all the signals are hidden from the outside world. A simple message passing protocol, over a TCP connection, supporting functions like getState, setState, getValue and setValue are used for accessing the signals from remote computers running client programs.

HARDWARE

In the accelerator we have devices requiring analog and digital type signals for controlling/monitoring. Signals from devices located nearby are grouped and connected to one computer, using CAMAC, VME or some custom hardware interface. Several such groups are required to take care of all the signals. Each signal is characterized by a unique name and interfacing details like hardware address and datasize. Most of them are handled using standard modules like ADC, DACs, Output Registers and Input Gates. Special modules were made for interfacing the Beam Profile Monitor and the LINAC resonator controllers. The CAMAC Crate Controller used in the system are equipped with a built-in single board computer having PC104 interface and Ethernet port. On power-up the CAMAC controllers boot from a central server, using the Linux Terminal Server software. The VME Crate controllers also have embedded PCs inside them with Ethernet interface. All of them are connected to the same Ethernet network.

Computers providing the user interface are equipped with four shaft encoder knobs, acting as incremental input devices, for setting the value of analog signals. They are

AN UPDATE ON CONSYS INCLUDING A NEW LABVIEW FPGA BASED LLRF SYSTEM

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Abstract

ConSys, the Windows based control system for ASTRID and ASTRID2, is now a mature system, having been in operation for more than 15 years. All the standard programs (Console, plots, data logging, control setting store/restore etc.) are fully general and are configured through a database or file. ConSys is a standard publisher/subscriber system, where all nodes can act both as client and server. One very strong feature is the easy ability to make virtual devices (devices which do not depend on hardware directly, but combine hardware parameters.)

For ASTRID2 a new LabVIEW based Low-Level RF system has been made. This system uses a National Instruments NI-PCIe 7852R DAQ card, which includes an on-board FPGA and is hosted in a standard PC. The fast (50 kHz) amplitude loop has been implemented on the FPGA, whereas the slower tuning and phase loops are implemented in the real-time system. An operator interface, including live plots from the regulation loops, are implemented in a host program on Windows. All three levels have been implemented with LabVIEW. The LLRF system is interfaced to ConSys through LabVIEW shared variables.

STATUS OF CONSYS

ConSys was originally made as a new control system for the storage ring ASTRID in 1998 [1-3]. It is now used at several machines at the University of Aarhus, which is including the new storage ring ASTRID2 [4] presently being commissioned. ConSys is also used at Stockholm University to control DESIREE and previously CRYRING as well.

The control system follows the standard model for a distributed control system using the publisher/subscriber method. It is running on Windows and written in Microsoft Visual C++ using MFC base classes. The design of the system is based on an object oriented programming strategy and the core system has been stable for many years. In ConSys the same core software is running on all computers - operator console PC's as well as frontend computers/device servers. Almost all configurable data are stored centrally in a SQL database: This includes all address information needed to locate devices and parameters, scaling data for conversion between binary and physical information, and display information used by a general purpose operator console application to generate operator pages for control and monitoring.

ConSys Devices

Data are collected and controlled on frontend computers through ConSys devices [1]. A large number of different hardware can be controlled and monitored by ConSys. Some hardware is controlled by dedicated devices where the device interfaces needed are coded directly into ConSys. Other equipment is controlled through analogue and digital I/O through general hardware. These kinds of hardware are serviced by standard ConSys devices where all configurable information is stored in the SQL database. At ASTRID we use home built equipment, as well as industrial systems. In the original control system all general control was done through home built so-called G64 systems – small CPU crates with general purpose analogue and digital control – including table based ramping of the machine. Most of these systems are still running today. Newer systems with need for general I/O are now based on Beckhoff PLC (Programmable Logical Controller) systems. PLC systems are relatively cheap, reliable and flexible systems for slow control and data acquisition. Simple automation codes are in some cases made directly in the PLC controller. Examples of programs implemented in PLC systems are: vacuum baking control, vacuum interlock/safety systems, personal safety system, undulator safety system and general averages of ADCs. All PLC systems are connected via Ethernet and serviced by a general ConSys PLC device for monitoring and control. As with our existing general devices all address and conversion information needed by ConSys to service the PLC's is stored in the central SQL database.

Another kind of general purpose I/O device is an interface device to LabVIEW shared/network variables. ConSys supports read and write of simple parameter types (Boolean, Word, Floating point) to shared variables. The shared variable names, location and data types are stored centrally in the SQL database. This device is used with NI CompactDAQ and CompactRIO systems as well as the LabVIEW based RF system presented later in this article.

A similar device is used to interface EPICS channels. The ConSys to EPICS channel interface is used for control and monitoring of the ASTRID2 beam position system, which is based on Libera Electron Beam Position Processors running an EPICS device.

Some hardware have embedded processors with control and monitoring through various interfaces. For this kind of hardware, specialized ConSys devices are implemented. The implementation is made so several instances of the same kind of hardware can be controlled by the same device code. This implies that all instance

PLC-BASED CONTROL SYSTEM FOR LINEAR ACCELERATOR (LCS) AT EBC KHARGHAR, BARC

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Abstract

Currently the 10MeV Linac is being used for different research and industrial applications. The control system in operation was developed using CAMAC based Data Acquisition System (DAS) and Hard-wired Interlock System. It is proposed to replace the CAMAC system with a state-of-the-art indigenously developed Programmable Logic Controller (PLC) that is verified to the level of a Class IB computer-based system used in nuclear power plants. A PLC node comprises of two VME bus based CPU boards (PowerPC MPC7447, 600MHz) working in redundant mode. The inputs and outputs are common to both CPUs. The I/O boards are hot swappable and intelligent. An intelligent Ethernet board is used for communication with a PC running the SCADA software and industry standard communication protocols drivers. The PLC hardware and software has undergone rigorous verification and validation. A user-friendly 'Application Development Environment' is provided to the process engineer for building the application using pre-defined function blocks. The LCS developed using PLC is to be used for operating the Linac irradiation facility, remotely as well as locally in a fail-safe mode, with sequential start-up and sequential shut-down. Apart from system status monitoring, data archiving, alarm generation and setpoint adjustments, it monitors the important parameters and trips the Gun Modulator High Voltage (GM HV), the Klystron Modulator High Voltage (KM HV) and the Electron Gun Power Supply (EG PS) on fault conditions.

INTRODUCTION TO LINAC [1]

The 10 MeV Linac Irradiation Facility consists of the RF Linac and conveyor system. It is housed in a two-storied building with 2.6 meters thick concrete shielding walls. The Linac structure with electron gun, RF cavity, gate valves, Sputter Ion Pumps (SIP), and beam transport line is at the first floor as shown in figure 1, whereas scan magnet, scan horn, titanium foil, SIP for scan horn and conveyor system for material handling is at ground floor. The Electron beam at 50 KeV is generated in electron gun

with LaB₆ cathode and injected into the on-axis coupled cavity Linac which accelerates the electrons to 10 MeV. A 2856 MHz, 6MW Klystron based RF Power source is used to establish the required electric field of 18 MV/m inside the Linac. After acceleration, the magnetic sweep scanner deflects the beam in the scan horn and is taken out to the atmosphere through a 100 cm X 7 cm X 50 μ m titanium foil exit window for irradiation jobs. The Linac up to titanium foil is maintained at 10^{-7} torr vacuum with the help of rotary-backed turbo molecular pump and sputter-ion pumps.

Linac can be operated in various modes like RF Conditioning Mode, Vacuum System Maintenance Mode, Beam Trial Mode and Job Irradiation Mode using the LCS.



Figure 1: 10- MeV LINAC.

SYSTEM REQUIREMENTS

The main function of the system is to trip the GM HV, the KM HV and the EG PS against unhealthy conditions of various digital and analog inputs. The system is also used by the operator for operating the subsystems of Linac during various modes of operation. Fail-safe operation, with sequential start-up, sequential shut-down and tripping of

*retired

STATUS OF THE ULTRA FAST TOMOGRAPHY EXPERIMENTS CONTROL AT ANKA

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Abstract

X-ray imaging permits to spatially resolve the 2D and 3D structure in materials and organisms, which is crucial for the understanding of their properties. Additional temporal resolution of structure evolution gives access to dynamics of processes and allows to understand functionality of devices and organisms with the goal to optimize technological processes. Such time-resolved dynamic analysis of micro-sized structures is now possible by aid of ultrafast tomography, as being developed at the TopoTomo beamline of the synchrotron light source ANKA.

At TopoTomo, the whole experimental workflow has been significantly improved in order to decrease the total duration of a tomography experiment down to the range of minutes. To meet these requirements, detectors and the computing infrastructure have been optimized, comprising a Tango-based control system for ultra fast tomography with a data throughput of several 100 MB/s. Multi-GPU based computing allows for high speed data processing by using a special reconstruction scheme. Furthermore the data management infrastructure will allow for a life cycle management of data sets accumulating several TByte/day.

The final concept will also be part of the IMAGE beamline, which is going to be installed in 2013.

INTRODUCTION

Third-generation light sources offer new possibilities for X-Ray imaging experiments. Fast imaging techniques became available, thanks to the high flux and to new fast CMOS detectors. One of the fields benefiting from is micro-tomography, where the speed-up is generating large data sets in a few seconds.

The reconstruction of these large 3D data sets was usually performed offline. Due to the reduced reconstruction time from initially several hours down to only a couple of seconds the reconstruction became part of the online data processing chain. For the TopoTomo beamline at ANKA [1, 2] a GPU-based ultrafast tomography framework (UFO) has been developed in order to merge all components of a tomographic scan into a homogenous workflow.

Remaining challenges concern the need for a high performant, but still reliable control system, embedded experimental workflow, a quick online rendering and visualization. The final evaluation is still done by commercial software. Last, but not least, for handling experimental data of up to several TByte/day, a data-and-life-cycle management has to be introduced.

CONTROL SYSTEM OF TOMOGRAPHY

At ANKA the different layers (hardware, control, user interface) of a beamline communicate via the Tango software bus [3] (see Fig. 1). All hardware components are realized as Tango servers. Also the SCADA System WinCC-OA (PVSS2) [4] for vacuum control, etc., can be regarded as a Tango server. The Tango client SPEC [5] and its easy-to-handle macro language is used as command-line scripting interface to adapt the beamline optics and auxiliary elements to the specific experimental needs.

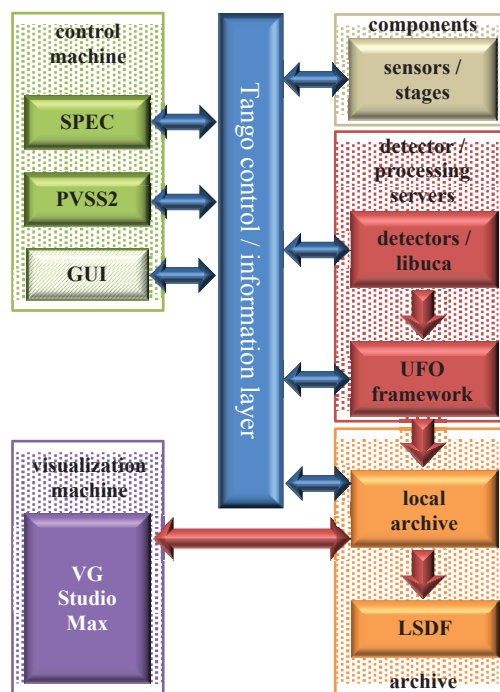


Figure 1: Communication (blue arrows) and dataflow (red arrows) between the different software layers and devices.

Instead of the slow overall-beamline control system, an optimization to reduce the total duration of a tomography experiment requires a significant improvement of the performance of all layers and of the IT infrastructure. For the software layer, the dead time (~ms) of a pure Tango-based software communication has to be replaced by hardware based triggering and the streaming of the data has to be designed carefully.

For the infrastructure of the TopoTomo beamline four servers (see Table 1) are involved in the workflow of a tomography scan. The different servers are connected to

HYPERARCHIVER: AN EVOLUTION OF EPICS CHANNEL ARCHIVER

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Abstract

Data storage is a primary issue in any research facility. In the EPICS middleware based accelerator community, Channel Archiver has been always considered the main reference. It works with Oracle and MySQL, probably the best well known relational databases. However, demanding requirements at minimum costs have fostered the development of a wide range of alternatives, like MDSPlus (Consorzio RFX), SciDB (BNL) or Hypertable (IFNF). This document launches a tool called HyperArchiver, which was firstly developed at IFNF (Italy) and eventually customised by ESS Bilbao (Spain). Based on a NoSQL database named Hypertable, it focuses on large data sets management with maximum scalability, reliability and performance. Besides the update and further customization made at ESS Bilbao, HyperArchiver is presented with a set of GUIs, in order to provide an easy use and integration with any general control system. A LabVIEW VI and two cross-platform PyQt GUIs for both Hypertable data retrieval and HyperArchiver control have been developed and successfully tested at ESS Bilbao (see Figures 1–3).

INTRODUCTION

Particle accelerators are very complex and expensive devices. Therefore a reliable distributed control system allowing easy maintenance and upgrading turns basic in this kind of facilities. EPICS (Experimental Physics and Industrial Control System) is a set of Open Source software tools and applications, which provides the infrastructure for distributed control systems. Many particle accelerator, large experiments and major telescopes facilities use it to build complex control systems made of tens or even hundred of computers, networked together to allow communication between them and provide control and feedback from different locations. In this context, data storage is a very important issue, not only as part of the control system itself, but also for the proper functioning and use of the accelerator and its experimental lines.

EPICS ARCHIVING TOOLS

The most standard EPICS standalone client for data archiving is called Channel Archiver [1], which is based on the relational databases MySQL and Oracle (therefore it is also called RDB Archiver). Unfortunately, they both have some well known drawbacks, which explain the efforts made towards the improvement of its performance and usability [2]. However, this has also fostered the development of a wide range of alternatives focused on high performance and large-scale dataset management, like MDSPlus,

SciDB (BNL) [3] or Hypertable (IFNF) [4]. In this work only the last one will be discussed, but it should be kept in mind that they are all possible solutions for the RDB Archiver limitations.

Channel Archive

The Channel Archiver is the standard archiving tool for EPICS. Using the EPICS Channel Access (CA) network protocol, it can collect real-time data from any CA server on the network. It stores the full data set offered by CA (values, timestamps, status information, engineering unit names and display, control and alarm limits), allowing scanning at a fixed period or on change.

Since its original design, the EPICS Channel Archiver has undertaken several significant transformations. The version publicly known as an EPICS extension [1] was developed at the Spallation Neutron Source (SNS), Los Alamos, USA. Its main feature is the usage of a relational database instead of the indexed files used by the original Channel Archiver [5]. This version of Channel Archiver supports both MySQL and Oracle RDB and is entirely written in Java as part of the Control System Studio (CSS). This tool significantly improves data access and retrieval, in comparison to the original indexed file. Nevertheless, both Oracle and MySQL have some disadvantages like the expensive costs of Oracle or the effective maximum table size in MySQL, which can become a great limitation considering that RDB Channel Archiver stores all samples in one single sample table.

HyperArchiver

HyperArchiver [6] is a modification of the Java RDB ArchiveEngine which uses Hypertable instead of MySQL or Oracle. It was developed at INFN/LNL in Legnaro (Italy) and customised at ESS Bilbao (ESS-B) afterwards. Hypertable is a non relational, high performance and distributed database released under GNU license, which focuses on management of large data sets with maximum scalability and reliability. HyperArchiver is actually a hybrid version, as samples (bulk data) are stored in Hypertable database, but the basic static data of EPICS PVs is still recorded in RDB Archiver's MySQL database. First tests at Brookhaven National Laboratory (BNL), USA, have already shown very good performance on data insertion and retrieval [7].

HYPERARCHIVER AT ESS BILBAO

HyperArchiver Customization

HyperArchiver version released at Legnaro was meant to be used with Hypertable 0.9.3.3, and had some proved

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EPICS MySQL ARCHIVER INTEGRATION BETWEEN EPICS AND MySQL

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Abstract

The performance evaluation and analysis of inter-system dependency of the various subsystems of the Superconducting Cyclotron (SCC) demand a well configured data logging, archiving and historic analysis facility for large number of control parameters along with on-line failure analysis facility of every system. Experimental Physics & Industrial Control System (EPICS) is used as development architecture of the control system of these systems with MySQL as database for large amount of relational data management. This combination requires integration between EPICS and MySQL server. For this purpose, MySQLArchiver as an EPICS Extension is developed for data logging and archiving of control parameters into MySQL database. This extension also provides a web based tool for online monitoring of control parameters and historic analysis of archived data. This paper describes the software architecture, implementation, as well as method of configuration for any other EPICS based control system as a utility. This facility is also elaborated with examples, web page views and experiences of deploying it in SCC.

INTRODUCTION

The performance of a particle accelerator is measured by its beam stability. The beam stability is achieved through fine tuning of the system parameters. The requirement of archiving the system parameters originates here. The Experimental Physics & Industrial Control System (EPICS), a standard open-source dual layer software tool for designing distributed control system, is widely used in large accelerators around the world for implementing supervisory control software. It has its own Channel Access (CA) archiver for storing system parameters into a proprietary database using channel access protocol. Since modern accelerators e.g. Superconducting cyclotron are comprised of various critical systems e.g. cryogenic system which are entirely vendor dependent. These systems have their own proprietary or third party supervisory system mostly without support for EPICS channel access. While fine tuning such accelerators with EPICS at supervisory control layer, EPICS channel archiver fails to store the third party system parameters. Again configuration and maintenance of the archiver demand expertise in EPICS tool set.

In contrast, interface to an open relational database e.g. MySQL, PostgreSQL etc. is more readily supported by most of the industry standard control software. The availability of expertise and support for these databases is plenty in industry. Hence an archiver based on such open relational database engine with channel access support

will mitigate the requirement of storing control parameters from heterogeneous systems (EPICS and non-EPICS/third party) in a common platform. An EPICS archiver is developed using MySQL as database engine for archiving and retrieving the control parameters of Superconducting Cyclotron (SCC), Kolkata. MySQL is chosen due to its simplicity for installation and maintenance.

SOFTWARE OVERVIEW

An archiver is a client tool, i.e. CA Client, from the perception of EPICS dual layer architecture. The main purpose of the archiver is to collect the control parameters using CA protocol from various Input Output Controllers (IOC) distributed over network and then it stores the values into a database. The user interface for retrieving the archived data for analysis purpose is also an integrated part of the archiver. The software architecture and other components of EPICS MySQL Archiver are described below.

Architecture

The software architecture of EPICS MySQL Archiver is shown in Fig.1. A multilayered architecture with a common memory resident database is adopted for this application.

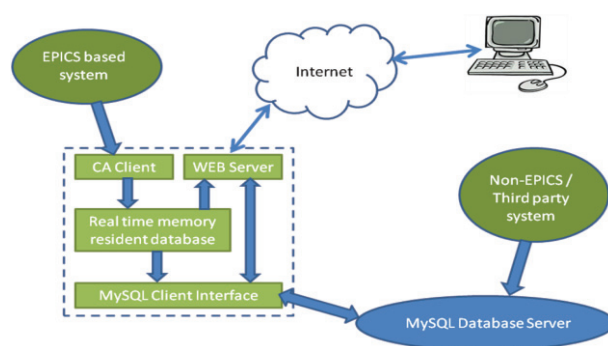


Figure1: Software architecture of EPICS MySQL Archiver.

The top layer of the software is consists of a CA Client interface and a Web server interface. The CA Client interface is dedicated for acquiring the values of the EPICS based parameters through CA link. The intermediate layer is a memory resident real time database (RT DB) keeping the latest values. The lowest layer is MySQL client layer dedicated for communicating with MySQL database server using SQL commands. This layer is responsible for archiving data from RT DB layer into database and also for retrieving archived data on demand. A web based user interface is provided through Web server interface. The user interface is equipped with tools for viewing system and subsystem wise online status of

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USING MEMCAHED AS REAL-TIME DATABASE IN THE SPARC CONTROL SYSTEM

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Abstract

The first implementation of the SPARC control system was based on a distributed TCP/IP data server: each front-end CPU had its own server to distribute data to the console. We decided to move the system to a NoSQL key value database. We decided to use an open source database Memcached. This is a database that is high performance key-value cache optimized for speed only. For this reason we could use memcached not for storing data, but as a channel of communication between front-end processors and consoles. The first object that we have installed is the camera system. We chose this class of elements because the amount of data is high; cameras are at least 640x480 with 8 bit. In this first installation we made some speed test: we increased the speed transfer and the data transfer is now independent from the number of high level CPUs that are using the same image. The success of this installation convinced us to bring the entire data transfer of SPARC control system to use Memcached as data server.

SPARC

The SPARC*[1] (Sorgente Pulsata e Amplificata di Radiazione Coerente, Self-Amplified Pulsed Coherent Radiation Source) (Fig.1) project is to promote an R&D activity oriented to the development of a high brightness photo injector to drive SASE-FEL experiments at 500 nm and higher harmonics generation. Proposed by the research institutions ENEA, INFN, CNR with collaboration of Università di Roma Tor Vergata and INFN-ST, it has been funded in 2003 by the Italian Government. The machine is installed at Laboratori Nazionali di Frascati (LNF-INFN). It is composed by an RF gun driven by a Ti:Sa laser to produce 10-ps flat top pulses on the photocathode, injecting into three SLAC accelerating and 6 undulator sections.

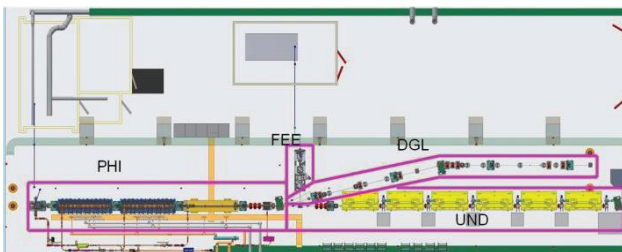


Figure 1: SPARC.

CONTROL SYSTEM DESCRIPTION

The control system should guarantee and simplify machine operation. In general the main operations in an accelerator control system are: data taking, display of information, analysis, command execution and storage. The simplest and functional control system has distributed processors on a classic three levels architecture (Fig. 2).

- *First level:* At this level we find the console with its human interface to allow the operator to control the machine, a logbook to share information within the collaboration, a database to store all information coming from the machine and a web tools to help the management of the control system and to share some information outside the collaboration;
- *Second level:* At this level we find the front-end CPU that executes commands and handle all the information about the status of the machine available at the first level. Meanwhile it automatically saves data from its various elements in two ways: on value changes and/or at fixed time intervals;
- *Third level:* This is the acquisition hardware where we find an appropriate acquisition board or the secondary field bus to acquire data from the real element.

The interconnection bus between the levels is a Gigabit Ethernet LAN.

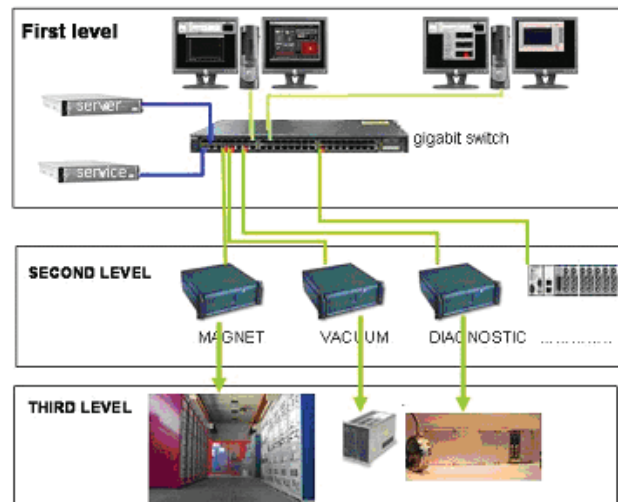


Figure 2: Control System Structure.

ELEMENTS

The control system allows to control all machine elements (from the Laser until undulator) and their diagnostic instruments.

* The SPARC project is financially supported by the EU Commission in the 6th FP, contract no. 011935 EUROFEL and contract no. RII3-CT-2003-506395 CARE

CONTROL SYSTEM INTEROPERABILITY, AN EXTREME CASE: MERGING DOOCS AND TINE

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Abstract

In controlling large facilities one is rarely able to manage all controllable elements via a common control system framework. When the standard framework must deal with numerous 'foreign' elements it is often worthwhile to adopt a new framework, rather than 'disguising' such components with a wrapper. The DOOCS[1] and TINE[2] control system frameworks fall into this scenario. Both systems have a device server oriented view, which made early mapping attempts (begun in 2000) immediately successful. Transparent communication, however, is but a small (albeit important) part of the control system merger currently taking place. Both systems have well-established central services (e.g. archiving and alarms), and possess a general 'culture' which might dictate to a large extent how something is actually 'done'. The long term goal of the DOOCS/TINE merger is to be able to make use of any tool, from either the DOOCS or TINE toolbox, on any control system element.

We report here on our progress to date, concentrating on the REGAE accelerator, and plans for the XFEL accelerator (to begin commissioning in 2015).

INTRODUCTION

'Interoperability' is a bit of a trendy word these days and it is important to be clear at the outset what we mean by 'control system interoperability'.

Any control system framework will likely provide interfaces to popular scientific and engineering software such as MatLab and LabView as well as popular user utilities such as Python, Java, .Net, and the like. If these interfaces are not native to the software in question then one speaks of 'interoperability' with regard to allowing the control system to interface ('interoperate') with such external software packages. In this paper, however, we refer to 'interoperability' as being that between the different control system frameworks themselves.

Since circa 1990 control system frameworks have been typically recognized by their names rather than, say, 'the control system they use at KEK'. Likewise there has been a strong tendency for institutes to adopt an existing controls framework, rather than 'inventing their own'. The most popular of these is EPICS[3]. There are nonetheless a large number of institutes which base accelerator control on something else, for example TANGO[4], ACS[5], STARS[6] or, our primary focus here, TINE[2] and DOOCS[1].

Consequently when the primary control system is not, for instance, EPICS it often occurs that, over the course of operations, some provision must be made to interface to exotic EPICS elements which invariably creep into the

system. This is in fact one of the primary motivations for pursuing interoperability. Experiments and test equipment from other facilities can suddenly introduce timelines, not to mention complexity, which necessitate seamless, rapid, and robust integration of foreign components into a control system. Epics2tine [7] is one of the first attempts to do this systematically. Since then, a number of translation interfaces and gateways such as tango2tine, epics2tango, etc. have been available.

In this vein, a doocs2tine translation layer was embedded directly into the DOOCS libraries in the year 2000. This constituted the primary step in the eventual control system merger now taking place.

Below we will first discuss what the interoperability between control system frameworks might mean in general and then give specific details concerning what it means to merge two relatively distinct control system frameworks. We note here that this goes far beyond the simple ability to 'trade data'.

CONTROL SYSTEM FRAMEWORK INTEROPERABILITY

There are in principal three ways to go concerning the interoperability between two distinct control system frameworks [8]. If System A refers to the primary control system framework, then each of these interoperability methods amounts to translating requests from System A into System B language, obtaining results, which are then translated back to System A language. This can be achieved by a stand-alone gateway process, by incorporating the translation layer directly within the System A client-side API, or by incorporating the translation layer within the System B server-side API. The relative merits of these approaches have been discussed before [8]. Solutions such as the Joint Controls Project (JCOP) [9], Control System Studio (CSS) [10], or java DOOCS Data Display (*jddd*) [11] focus on the second method listed above. We note here that the third method, server-side translation layers, being the most invasive is also the most demanding, as the introduction of any new software (the translation layer) on the front-end elements places these critical components at new risk. Nevertheless, it is precisely this third method which allows a control system merger to take place in the first place and is the key to the DOOCS/TINE merger we now describe below.

MERGING DOOCS AND TINE

Device Servers versus Databases

Control system frameworks have a general perspective concerning the accelerator control points. Some, such as,

TANGO FOR EXPERIMENT CONTROL

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Abstract

The Tango control system framework allows you to control an accelerator complex as well as single equipment. The framework contains the communication bus with the standard communication modes (synchronous, asynchronous, event driven) as well as the basic hardware access modules, GUI tools and development kits, bindings to commercial products (LabView, Matlab, IgorPro) and services (administration, archiving, access control) to set up a control system.

Tango was mainly developed by several synchrotron light sources that have to support not only the accelerator complex but also a lot of experimental end stations. For synchrotron experiments we have to control the whole process from basic hardware access over data taking to data analysis.

This paper describes in the first part the special features of Tango allowing flexible experiment control. The dynamic configuration, the rapid hardware interface development and the sequencing and scanning framework are some examples.

The second part gives an overview of some packages developed in the Tango community for experiment control: A HKL library for diffraction computation and diffractometer control, a library to control 2D detectors and a data analysis workbench with workflow engine for on-line and off-line data analysis. These packages are not part of Tango and can be used with other control systems.

TANGO BASICS

What is Tango?

Tango [1] is a control system tool kit developed by a community of institutes. It is object oriented with the concept of devices (objects) for each piece of hardware or software to be controlled. Tango classes are merged within operating system processes called Device Servers. Three types of communication between clients and servers are supported (synchronous, asynchronous and event driven).

But Tango is not only the software bus which handles the communication between device servers and clients. The Tango tool chain offers software from the hardware interface to the graphical user interface for several programming languages as shown in Table 1.

Tango utilities are available, with the basic installation, for code generation, device configuration and testing and for administration and survey of a whole Tango control system.

An archiving and a configuration snapshot system usable with Oracle or MySQL are also available.

Table 1: Available Tango Modules.

Module	Description
Core Libraries	Client/Server communication libraries for C++, Python and Java
Device Classes	About 300 hardware interface classes are available to download [2]
GUI Frameworks	Available for C++ and Python using QT, for Java using Swing and a web interface written in PHP
Client Bindings	LabView, Matlab and IgorPro
Tools	Pogo – Code generator for device classes in C++, Python and Java Jive – Configuration and testing tool Astor – Administration and survey of the Control system
Archiving	Archiving and snapshot system with GUIs and web interface. Usable with Oracle and MySQL
Alarm System	Event driven alarm service
Sardana	Framework for experiment control : Interface standardization, configuration, sequencing, command line interface

Rapid Interface Development

Important for flexible experiment control is a short development cycle to interface and integrate new hardware into the control system. Tango with its code generator (Pogo) offers a very comfortable way of implementing new hardware interfaces. The graphical interface builder allows the user to design the network interface and the main functionality (state machine, refreshing rate, memorization, etc.) of a device server.

The device server code can be generated in three programming languages: C++, Python and Java. The user has only to fill-in the code necessary to access the underlying hardware. For any change of the interface or for example the state machine, Pogo can be used to modify the existing code (Fig. 1).

Dynamic System Configuration

For experiment control systems distributed over several hosts it is very handy to have a centralised way to survey and to reconfigure running software. Tango offers such an administration system which is part of the core package. Two parts are necessary, the Starter server which is running on the distributed hosts and the graphical administration interface Astor (Fig. 1).

CONTROLS ARCHITECTURE FOR THE DIAGNOSTIC DEVICES AT THE EUROPEAN XFEL

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Abstract

The European XFEL X-ray laser is a 3.4-km-long facility, which runs essentially underground and comprises three sites above ground. It will begin on the DESY site in Hamburg, Germany and runs mostly below surface to the XFEL research site, which is to be erected south of the town of Schenefeld. First electron beam is expected in 2014 in the injector and in 2015 through out the whole facility. The XFEL will be an electron accelerator and its electron beam will be used to create intense photon beam in long undulator sections to be used in various research fields.

For controlling all diagnostic devices like a toroid, BPM or BLM, it is planned to use the new MTCA.4 crate standard instead of VME. ATCA is an emerging standard from the Telecom Industry and adapted with the PICMG MTCA.4 branch for physics usage. The communication on the backplane utilizes the high-speed serial PCIe communication plus precise clock lines and SATA interface. The MTCA.4 hardware supports hot-plug mechanism and remote monitoring and control via IPMI over Ethernet. Some of the diagnostics will be connected to 16Bit ADCs with up to 125Mhz sampling rate from Struck Company or to an internal DESY development call DAMC2. The software architecture is based on the DOOCS control system known from the FLASH accelerator. The raw data from the ADCs will be read via DMA transfer by one server process. Then this raw data will be distributed locally on the CPU using a message passing system based on the ØMQ project. The receiving server processes in order to calculate these data into engineering units. Everything works in an event driven way.

The current hardware and software concept will be presented.

INTRODUCTION

At FLASH over the last 15 years, VME systems have been used for all kinds of readout and control of fast diagnostics like BPM, toroid or wirescanner. The more then 30 years old VME standard has several drawbacks e.g. the parallel bus, no standardized crate management and it is relative expensive. So, it was considered to move to a more modern crate standard for the European XFEL [1] project. Since FLASH [2] is the "test bench" for XFEL, it was decided to install the same hardware and software for the FLASH2 extension and migrate slowly the old VME systems to the µTCA one.

Since 2002, the new Advanced Telecom Computing Architecture (ATCA) emerged on the market, which is based on PC technology and serial communication links.

In addition to ATCA, a smaller version of it, based on the ATCA mezzanine cards, called µTCA was defined. This standard was extended even further to MTCA.4 [3], formerly known as µTCA for Physics.

The reasons, why µTCA was chosen for the XFEL are the following:

- ∞ Modern standard based on common PC technology
- ∞ Fast serial communication via PCIe
- ∞ Standardized crate management via IPMI
- ∞ Hot Swap capability
- ∞ Capable of redundant crate layout
- ∞ More cost efficient then VME

DOOCS

The Distributed Object Oriented Control System DOOCS [4] is the leading system for the FLASH accelerator and chosen for the XFEL. DOOCS is a common client/server control system and based on an object-oriented approach at the front-end/server and client/display side. It is mainly implemented in C++, but there is now a Java client-side implementation available called jDOOCS, which is the communication interface for the new display tool jDDD [5]. An interface for MATLAB clients is provided. The communication protocol is based on ONC Remote Procedure Calls (RPC), but efforts are on the way to replace it by the TINE [6] protocol. The client interfaces of EPICS and TANGO are integrated.

µTCA HARDWARE

The µTCA crate is a 19" form factor frame to accommodate the AMC cards. There are already several versions of these crates on the market, which allow sliding in the AMCs in horizontal or vertical orientation. One may purchase simple desktop test crates or full-featured 19" versions with 12 slots with the possibility of redundant fans, power supplies, CPUs or MCHs.

MTCA.4

For the XFEL project, the standard is enhanced to host vertical orientated AMC boards with double height and the possibility to attach Rear Transition Modules (RTM). These RTMs are used to connect IO signals and to allow signal-conditioning circuitry. Compared to 6U VME boards, it offers about 30% more PCB space. The idea of this standard extension is to add features, which are required especially for industrial and physics applications, like precise clock distribution over the backplane. This standard is called MTCA.4 and defined by the PICMG organization in 2011.

PC BASED REAL TIME DATA EXCHANGE ON 10GbE OPTICAL NETWORK USING RTOS *

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Abstract

The traditional embedded systems are expensive to adapt to the new requirements. The Personal Computer based systems offer alternatives for industrial controls. It reduces the capital cost and provides a solution for multiple applications. However, limitations of PC based controls should be resolved. PC operates on a non-real time OS with non-deterministic response to real time events and data. The real-time pre-emptive kernel for Linux uses Xenomai for better solution. A real-time 10GbE data exchange optical network using Xenomai extension for Linux is demonstrated. The hardware based on Intel_82599 10GbE Ethernet PCIe network card supports IEEE1588 standard for synchronization, deterministic response to real-time interrupts and events.

The benchmark testing comprises nodes and data sources, for data exchange among nodes, which would improve the performance of PC control systems. Data sources and consumers include time synchronization, hardware and software events broadcasting. A single network cable is used for exchange of status and control data among nodes. Moreover, the open source Ubuntu Linux RTOS will help the future development.

INTRODUCTION

Industrial control systems are evolving from dedicated systems to generalized and flexible systems. Traditional controls were designed around dedicated embedded system, wherein the design was applicable for a given set of control parameter and process. These systems would need major changes for new set of control parameters, computations and processes. The personal computer based controls offer better computational power, flexible and faster systems, via Ethernet [1]. The complex scientific experiments, [2] require more computational power and better controls [3]. Multiple applications and wider communication support on PC could offer cost-effective solution for real-time network.

Implementation of PC based industrial control system encounters many limitations [1, 2]. PCs were basically designed for applications with non-real time responses. Operating Systems (OS) for PC do not exhibit deterministic response to real time events and data [4]. Most of the common OS are not pre-emptive. However, as per [4], Xenomai kernel for Linux OS is a better pre-emptive kernel, which provides deterministic real time response. Xenomai is an alternative to the proprietary real time operating system, because it extends GNU/Linux with real time performance [5].

The pre-emptive kernel needs a better support from the system hardware, so that hard-real time interrupts are serviced within a given time-frame. PC based controllers require networked nodes for data acquisition, event monitoring and control.

With the advent of 10GbE Ethernet controller cards, it is now feasible to setup a multi-node network with reasonable throughput and latency performances [6]. Ethernet controllers such as 82599 and X540-T2 are now available from Intel, with Linux drivers. Hard-real time network are possible with Ethernet controllers [6], due to faster PCI express interface. The fast PCIe 2.0 interface on a PC ensures faster response from host CPU. The 10GBASE-T converged network adapter from Intel such as X540-T2, offers advantages of low latency, load balancing on multiple CPUs, MSI-X support and flexible I/O virtualization.

The real-time data exchange needs reliable time synchronization. In particular, a hard real-time network needs synchronized time stamping on data packets. Intel's controller support IEEE1588 Precision Time Protocol (PTP). Time synchronization is achieved with accurate time reference from GPS connectivity.

According to the above facts, network adapters for optical cable (X-520-SR2), as well as for Cat6A copper cable (X540-T2) were used to create 10GbE network, running on Linux with Xenomai real time framework.

An experimental real-time network is demonstrated for benchmark testing of 10 GbE network using Linux RTOS. Standard network performance test utilities such as Netperf, Iperf and Jperf were used for the benchmarking. Tests were performed both for TCP and UDP data exchange.

REAL TIME DATA EXCHANGE

The real time data exchange require pre-emptive kernel with deterministic response time. There are two open source real time extensions for Linux namely RTAI and Xenomai. However, Xenomai is being updated by the open source community. The comparative study [2] of VxWorks, RTAI and Xenomai indicates that performance of Xenomai is acceptable for most applications. It is necessary to apply ADEOS patch for Xenomai. We have used standard open source patches available for Xenomai kernel. For the present testing, the interrupts priority was ensured with minimum external devices connected to the CPU. The main objective is the basic setup of real time network using 10GbE network card, wherein the PC is used exclusively for the benchmark testing.

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MASTER SLAVE TOPOLOGY BASED, REMOTELY OPERATED, PRECISION X-RAY BEAM PROFILER AND PLACEMENT SYSTEM FOR HIGH PRESSURE PHYSICS EXPERIMENT AT INDUS-2 BEAM LINE

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Abstract

RRCAT has commissioned a beam-line on Indus-2 synchrotron facility for carrying out Angle Dispersive X-ray Diffraction Measurement. A typical high pressure measurement is carried out by placing the sample in the Diamond Anvil Cell (DAC) with the sample located in a region of beam diameter within 50-100 μm . The X-Ray beam has to pass through the DAC to ensure maximum illumination of the sample with the X-Rays. An X-Y beam scanner/locator cum placement system is developed, which scans an area of $10 \times 10 \text{ mm}^2$ with resolution of 10 to 100 μm in rough scan mode and fine scans selected area with programmable resolution of 2.5 to 25 μm . The scanner acts as slave to the PC in which master GUI grabs the data on serial port and plots the image of X-ray beam. It also analyses and detects the coordinate with maximum intensity. Thus the DAC can be placed at the desired location with an accuracy of 2.5 μm anywhere within $10 \times 10 \text{ mm}^2$, for performing experiment. Developed system takes only ~ 5 minutes to search the beam and a few seconds to place DAC at any the desired location within the scanned area.

INTRODUCTION

RRCAT has commissioned beam-line (BL-12) on Indus-2 synchrotron facility to carry out Angle Dispersive X-ray Diffraction (ADXRD) measurements. Since its commissioning, this beam-line has been used by various researchers, however, for its wider utilization; it is upgraded to perform measurements at high pressures using Angle Dispersive geometry. High pressure XRD measurements are extremely important to determine the structural properties of materials under extreme condition and provide information about the bulk modulus, stable phases etc. It is carried out by placing the sample in the Diamond Anvil Cell (DAC) that has a very small sample volume with a cross-sectional circular opening area of ~ 150 micros. Alignment of the incoming X-Ray beam from the beam-line with sample in DAC to ensure maximum illumination of the sample is thus a challenging task. Further, as the X-Rays are ionizing radiations and the exposure to the user needs to be essentially avoided, the alignment needs to be carried out in a shielded environment using a remote controlled system. To accomplish the above tasks, a master slave topology

based remotely operated precision beam locator cum placement system and interactive control software to measure beam size was developed.

The DAC is mounted on a two axes translation stage, with motion in a plane perpendicular to the X-Ray, and an X-ray sensitive detector is placed behind the cell. The software guides the DAC through a matrix of user selected points and the detector, gives the X-Ray intensity through the DAC as a function of its X & Y position. These data are presented in image format, which can be displayed in various shades of color. The optimum position of the DAC is determined as the co-ordinates where the transmission of X-Rays through the DAC is the maximum.

SYSTEM DESIGN PHILOSOPHY

- ADXRD beam line of Indus-2 has been used by various researchers may or may not be software conversant. Keeping this point in mind, GUI based robust software have been designed and developed, which is self-explanatory and has capability to guide even a beginner. To fulfill this, in software design, elaborate error handling has been incorporated.
- The instrument uses indigenous components like XY motorized translation stages manufactured in India and its fast driver and controller have been developed in-house at RRCAT.
- Keeping current and future software trend in mind it was decided that software must operate on future Windows platform (64 bit) instead of currently used Win XP.

SOFTWARE

The GUI based software is named **Lakshya**, functions as master and is developed using Vb.Net. XY translation stage control and data acquisition unit based on micro controller and its software is developed in assembly language, which functions as a slave unit of **Lakshya**. All the settings of XY translation stage and data acquisition module are done in master's GUI and final user approved settings are only transmitted to slave for execution. Current software uses $10 \times 10 \text{ mm}^2$ area to locate x-ray beam. Keeping future need and different applications in

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A FLEXIBLE AND TESTABLE SOFTWARE ARCHITECTURE: APPLYING PRESENTER FIRST TO A DEVICE SERVER FOR THE DOOCS ACCELERATOR CONTROL SYSTEM OF THE EUROPEAN XFEL

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Abstract

Presenter First (PF) uses a variant of Model View Presenter design pattern to add implementation flexibility and to improve testability of complex event-driven applications. It has been introduced in the context of GUI applications, but can easily be adapted to server applications. This paper describes how Presenter First methodology is used to develop a device server for the Programmable Logic Controls (PLC) of the European XFEL undulator systems, which are Windows PCs running PLC software from Beckhoff. The server implements a ZeroMQ message interface to the PLC allowing the DOOCS accelerator control system of the European XFEL to exchange data with the PLC by sending messages over the network. Our challenge is to develop a well-tested device server with a flexible architecture that allows integrating the server into other accelerator control systems like EPICS.

TECHNICAL BACKGROUND

The European X-Ray Free-Electron Laser (XFEL) Facility will use three ~200m long undulator systems to produce laser light by the Self Amplified Spontaneous Emission (SASE) process [1]. The photon energy can be varied by a change of the undulator gap. The corresponding motion control is implemented with Beckhoff TwinCAT PLC software on Windows PCs.

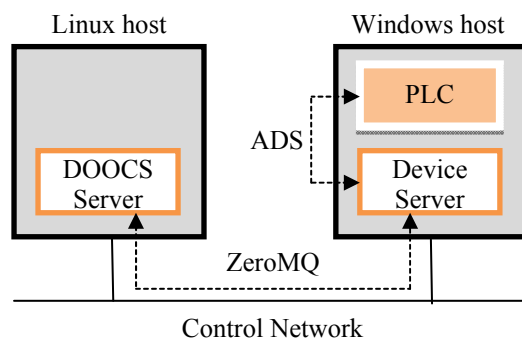


Figure 1: Integration of undulator control into DOOCS.

Figure 1 shows how undulator control is integrated into the Distributed Object-Oriented Control System (DOOCS), which is the accelerator control system of the European XFEL facility [2]. The DOOCS Server, running on a Linux host, defines for the undulator system a set of properties, such as the undulator gap. These properties can be read or modified by DOOCS client applications (not shown in the figure) in order to control the undulator system. The DOOCS Server exchanges the property

values with the Device Server using the ZeroMQ message transport library [3]. The Device Server runs on a Windows host together with the PLC of the undulator system. Both exchange the property values using the Beckhoff Automation Device Specification (ADS) protocol.

The reason for having two servers is that ADS is supported only for Windows platforms and the DOOCS Server is supported only for Linux platforms. The message interface between both servers crosses this platform border. An additional benefit of the message interface is that it adds flexibility on the machine control side. Anything may connect to the Device Server, regardless of the platform it runs on, as long as it is able to generate appropriate messages. It could for example be an EPICS Channel Access Server (CAS) with only little effort to implement the message interface.

DESCRIPTION OF PRESENTER FIRST

So, how does Presenter First help in developing the Device Server application? Presenter First proposes a pattern for structuring the code in a specific way, and a process for developing the application in a specific sequence [4]. The pattern improves testability of the code and offers some flexibility regarding the interaction with the environment. The process saves effort by developing on the basis of the intended behaviour of the application.

The Pattern

Applications are implemented using a variant of the Model View Presenter (MVP) pattern, as shown in Fig. 2.

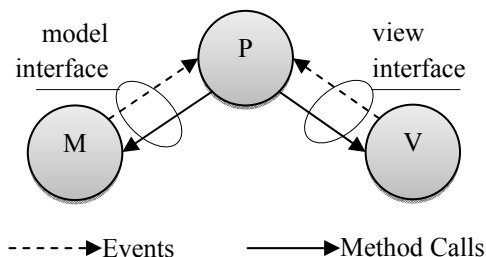


Figure 2: MVP variant used in PF.

The presenter represents the behaviour of the application that is defined by the functional requirements, the model manages the application data and logic, and the view interacts with the environment. Model and view do not communicate directly with each other because this would limit flexibility; instead both communicate with the presenter over clearly defined interfaces. They send events to the presenter to trigger some behaviour, which

DESIGN, DEVELOPMENT AND ANALYSIS OF A COMPREHENSIVE OPEN SOURCE SYSTEM FOR PROACTIVE MANAGEMENT OF SECURITY ASPECTS OF A CONTROL NETWORK

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Abstract

Control networks can only be assumed to be secure, when they work in complete isolation and all communication ports of the constituent control devices are disabled and are closely monitored for security breaches on 24X7 basis. With more and more control systems being developed using Common Out of The Shelf (COTS) computers, using windows OS, the chances of virus attacks on such control networks is extremely large. Handling zero day virus attacks or virus attacks with unknown cure, is a serious challenge for control network administrators. Another important aspect, somehow related to the security of the control network, is the rising temperatures of the control devices, because of 24X7 operation. All this is difficult to handle manually or using disconnected systems and hence there is a requirement of a comprehensive system which can do all this automatically. In this paper we will discuss the various security related parameters of the control networks and then present a simplified design followed by development details of a comprehensive open source system for proactive management of the security aspects of the control network.

INTRODUCTION

Modern day control networks are large and connected to Internet. They have distributed architecture and contain control, information & resource sharing related network components. COTS computers with Windows Operating System (OS) are used widely in large control networks with distributed architectures. Generally Windows OS based systems are prone to malware attacks. Due to this and the proximity of Internet to such networks, the security issues in such networks are numerous. Managing all these issues proactively and cost effectively is a huge challenge [1], but solutions in the form of numerous Free Open Source Software (FOSS) tools exist.

Out of numerous challenges in securing advanced distributed architecture [2], [3] control networks, proactive management of a) zero day malware attack and b) the overheating of control network components in distributed networks are important. The security concern about malware infected PCs on a network, is very serious, in control networks, since it sometimes causes transfer of control of the systems to some third party on Internet. The not so old “stuxnet” [4] and “duqu” menace are striking examples. The second security cum safety concern is the overheating of switching and server components, due to

long continuous operations, in large distributed control networks. The situation caused by non working network communication channels and servers, due to overheating, in a control network can cause serious operational issues.

In this paper, we carry out risk analysis of a modern day Distributed Architecture Control Network (DACN) and then identify the areas for proactive management of its security aspects. We present a comprehensive approach to implement a secure DACN [5] using the various FOSS tools. This is followed by the design and development details of our in-house solutions, conceived, for addressing the above mentioned security concerns [6]. The detailed security analysis of the proposed comprehensive approach has been carried out and presented in the paper.

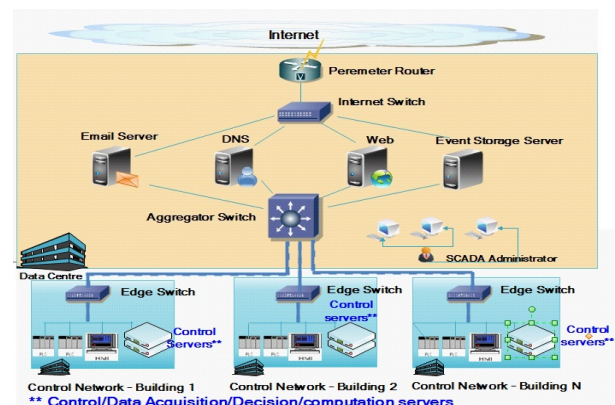


Figure 1: Distributed Architecture Control Network.

TYPICAL DACN

Figure 1 depicts the block diagram of a typical DACN which has the following salient features:

- Uses COTS PC, with windows OS, for computation and decision making.
- Uses Ethernet Technology with wide usage of Quality of Service (QoS) feature for real time communication with other systems.
- Uses modern communication servers like name, email and web for publishing information, thus is connected to Internet in some form or the other.
- Has some data acquisition and control hardware.
- Has some alarm generation system in place.
- Has a storage system for storing events.
- Has redundancy for Computation, Decision making, Communication and Data acquisition & Control.

WHAT IT TAKES TO MAKE A SYSTEM RELIABLE

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Abstract

What is a reliable system and how is reliability defined? This depends on the actual situation and in which environment the system is operated. If you can rely on a scheduled downtime of the controlled system every week, reliability is defined in hours or weeks. In this case the system must run just longer than the scheduled downtime. If the system has to continuously operate for months and even years, your requirements are rising. In cases where continuous operations must be guaranteed even during software or hardware updates, redundant systems come into play. The hardware selection process is driven by basic requirements like 'no moving parts' or 'redundant power supplies'. This implies the selection of possible (fan-less) CPU boards with passive cooling. It also implies no hard discs and reduces therefore the selection of possible operating systems. Continuous operation during updates requires redundant controllers/ CPUs also in addition to redundant power supplies. The latter has a lot of impact on the software running inside the controllers. We will describe the selection process of the components we have chosen and summarize our experience of several years of operations.

REQUIREMENTS

The requirements for process controllers in cryogenic systems are extremely high. Cryogenic systems have to run 24/7 in periods lasting for a year or more. A downtime of the control system will typically cause a downtime of the cryogenic plant of two to four hours to recover cryogenic operations. This does not take into account the systems being fed with liquid helium or the accelerator operations depending on the helium supply.

For the new European XFEL the situation will be even more extreme. The cold compressors of the cryogenic plant are extremely sensitive to distortions of any kind. Any unstable environment will cause an immediate shutdown of the cold compressors. The recovery time is expected to be between twelve and twenty hours at least. Stable process controls have an even higher priority.

POSSIBLE APPROACHES

How can these necessary uptimes be achieved? At DESY we have gained a lot of experience with commercial process control systems. They have the advantage to be supported by a company and should expectedly be reliable. The disadvantage being that they provide a closed environment. No 'special' functions which are necessary for cryogenic controls can be easily integrated. As an example cryogenic temperatures need dedicated calibration curves of a 5th to 7th grade polynomial. There's no easy way to these running in a commercial environment. Another example are

dependencies on the operating system, if not on the frontend controllers then at least on the operator screens. Security updates on the Windows operating system may cause problems in the operator's programs or the commercial software may define the time of system updates or hardware changes while the rest of the Window systems run on a different upgrade pace.

Using PLCs

PLCs may be a solution to reach stability. Predictive continuous processing speeds for all processing blocks in a PLC ensure stability in this respect. Thus PLCs are ideal candidates for machine protection systems. Full process controls on PLCs have certain limitations in processing functionality (see temperature calibration) and transparent data exchange with the operator interface. By default the PLCs do not support transparent data exchange for each and every property of the processing blocks. Each possible connection must be explicitly configured.

Redundancy in PLC controls is partly available but the selection of possible candidates is limited.

Using embedded (real-time) Systems

There is a lot of experience at DESY using embedded real-time systems for process controls. We are using vxWorks on the front end processors and EPICS as the process control system. This combination is typically used for machine controls. At DESY we added and/ or improved the processing block in EPICS to make them process control ready. EPICS comes with transparent access to all properties of the processing blocks. No specific configuration is necessary to gain access to these properties. This is a big advantage over PLCs. On the other hand EPICS did not come with redundancy support.

Redundancy

Redundancy is an important feature when 24/7 operations shall be guaranteed over periods of more than a year. Hardware problems on the processor, on I/O boards or on the control system Ethernet may cause system failures. These hardware problems can be overcome by adding a second processor running the same process database and sequence program in parallel. In case of a failure the second processor will take over without shutting down the controlled cryogenic plant. This kind of redundancy support has been added to the EPICS based control system. This kind of setup shall also help during software updates in the future.

PROCESSORS

We started with VME processors when we started using EPICS at DESY. This was the initial platform for EPICS IOCs. The disadvantage of VME is that a complete VME crate is necessary for a single CPU. And

PLC CONTROLLED SEARCH & SECURE SAFETY INTERLOCK SYSTEM FOR ACCELERATOR

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Abstract

A PCVM type 3MeV DC Electron beam accelerator has been developed at Electron Beam Centre, BARC, Mumbai, India. A PLC assisted search and secure system has been designed, developed and installed as the human safety system for radiation protection in the accelerator area.

INTRODUCTION

The electron beam accelerator has various subsystems. All the subsystems have to work together in a pre-defined sequence to generate the desired accelerated electron beam from the accelerator. All the subsystem such as vacuum system, sweep scan magnet unit, high voltage unit, chiller water unit, air circulation unit, search-secure, safety interlock unit, steering/focussing magnet unit has to be controlled. Each group of similar units has been provided with a PLC controller in order to perform the fully automatic operation of that subsystem. Finally all the PLCs are connected together on Modbus TCP-IP network to achieve a single point control of the accelerator. A touch screen panel has been provided at the control panel as an institutive user interface.

SYSTEM OPERATION

The 3 MeV electron beam accelerator is an industrial accelerator developed for the various industrial electron beam processing applications. The accelerator generates high dose X-ray radiation as by product when operational. The Accelerator is placed inside a hall made of thick concrete walls. The accelerator hall is called as the cell area. All the power supplies and other support systems are placed outside the cell area. Cables and electrical connections from the accelerator to the power supplies are made through S bands holes created in the walls of the cell. Since the accelerator generates large amount of radiation, which is actually a required feature for the irradiation but at the same time all the human being working in that region has to be protected against the radiation. The cell area needs to be fully evacuated for any human presence before starting the accelerator. A PLC based search and secure system has been installed to ensure all the regions of the cell area has been thoroughly checked for human occupancy and there is no human present before we can start the accelerator. The whole search and secure operations is carefully designed to check each and every corner of the cell area. Besides this the system provides an option of emergency shutdown of the accelerator. The emergency switch off button has been provided at various locations in the cell area. If a person is

trapped then he can press the emergency button and the high voltage in the accelerator will switch off immediately and source of radiation will cease off.

The cell area has one shutter and one entry/exit door. Before starting the search operation the shutter is closed and its status is monitored using a limit switch. The Entry/exit door has been provided with a mechanically close but electrically locks type of door lock. The door lock also provides the door open/close feedback signal for interlock purpose. The door lock operates automatically and controls the entry of any new visitor before the search operation starts. In order to locate any visitor or operator inside the cell search operation is performed. Seven no of search and secure units have been installed at carefully selected locations inside/outside the cell area. Each of this unit consists of two button and two indicators. Green Button as 'secure' (it is to be pressed during search operation), Red button as 'Emergency OFF' (It is to be pressed by the person trapped inside the cell to switch off the accelerator), 'Search ON' indicator indicates that the unit is active and 'secure' button can be pressed. If the secure button is pressed, the second indicator indicating 'Secure' will turn on indicating the unit is secured. Performing the 'secure' operation on these field units ensures the operator who is performing the search and secure operation physically goes to the location where the unit is located and ensures that he has personally ensured that nobody is present in that region.

All the seven Search & Secure field units are connected to the PLC controller unit for control and monitoring. The limit switch to sense the shutter close and electrically lockable lock and a hooter is also connected to the controller unit. Before the search operation starts, the shutter is closed in order to stop any new visitor entry. The Search & Secure (S&S1) unit get power automatically when the shutter closer switch turns ON. The operator will secure the unit S&S1. This operation also starts a hooter for 20seconds inside the cell to indicate the search operation has started so that if anybody present in the cell can move out. Securing the S&S1 will unlock the door for 10 seconds so that the operator can go inside the door and close the door. The door gets automatically locked after 10seconds. This closure disables any new entry. After the door is closed S&S2 unit gets the power from the PLC. The operator secures the unit S&S2, unit S&S3 gets the power from PLC and so on. After all the six S&S units have been secured the door gets unlocked for 20 seconds so that the person performing the search operation can come out of the cell area. The operator clears the S&S7 in order to finish the

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MACHINE THROUGHPUT IMPROVEMENT ACHIEVED USING INNOVATIVE CONTROL TECHNIQUE

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Abstract

In any type of fully or semi automatic machine the control systems plays an important role. The control system on the one hand has to consider the human psychology, intelligence requirement for an operator, and attention needed from him. On the other hand the complexity of the control has also to be understood well before designing a control system that can be handled comfortably and safely by the operator. As far as the user experience/comfort is concerned the design of control system GUI is vital. Considering these two aspects related to the user of the machine it is evident that the control system design is very important because it is has to accommodate the human behaviour and skill sets required/available as well as the capability of the machine under the control of the control system. An intelligently designed control system can enhance the productivity of the machine.

INTRODUCTION

The control system has been developed for subsystems of three different electrical machines. The present work describes how the throughput of a machine can be enhanced by innovative control system design.

SYSTEM OPERATION

Control system for three different types of electrical machines has been designed/ developed and installed. Following is the description of the machine productivity improvement by control system design:

1] Beam utilisation factor improvement from 50% to 98% by modulating the speed of the convey system: A 10MeV, Electron beam, RF Linac is operational at EBC, Kharghar, Navi Mumbai. The beam output scans one meter length in a scan horn. The product under irradiation is placed below the beam horn on a conveyor trolley. The trolley is one meter long and there is one meter gap between each of the trolley. With the highest possible (limited by trolley track conditions and angle of turn since the trolley follows the zigzag path) constant speed of 5mtrs/min operation of the trolleys, the beam utilization by the product kept in trolley will be 50% since same amount of the beam falls in the gap between the trolleys. We have modulated the speed of the trolley. The trolley speed is reduced from 5mtrs. /min to 0.1mtrs/min when it is under the beam otherwise when the beam falls between the trolleys the conveyor speed is kept at 5mtrs. / min. This speed modulation operation is performed by sensing

the arrival and departure of the trolley using a limit switch which is activated by the base of the trolley. Using this method the beam utilization for the irradiation goes up to 98% from 50% hence 48% rise in productivity.

2] Productivity improvement of the Electromagnetic machining facility: APPD/BARC has developed a 20kV 10KJ Electromagnetic machining (EMM) facility. In this EMM facility a large value capacitor is charged by a DC supply to a set voltage. This charged capacitor is then quickly discharged using triggered spark gap into a coil to generate an intense magnetic field. This magnetic field generates the eddy current into the job piece to do the mechanical forming. We have developed and installed a PLC based control system to control the EMM machine. We used to charge the capacitor bank manually before the control system was installed. A DC voltage source made using motorised variac was being used for the capacitor charging. When the voltage is set the capacitor takes time equal to five RC times constant by charging the capacitor exponentially to charge to the set input voltage.

With the implementation of PLC based control system in the EMM facility the capacitor voltage has been conditioned /isolated and fed to the PLC. When the operation starts the PLC sets the double voltage as the charging voltage to the capacitor bank and trip voltage as the capacitor voltage desired. When the power is switched ON the capacitor starts charging very fast since the input voltage is two times to that of the desired voltage. As soon as the desired voltage on the capacitor bank is reached the control system isolates the charging supply to the capacitor bank. This technique reduces the total charging time to 1/7th to that of the earlier technique. Since the EMM facility is an industrial production machine, the productivity is a direct function of the capacitor charging time. Hence it can be stated that the total throughput of the EMM machine can be enhanced by 700%.

CONCLUSION

The control system has been commissioned and it is working satisfactorily. The capacitor charging time has been reduced but the full utilisation of this reduced time can only be done when the job piece under machining is loaded on the machine using automatic feeding system.

ACKNOWLEDGMENT

We gratefully acknowledge the technical support offered by the developer team of the EMM facility/ accelerator design team in making us understand the machine operation and the control process. This has helped us a lot in the development, commissioning and operation of the control system.

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DESIGN AND ANALYSIS OF SECOND HARMONIC MODULATOR FOR DC CURRENT TRANSFORMER

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Abstract

DC Current Transformers (DCCT) are widely used in particle accelerators. DCCT is a device which produces even harmonics, predominantly second harmonics corresponding to DC beam current flowing through two toroids. The second harmonics is detected by digital synchronous detector implemented in programmable logic. Current proportional to the detected second harmonic is passed through the toroids in a feedback loop such that the flux due to the DC beam current is cancelled by it. This feedback current is the measure of average beam current. The high permeability toroid's, excitation and output windings are collectively called magnetic modulator, which is a key component of DCCT. Design and analysis of a second-harmonic magnetic modulator used as a detector for DC Current transformer for high resolution current measurement is presented.

INTRODUCTION

Ion current in a particle accelerator is a key performance measurement parameter. Based on the requirement of a particular experiment various configurations of the particle beam are required, thus the characteristics of the beam are different for these configurations. In order to have a measure of performance the average beam current forms a useful parameter for measurement. DCCT is non-destructive current measuring instrument in particle accelerators which can be calibrated. We have been involved in a project of technology development for Accelerator Driver Subcritical Systems [1] and as a part of development of high resolution DCCT, a second harmonic magnetic modulator for DCCT was designed and implemented. The following sections describe principles of second harmonic magnetic modulator. Processing algorithm was implemented in programmable logic. Experimental results of the magnetic modulator in a feedback loop have also been presented.

SECOND HARMONIC MODULATOR

A second harmonic magnetic modulator in its simplest configuration consists of a single high permeability toroid core with excitation and output winding. The particle beam current through the core is considered as input signal. If the toroid is excited to saturation by an anti-symmetric waveform, the resulting magnetic flux and hence the signal induce in the output windings contains fundamental and odd harmonics of the excitation frequency. When a dc current is passed through the toroid, even harmonic contents also appear in the output.

The main disadvantage of this configuration is the presence of large amount of odd-harmonics in the output. These odd-harmonics are comparatively much larger than the second harmonics and there is a probability of overloading the succeeding stages of electronics. So double core modulators are normally used for this applications as shown in Fig. 1. Two identical cores arranged in an opposition manner so that the odd harmonics would cancel each other. Ideally, output V_d will be zero if there is no input current, provided the cores are matched. In presence of input signal even harmonic components appear in the output and when the input signal changes sign V_d undergoes a phase reversal. But in practical conditions, imperfections in core matching and the presence of even harmonics in excitation signal causes zero error in all types of magnetic modulators. The earth's magnetic field and any other stray fields, thermal e.m.f.s in circuit connections are the other causes of zero error and drift. The zero error caused by memory effects should be removed by proper demagnetization [2]. Either the peak value or second harmonic component of the output can be a measure of input signal. One of the advantages of second harmonic detection over the peak detection method is that, the succeeding amplifier gain can be more as the amplifiers are not loaded by other harmonic components [3]. Toroidal cores are the most critical components of the modulator. Magnetic properties of these cores are the main factors which determine the resolution and the zero stability of the instrument.

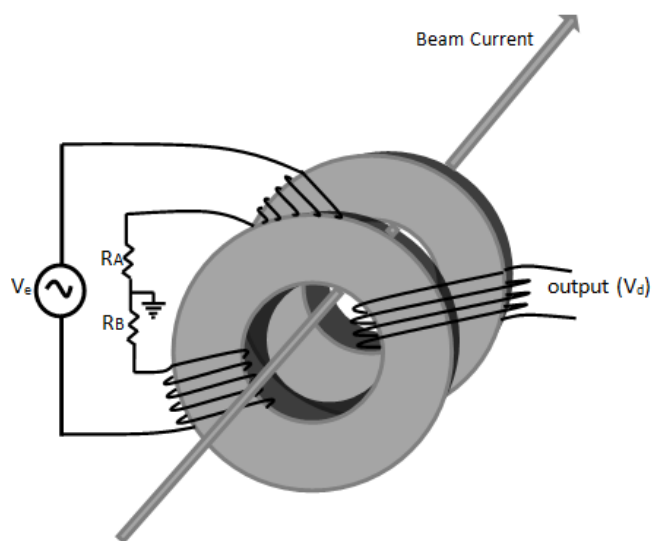


Figure 1: Schematic of second harmonic magnetic modulator.

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FLOGBOOK: FROM CONCEPT TO REALIZATION

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Abstract

Indus-1 and Indus-2, the Synchrotron Radiation Source (SRS) facilities at RRCAT Indore are national facilities and being operated on round the clock basis to provide synchrotron radiations to users as well as carrying out machine studies. Both of these accelerators are widely distributed systems and employ many sub systems for their operation. These sub systems are also made up of heterogeneous type of hardware and software modules. Indus-2 Control System is presently controlling approximately 10,000 input/output parameters for its operation. To keep the whole system up and running the faults & failures encountered during machine operations are attended at site and all observations and rectifications information are to be recorded electronically by the crewmembers. FLogbook has been conceived & developed to meet such needs. This web based software operates in the intranet environment over three tier software architecture. It mainly uses JavaServer Pages (JSP), JavaBeans and SQL databases for designing its building blocks. Using relational database features have been provided in the package for logging, e-mailing, searching & commenting the faults of various sub systems. Recently we have deployed the FLogbook in the field and machine operation crewmembers have been asked to use it as & when required.

INTRODUCTION

The main motivation of this software is to constantly monitor and improve the performance of Indus-1 & Indus-2 accelerators.

Indus-1 & Indus-2 are big & complex machines and involves various types of hardware and software for running it smoothly at round the clock basis. Seeing the complexities of various parts of both accelerators, it was felt to have a system that would systematically record the fault & failure information of accelerators encountered during its operations. This information would be recorded by accelerators crewmembers.

REQUIREMENTS

Based upon the previous experiences and feedback received from various system experts following basic requirements were considered before developing the FLogbook:

- (1) It should be possible to use the FLogbook by multiple users simultaneously connected over campus network.

- (2) The FLogbook should be easy to use for especially non computer experts.
- (3) Only authenticated users should be able to use the FLogbook. It should be possible to log the textual as well as non textual data e.g. image, documents etc into FLogbook
- (4) It should be possible to transmit the logged information with attachment to concerned sub-system experts electronically.
- (5) It should be possible to query & retrieve the stored historical data with different search arguments.
- (6) It should be possible to add comments on logged faults by concerned sub-system persons.

SOFTWARE DESCRIPTION

Access to FLogbook has been protected with password so that only authenticated users could use the system. System checks user's credentials using institute's central e-mail server. Hence users may use the software using his/her official e-mail login and password.

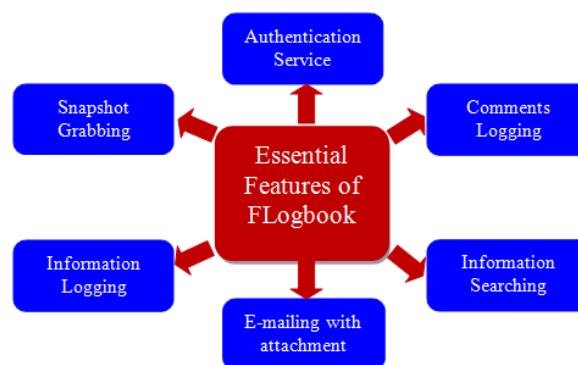


Figure 1: FLogbook Features.

Essential features of FLogbook have been shown in Figure 1. FLogbook is equipped with a software module for saving the computer's desktop in popular image files. This module has been developed in java and packaged in an executable jar file. On clicking the link provided in application this software module downloads & installs on user's machine & sits silently in system tray. This module is very useful for instant grabbing of machine control console desktop if any abnormality or unusual is noticed by the crewmembers.

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DEVELOPMENT OF A MONITORING SYSTEM FOR THE FL-net PROTOCOL

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Abstract

FL-net is being used as a communication protocol between the front-end computers and PLCs in several control systems at SPring-8 and SACLA. It is an Ethernet-based open standard protocols used for a factory floor networks. Furthermore, it is an UDP/IP-based master-less token passing protocol and supports cyclic transmissions. SACLA has experienced certain problems in terms of data acquisition when using FL-net for a beamline machine protection system. To resolve these problems, we developed a monitoring system for the FL-net protocol that captures and analyzes all packets of an FL-net network segment, detects protocol failure events, and stores the event information in a relational database. We can easily refer to the stored information in the database using a Web browser. The software-based monitoring system is highly portable and does not require a dedicated hardware-implemented protocol stack. This paper presents the monitoring system design for FL-net.

INTRODUCTION

FL-net was first introduced at SPring-8 in 2005 as a field-bus for the communication between the VME system and PLCs. The control systems using FL-net are as follows: a status monitoring of linac interlock system at SPring-8 [1]; a vacuum, RF high-power, and low-noise power supply control system; an undulator control system; a precise water temperature control system at SACLA [2]; and a facility control system at both SPring-8 [3] and SACLA [4]. Figure 1 shows a schematic view of a typical control system using FL-net at SPring-8 and SACLA. In our control system, FL-net shares Ethernet switches through the use of virtual LAN technology (VLAN). The SACLA control system currently utilizes 45 types of VLAN segments for FL-net. Packet capturing and protocol analyses are helpful for troubleshooting the network. On the other hand, analyzing a very large amount of captured data requires a lot of time and effort. In addition, since problems may occur at any time, we have to monitor the packets over the long term. For the SACLA control system using FL-net, a problem occurs at least once a month. While an FL-net protocol analyzer has been released on the market, it was not designed for a long-term monitoring.

We therefore developed a monitoring system for the FL-net protocol in March 2012, and started monitoring the system in May. Herein, we describe the design of the system and the effects of its installation.

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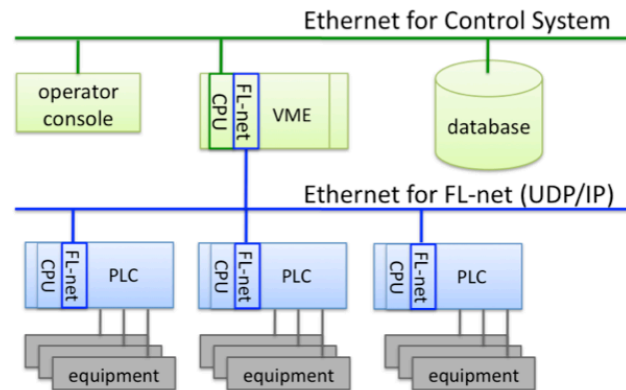


Figure 1: Schematic view of a typical control system using FL-net at SPring-8 and SACLA.

FL-net

The FL-net protocol was authorized by the Japan Electrical Manufacturers' Association (JEMA), and was established as a JEM standard in 2000 [5] and as a Japanese industrial standards (JIS) in 2004 [6]. Since several PLC vendors provide FL-net interface modules, we can build a control system using multiple vendor products. The FL-net protocol has the following features.

- The standard UDP/IP Ethernet communications protocol is used. Cables, hubs, and other networking components are readily available.
- The network operates at 10 Mbps (version 2.00).
- Up to 254 nodes can be connected to the physical network layer.
- Message transmissions for asynchronous data communication and a cyclic transmission are supported.
- Message transmissions sends/receives up to 1024 bytes of data.
- A cyclic transmission uses the common 8-Kbits and 8-Kwords memory shared by all nodes.
- Nodes can be automatically connected to or disconnected from the FL-net network by adopting a master-less token method.

SYSTEM DESIGN

Our design policy was to capture and analyze all packets flowing through the Ethernet of the FL-net network, and to record all problematic events. In FL-net, network packets continuously flow at a rate of ~ 4 Mbps. If all packets of the captured data are saved as files in pcap format, which is a standard format treated by open-source network analyzers such as tcpdump [7] and

MODULAR BEAM DIAGNOSTICS INSTRUMENT DESIGN FOR CYCLOTRONS

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Abstract

The Cyclotrons at VECC, Kolkata i.e. Room Temperature Cyclotron (RTC) and Superconducting Cyclotron (SCC) comprise of internal and external Beam Diagnostic systems. These systems provide the beam developer with position, intensity, beam profile, a visual impression of the size & shape of ion beam, and operational control over diagnostic components like 3-finger probe, Beam Viewer probe, Deflector probe, Faraday cup, X-Y slit, Beam viewer etc. [1]. Automation of these components was initially done using customised modules for individual sub-system. An expansion of this facility and various levels of complexity demand modular design to cater easy modification and upgradation. The overall requirements are analysed and modular cards are developed based on basic functionalities like valve operation, probe/ slit/ viewer control, position read-out, Interlock, aperture control of beam line and communication. A 32-bit Advanced RISC Machine (ARM) based card with embedded EPICS is chosen as the master controller and FPGA/ microcontroller is used for functional modules. The paper gives a comprehensive description of all modules and their integration with the control system.

INTRODUCTION

Various upgradations of different sub-systems are being done in both the cyclotrons at VECC, Kolkata are engaged with different kinds of experiments. RTC is getting modernized with new breed of automated beam diagnostics equipments whereas upgradation of internal beam diagnostic system is being done to facilitate internal beam tuning for better extraction at SCC. All the beam regions (injection, acceleration, extraction & external line) are employed with many beam diagnostic stations as per the beam tuning and transportation requirements [2]. The beam diagnostic stations are equipped with different set of components which are either electrical or electro-pneumatically controlled. Development of customized instruments with uniform control scheme, as employed in other sub-systems is required to control and monitor these diagnostic components.

DESIGN CRITERIA

The modular design of the diagnostic control instruments has undergone through several modifications for multiple times due to fast changing and customized requirements. The earlier versions of these instruments had common data and control lines [3]. This design had

the restriction of sharing hardware resources due to interfacing compatibility. The recent development introduces an EPICS embedded main controller card, interfacing with other functional modules through dedicated serial lines on backplane. This design has given liberty to the development of individual module while keeping the same software architecture. The developer gets a choice of selecting his own tool chain according to the complexity of functional requirements of the module.

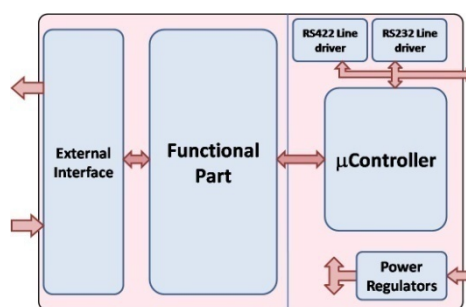


Figure 1: Block diagram of the basic scheme of module.

Each functional module is designed to have four building blocks: μ controller, functional component, communication and power supply as shown in Fig 1. AVR and C51 family controllers are used for the μ controller part. Functional part is designed as per the system requirements. Interface of these modules to main controller card is through dedicated TTL UART communication lines i.e. Rx (Receive), Tx (Transmit) and Ground. An optional RS232 line driver is also kept on each module for stand-alone operation.

HARDWARE MODULES

The newly designed instrument has a main controller card communicating with other functional modules and PC for controlling diagnostic devices. The description of developed hardware cards/modules are as follows:

Controller Card

The main controller card is designed using a Cavium ARM9 CPU based SBC (Single Board Computer) running on 250 MHz. This board has features like 64MB RAM, a bootable 4MB on-board flash, a microSD card slot and 5000 LUT (Look up table) Lattice FPGA. Interface to external devices can be done via Ethernet, USB host, USB device, or I2C ports as well as DIO, UARTs, and SPI which are implemented in the standard FPGA load. The SBC boots to Linux 2.6 from either an SD card or 4MB on-board flash having a bootable kernel image and an initial ram-disk image (Fig 2).

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FACILITY MONITORING SYSTEM USING STORAGE AREA NETWORK FOR VEC AND SCC

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Abstract

The facility monitoring system of cyclotron operational parameters at VECC is developed and commissioned recently. Storage Area Network (SAN) is used to isolate the control LAN and office LAN which ensures secured access of the control systems from outside world. EPICS gateway service and modified channel access save/restore tool have been used to integrate EPICS based control system of VEC and SCC with office network. This paper describes the implementation details of the overall facility monitoring system.

INTRODUCTION

The control systems of K130 variable energy cyclotron (VEC) and K500 superconducting cyclotron (SCC) at VECC, Kolkata, are isolated from each other as they run separately in their respective control network. However, online and historical monitoring of many important control parameters of both the facilities are required to be viewed from both the control rooms for proper diagnosis, maintenance and operation. Moreover, the facility managers, sitting at office network, require the automatic update of statistical information e.g. number of hours of beam time supplied to user, planned /unplanned shutdown etc. and hence, availability of control parameters from office network for automatic generation of operating reports and statistic in an application like spread-sheet for both the facilities are required. A facility monitoring system has been developed to cater all these requirements while maintaining access security aspects of the control networks as described in the subsequent sections.

PHILOSOPHY

A storage area network (SAN) is a dedicated network which is primarily used to make storage devices, accessible to computer servers. These storage devices appear like locally attached drive to the operating system of the server. A SAN network of storage devices is not accessible through the local area network by other devices and hence transaction of data from one network to other by means of SAN storage reduces vulnerability of cyber security threats. The facility monitoring system at VECC has been developed by adopting this idea where all the important parameters of both the facilities are transferred to the Office network for facility managers. A EPICS Process variable (PV) Gateway server [1], which can be

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configured to collect PVs from isolated networks and transmit them to another network, is installed. A software-based Firewall is also installed in the same Gateway server to provide the required access to perform CA monitor process to collect PVs from the IOCs running in the control networks. As all the required parameters can be accessed from the gateway server, one SAN server (SAN-1) is connected with the gateway server in a separate network. A channel access save/restore tool [2] is modified and installed in SAN-1 to save all parameters, to be forwarded in office-network, in the common storage. The other SAN server (SAN-2) which is connected in office network can access data-file containing the control parameters from the common storage. With this philosophy, one would ensure security of the control networks while passing all the required parameters in a separate network.

ARCHITECTURE

The overall system is divided into two layers where the first layer is the PV gateway layer (Dell PowerEdge) and second one is a storage area network where two servers (HP Server-1 and HP Server-2) are connected with a common storage through a point-to-point fibre channel as shown in figure 1. The gateway service is responsible for collecting all required parameters from SCC and VEC networks using EPICS channel access protocol. A channel access server process is available inside the gateway service which transmits all control parameters collected from the SCC and VEC control networks towards the SAN system. The gateway process has the ability to apply access security in addition to the access security configured in the firewall, running in the same gateway server, and hence, all incoming PVs are configured with read only access in the PV gateway.

The process running on SAN-1 server collects the monitoring parameters from the gateway server using CA protocol and saves the data into the common storage. The office-side server i.e. SAN-2 contains an duplicate EPICS IOC with all the PVs similar to the PVs collected from VEC and SCC control networks for monitoring. A modified channel access restore process on office-side retrieves the data from the common storage and update the duplicate IOC. An Apache-based web server running in SAN-2 collects the data from the IOC using EPICS CA-plugin application. The user can view the parameters in a web browser from the office LAN as shown in figure 2 and figure 3. The common storage (2.1 TB) is configured with RAID 5 and is divided into three logical

DESIGN AND IMPLEMENTATION OF AN IEEE 802.15.4 / ZIGBEE BASED STAR NETWORK FOR DATA ACQUISITION AND MONITORING

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Abstract

ZigBee based wireless technology is used to provide a low cost, low power, secured, PAN solution for monitoring of parameters from several distributed vacuum pumping modules installed in the SCC injection line. The parameters include module's pump RPM, input current and pressure reading of different vacuum gauges.

The ZigBee stack is written in a simplified form so that each node can create a network and can join to any established network when powered on. End nodes can be replaced through a little modification in the firmware codes. End node consists of sensors, signal conditioning circuits, microcontroller and ZigBee Transceiver whereas the Central node consists of microcontroller, Transceiver and UART interface. This paper highlights the future approach of utilizing this network for data acquisition related with environmental temperature, relative humidity, noise, water leakage from inaccessible areas of Cyclotron Vault, Pit, Basement and ECR Highbay for the ease of maintenance also the development of an environment monitoring system powered by solar cells covering a wide area.

INTRODUCTION

An Extremely Low Power (XLP) microcontroller based wireless network has been designed for several vacuum pumping modules using 2.4 GHz ZigBee [1] protocol on STAR topology. These pumping modules are installed at different locations of the SCC Injection line in a distributed manner. Two different network devices are designed to operate in this network, one is Coordinator and another is End device. Each End device acquires both analog and digital information from pumping module, generates a Zig Bee data frame for each sample and finally sends to the Coordinator. The frame structures follows IEEE 802.15.4 standards to keep the complexity to a minimum while at the same time making the network sufficiently robust for transmission in a noisy environment.

IMPLEMENTATION OF ZIGBEE

ZigBee is one of the global standards of low data rate wireless communication protocol formulated by the IEEE 802.15.4 working group. The ZigBee protocol has a transfer rate around 250 Kbps and 16 channels in the 2.4 GHz band [2], refer Fig.1, fully hand shakable protocol for transfer reliability, low power consumption (Tx or Rx mode or sleep mode) facilitating remote controlled battery operated systems and sensor network. The Higher Protocol Layers have been defined by ZigBee Alliance

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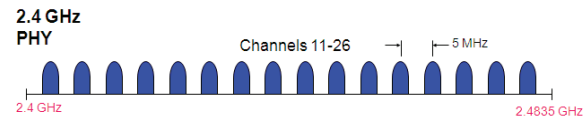


Figure 1: IEEE 802.15.4 PHY overview Operating Frequency band (Industrial, Scientific and Medical).

Group whereas IEEE 802.15.4 working group only utilizes the lowest two layers of OSI which are Physical Layer (PHY) and Data Link Sub Layer (MAC – Media Access Control Sub Layer) refer Fig. 2.

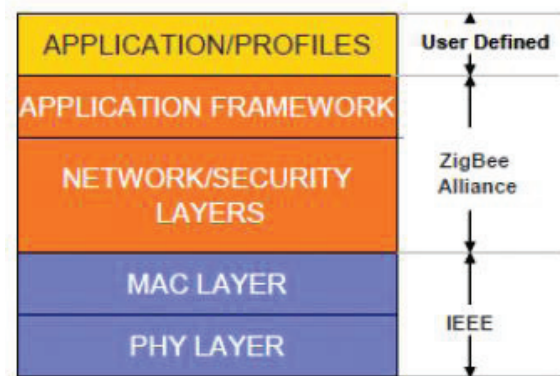


Figure 2: IEEE 802.15.4 Stack Architecture.

IEEE 802.15.4 standard supports several topologies refer Fig. 3 and the intention was to build a medium ranged (70 – 300 mtrs.) low data rate, low complexity wireless Personal Area Network to operate in an unlicensed international frequency range. ZigBee based wireless technology is implemented to provide such a solution.

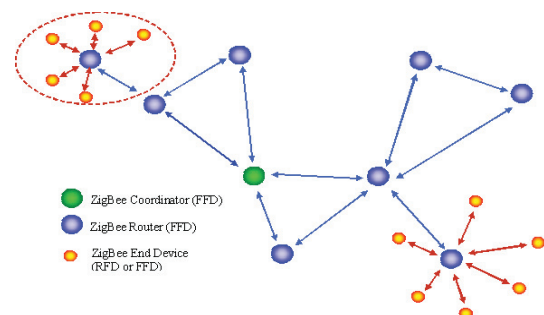


Figure 3: IEEE 802.15.4 standard Combined Topology, Highlighting STAR.

SCHEME OF THE SYSTEM

The star network has been developed by using two kinds of Zigbee nodes. Several End nodes are designed for each of the vacuum pumping modules and one

Socket-CAN DEVICE SUPPORT FOR EPICS IOCS*

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Abstract

This contribution describes an EPICS device support for CAN bus. It makes use of the Socket-CAN framework and is thereby independent from the API of a specific vendor. The device support has been used successfully in a production environment at the superconducting Darmstadt linear electron accelerator (S-DALINAC) since almost two years.

INTRODUCTION

CAN bus (Controller Area Network) has been chosen as the preferred field bus connecting in-house developed hardware to the S-DALINAC's accelerator control system. CAN bus is a rather robust communication bus. It allows a bit rate of 1 Mbit/s for distances up to 40 m. The underlying protocol is message-based. Every frame carries up to 8 byte of user data.

CAN interface controllers for personal computers are commercially available from different manufacturers, but although they all share the same basic functionality, most of them have a vendor-specific application programming interface (API). Moreover traditional CAN drivers are usually accessed by only one process at a time, which precludes the use of sniffer programs for debugging. In contrast to that the Socket-CAN network stack [1], included in recent Linux kernels, provides access to the CAN bus via network devices (BSD sockets). Those can be accessed by multiple applications at the same time via a vendor-independent interface. A set of open source CAN drivers provides access to controllers of different vendors.

For development purposes we use USB interfaces. They are easy to transport and can therefore be utilized to hook a laptop into a CAN bus segment for on-site diagnostics. The Linux computers running the IOCs (input output controller) are equipped with PCI/PCI express slot cards.

Since the S-DALINAC's accelerator control system is currently being migrated to EPICS [2], a CAN device support module has been developed to provide access to our devices from EPICS IOCs.

SOCKET-CAN

Opposed to a *character device driver based device support*, our solution here described relies on the Socket-CAN framework. The latter is included in the kernel main line since Linux kernel version 2.6.25, which is exceeded even by most of the conservative Linux distributions. On the

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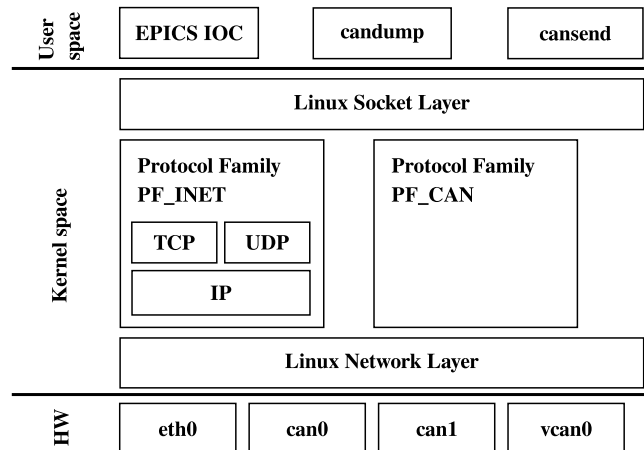


Figure 1: The Socket-CAN framework presents itself in the same fashion as the Linux kernel's network support. Different devices can be accessed by different applications at the same time. This is achieved by the network layer and appropriate protocol families.

one hand it brings along a growing number of CAN device drivers, on the other hand a network layer is implemented, which allows CAN interfaces to be treated in a similar fashion to ethernet devices [3]. The connection endpoint on the PC is represented by the Linux kernel as a BSD socket. The described functionality is combined in a so-called protocol family named **PF_CAN**. It is a common analogue of the **PF_INET** protocol family, which allows ethernet interfaces to be accessed with protocols like TCP and UDP. Both protocol families are provided by the kernel simultaneously. Figure 1 shows this architecture.

According to this concept, a CAN adapter does not just show up as character device `/dev/canX`, but needs to be brought up by

```
ip link set can0 up type can bitrate 1000000
```

as usual with ethernet devices. A virtual CAN device can be configured easily using the `vcan` kernel module. This is useful when doing IOC development without a physical CAN interface.

A central feature of the Socket-CAN framework is to reflect its bus property on the PC. While in hardware several participants can be connected to a CAN bus segment, the same should be possible on the PC. The Socket-CAN network stack makes this possible. Therefore, multiple applications, e. g. several IOCs and diagnostic tools, can be run

STATUS OF THE MIGRATION OF THE S-DALINAC ACCELERATOR CONTROL SYSTEM TO EPICS*

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Abstract

The S-DALINAC has been in operation for more than two decades. The control system has ever since been an in-house development. This contribution overviews the current status of the migration to a new EPICS-based control system. Several important subsystems have been adapted, but the process has not been completed yet. The general network infrastructure has been restructured in context of the ongoing migration and is also presented.

INTRODUCTION

The superconducting Darmstadt linear electron accelerator S-DALINAC was taken into full operation in 1991 [1]. Two separate control systems, one for beam transport and one for the rf controls, both based on VMEbus computers, were used. The former was upgraded once, with a VMEbus Single Board Computer equipped with a DEC Alpha CPU and running VxWorks [2]. The user interfaces had been developed on a OpenVMS cluster. Communication was carried out via a custom protocol over Ethernet. As the S-DALINAC is an accelerator exclusively developed by students, the life cycle of many subsystems is longer than the time of a full change of the staff. Moreover students can not be expected to have previous knowledge of the VMS operating system or VxWorks which made maintenance and further developments quite difficult.

When extension of the old control system became impossible, the development of a new control server was initiated. Since no real-time requirements for high level control need to be met, an architecture relying on standard PC hardware and TCP/IP was chosen for its low price and the good availability [3]. The resulting client/server control system is still in use. It controls most of the magnet power supplies and the movable scintillation screens used as an optical feedback for the operators. Due to its highly specific hardware, the rf control system still was stuck with the old computer hardware and software.

When the analog low-level rf control system was replaced by a modern digital solution in 2010 [4], a control system which could cope with the challenges of thousands of available parameters and diagnostic values was needed. For its Linux compatibility and its active community EPICS [5] was chosen. Already without writing program code it can be adapted to different needs, since the design allows extensive configuration of all aspects. Even the integration of proprietary hardware interfaces requires only

minimal programming effort, as the device support is well separated from the other parts of the system. The EPICS framework and most of the related tools are open-source software. There are no license issues at all.

After first on-site experience with the new control system the process of integrating more equipment unrelated to the rf control system started. A growing number of devices has ever since been integrated and existing single-purpose computer programs diminished leaving an increasingly cleaner operator environment.

HARDWARE

CAN Power Supplies

The S-DALINAC is an electron LINAC which is designed to provide beams of energies up to 130 MeV and 60 μ A. A low number of dipole magnets require currents between 50 and 300 A. The lenses, quadrupole magnets and steerers can be supplied with small power supplies (≤ 10 A of output current) which therefore contribute to the total number of approximately 200 magnet power supplies by 95 %. For replacement, an in-house development was preferred for cost reasons. The question for the hardware interface could be approached freely. A communication bus allows to connect multiple devices with a single cable and a single connector to the PC. The CAN (Controller Area Network) bus was chosen for its simplicity and cost-efficiency. Microcontrollers with built-in CAN controller are available. In contrast to ethernet-equipped controllers these are quite low-priced and need less configuration. Figure 1 shows the basic concept of the in-house developed hardware family.

Further Hardware Development

When different hardware was developed in-house later on, the basic design of the power supplies was adopted at its best. That is, not only do they share a CAN bus interface but even the same microcontrollers running the very same firmware. Even though the devices are fundamentally different in purpose, they share basic functionality like setting the power status. The firmware itself determines the type of hardware it is running on and adapts its behaviour accordingly. That is, the individual commands for each kind of hardware are provided.

Among others, the following hardware has been developed taking the same structure as basis:

- A multi-purpose measurement system which uses different modules to digitize voltages and currents, but

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MULTIPLE HIGH VOLTAGE POWER SUPPLY CONTROLS SOLUTION USING COMPACT, DISTRIBUTED ETHERNET BASED PC BOARDS AND LINUX/WINDOWS BASED GUIS

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Abstract

Compact Ethernet based High voltage PC boards have been developed, tested and produced to use as an integrated HV power supply unit to generate and control voltages varying from 0 to 2000 V dc from any OS independent PC platform. The Neutron gamma array (NAND) project at IUAC will need distributed control of at least 120 such units over a private Local Area Network to bias detectors. These Power supplies are being made as five independent boxes, each box consisting of 24 such HV PC boards and they will be interconnected using network switches. Presently, a compact two layer board with the PICO make DC-DC HV converter mounted on PCB, put together in a group of 24 of them, have been built and fully tested. The advantage of such a system is that, it is easily expandable to a large number of power supplies with low cost, globally accessible, multiple users in a network can set or read any power supply value through an OS independent PC. Control GUI applications are developed using C, IUAC PCLI [2], Qt c++ etc. and have been successfully tested.

INTRODUCTION

A large array of neutron detectors, named NAND [1] is being developed as a nuclear physics experimental facility to use with the beam delivered by the booster LINAC at IUAC. NAND will consist of about 120 detectors in the final phase in which each detector will have organic liquid scintillator cell coupled to Photonics photomultiplier tube. The detectors need to be biased at a dc voltage somewhere below 2000 V. A large number of compact power supply boards developed indigenously (approx. 70), has combined analog & digital circuitry in each PC board which can be addressed with unique MAC (Media Access Control address) and IP (Internet Protocol) address so that each can be specifically selected at a time for read write operations over distributed LAN.

THE HARDWARE

The COTS design of the H/W board for the HV generation and control, using the DC-DC converter module, is given in Fig.1 below. The board used SMD components due to its compact size required to fit-in 24 of them in a single box. The digital section consists of an 8 bit microprocessor (ATMEGA168/328) and an SPI driven Ethernet controller (ENCJ60). The analog section consists of a precise 12 bit DAC (AD 7541) connected to

the microprocessor using the parallel bits. A precision Voltage reference of 2.5 V is used externally to generate 0 to 2.5 V at its output. This voltage is amplified using a low offset high precision single supply OPAMP, CA3140, to generate 0-5 V for the DC-DC conversion. The small size PICO make HVP2N is used to generate 0 to -2000 V from a 0 to +5 V input. RJ45 connectors are used for the Ethernet connections to outside world. The block diagram of the HV control unit is given in Fig. 2.



Figure 1: The single compact HV board with Ethernet.

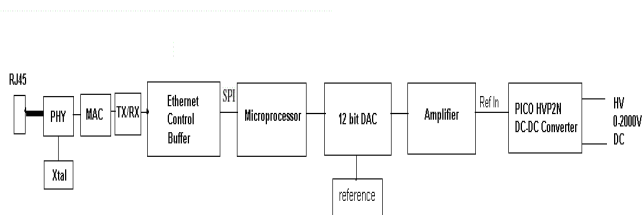


Figure 2: The block diagram of a HV control unit.

THE FIRMWARE

The boards use a small TCP/IP firmware stack. The TCP is used as the HTTP works on TCP protocol. The idea is to build an easiest user interface which brings in HTML code from the web server board into the browser client to perform simple read write operations using a

FAST DIGITAL FEED BACK CONTROL SYSTEMS FOR ACCELERATOR RF SYSTEM USING FPGA

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Abstract

Feedback control system plays important role for proper injection and acceleration of beam in particle accelerators by providing the required amplitude and phase stability of RF fields in accelerating structures. Advancement in the field of digital technology enables us to develop fast digital feedback control system for RF applications. Digital Low Level RF (LLRF) system offers the inherent advantages of Digital System like flexibility, adaptability, good repeatability and reduced long time drift errors compared to analog system.

To implement the feedback control algorithm, I/Q control scheme is used. By properly sampling the down converted IF signal using fast ADC we get accurate feedback signal and also eliminates the need of two separate detectors for amplitude and phase detection. Controller is implemented in Vertex-4 FPGA. Codes for control algorithms which controls the amplitude and phase in all four quadrants with good accuracy are written in the VHDL. I/Q modulator works as common actuator for both amplitude and phase correction. Synchronization between RF, LO and ADC clock is indispensable and has been achieved by deriving the clock and LO signal from RF signal itself. Control system has been successfully tested in lab with phase and amplitude stability better than $\pm 1\%$ and $\pm 1^\circ$ respectively. High frequency RF signal is down converted to IF using the super heterodyne technique. Super heterodyne principle not only brings the RF signal to the Low IF frequency at which it can be easily processed but also enables us to use the same hardware and software for other RF frequencies with some minor modification.

INTRODUCTION

A typical RF system of an accelerator consists of RF synthesizer, chain of amplifiers, RF cavity and other required sub systems. All these subsystems are realized using various active and passive components to fulfil the requirement for beam acceleration. Change in amplitude and phase characteristic of any of the component could lead to change in phase and amplitude of the EM field inside the cavity. To keep the amplitude and phase stable LLRF feedback control systems is used.

Block diagram of a typical Digital LLRF system is shown in the Fig. 1 which consists of four main components

- Synchronised LO and CLK generation
- RF to IF down conversion
- Digital controller
- Actuator

RF signal is first down converted to IF using mixer and appropriate LO signal. Synchronization between LO, RF and CLK is required for proper amplitude and phase detection. Controller is implemented in FPGA based digital signal processing board having fast ADC and DAC. The I/Q Modulator works as actuator to correct the amplitude and phase of RF signal. Digital signal processing schemes like CORDIC (COordinate Rotation Digital Computer), PI (Proportional Integral) controller and digital filters are used to implement the proper algorithm. These schemes are implemented using Vertex-4 FPGA.

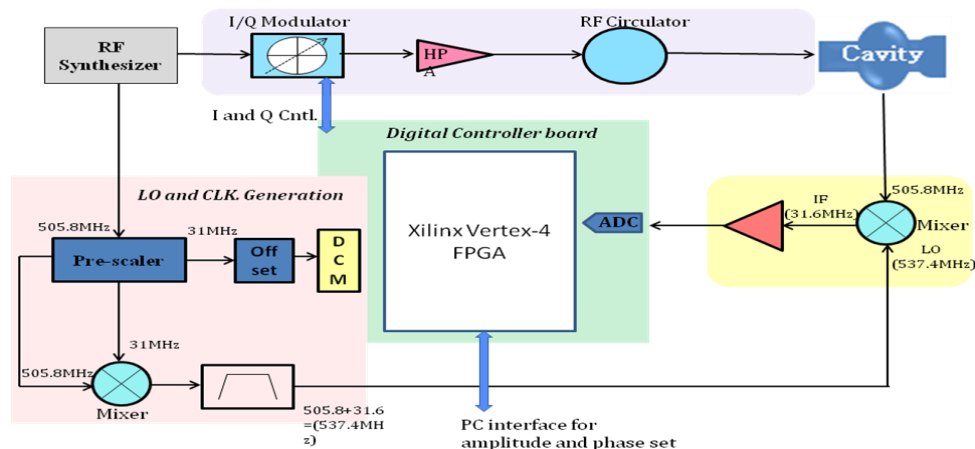


Figure 1: Block Diagram of Digital Feed Back Control System.

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API MANAGER IMPLEMENTATION AND ITS USE FOR INDUS ACCELERATOR CONTROL

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Abstract

The control system software needed for operation of Indus accelerators is coupled to the underlying firmware and hardware of the control system by the Application Programming Interface (API) manager. In the three-layered architecture of Indus control system, PVSS-II SCADA is being used at the layer-1(L1) for control and monitoring of various sub-systems. The layer-2(L2) consists of VME bus based system. The API manager plays a crucial role in interfacing the L1 and L2 of the control system. It has to interact with both the PVSS database and the L2. In order to access the PVSS database it uses the PVSS API, a C++ class library, whereas in order to access the L2 custom functions have been built. Several other custom functionalities have also been implemented. The paper presents the important aspects of the API manager like its implementation, its interface mechanism to the lower layer and features like configurability, reusable classes, multithreading capability etc.

INTRODUCTION

PVSS-II [1] has a highly modular structure. Various functionalities are handled by modules specifically created for different tasks. These modules are called *managers*. The Database (DB) and Event (EV) manager are the core managers that handle and manage all process variables of the system.

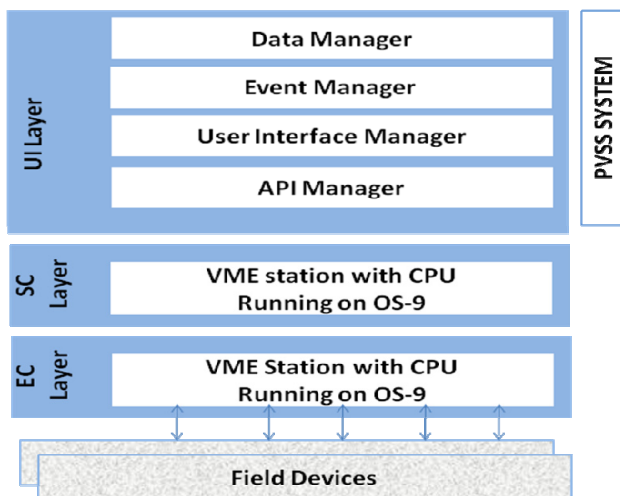


Figure 1: Software Layers of Indus-2 Control System.

The software layers of Indus-2 control system are as shown in Fig.1. PVSS system works at user Interface (UI or L1) Layer. The lower layers are Supervisory Control (SC or L2) and Equipment Controller (EC or L3) layers. The API manager is interfaced to the SC layer over Ethernet.

API MANAGER

What is API Manager?

PVSS offers a C++ application interface which enables it to extend its control functionality [2]. This interface allows the developer to implement his own custom functions together with full access to PVSS database. The self contained manager so implemented is called the API manager. It is also an interface for the integration of external programs [2]. Any software can be integrated in a PVSS System via class libraries provided by PVSS API. Implementation of these managers has been done for Indus-2 controls specific tasks. API managers have been developed for all sub-systems of Indus-2 viz. Magnet Power supply (MPS), RF, Beam Diagnostics (BDS), Timing (TCS), Vacuum (VCS), Radiation Safety (RSS), Machine safety and Interlock (MSIS), Beam line Frontend (BLFE) and Beam Orbit Correction.

Internal Structure of API

The API manager communicates with EV and DB

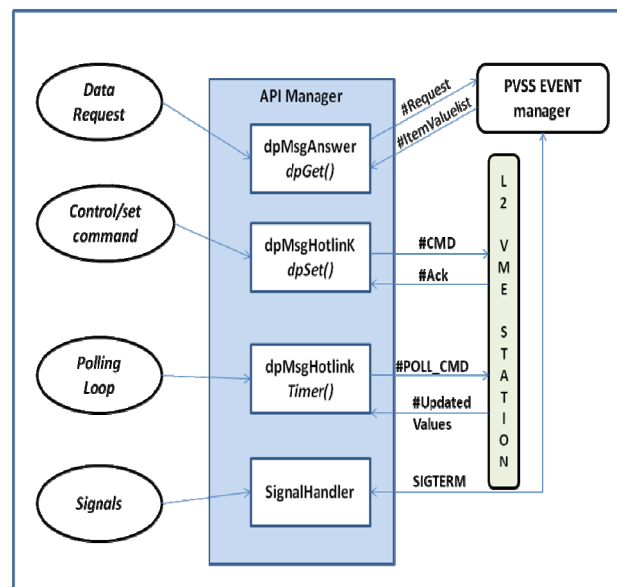


Figure 2: Event or Message handling by API.

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ADAPTIVE FUZZY CONTROL FOR TRANSFER CHANNELS IN PARTICLE ACCELERATORS

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Abstract

Long-term objective of this work is to develop a fuzzy technology based control framework to be applied in particle accelerators. Main motivation for this is the promise of fuzzy systems to exploit the tolerance for imprecision, un-certainty, and partial truth to achieve tractability, robustness, and low solution cost. Intended areas of application are manifold: we think on automatic operation, optimization of the operating conditions and yields; applied to various stages in the processing of circular and linear accelerators. As a first step towards this goal a fuzzy control system for a transfer channel in a particle accelerator has been developed. For it we built up the machinery, i.e. algorithms, data structures, integration in the existing control system and did a first proof-of-concept. Special emphasis is given on handling high dimensional data streams and the imminent challenges as sparsity and equidistance of the data.

INTRODUCTION

Model-based techniques for process control can provide valuable advantage over conventional approaches. They may yield a better understanding of the underlying system behavior than pure black box models and offer the opportunity to directly include expert knowledge. Such models, however, are costly to build and maintain when manually designed. Furthermore, they usually need to be continuously adapted since process conditions may change dynamically. Because of that evolving data-driven models with automatic adaptation techniques are becoming more and more attractive since they reduce maintenance costs while keeping high precision and interpretability.

Such a system that learns and evolves with every single sample from the data stream shall be developed for the use in a particle accelerator. A special problem here is the high dimensionality and homogeneity of the incoming data. For it, an additional projection step is implemented to reduce the dimensionality and filter out the most interesting ones.

Key ideas of the algorithm and the state of the work in progress are to be presented in the following. First we outline the current area of application within the DESY particle accelerator complex and sketch the algorithm's overall structure. In the following sections essentials of adaptive, i.e. evolving fuzzy systems are introduced and the projection mechanism is presented.

AREA OF APPLICATION

As a sandbox for its initial release the 450 MeV electron/positron transfer line between the accelerators PIA and DESY II within the pre-accelerator chain for PETRA III has been chosen. This decision was motivated by the ideal

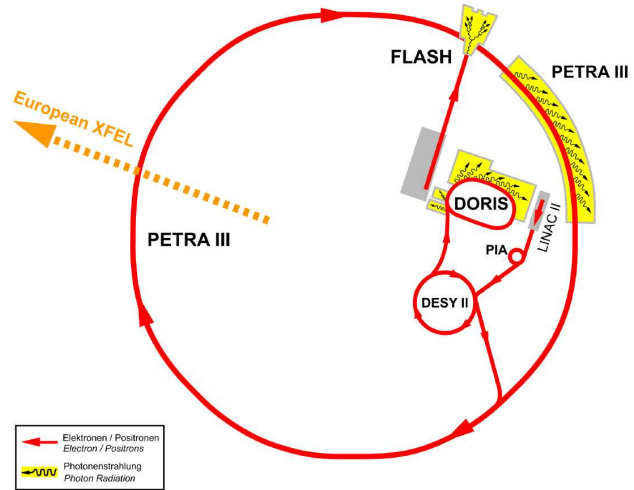


Figure 1: Particle accelerators at DESY.

test condition, since tests can be carried out parasitically to the regular operation at a quite high beam transfer frequency of 6 Hz. For a short overview over the DESY facility (Fig. 1) and its accelerators see [1]. The fuzzy control algorithms were integrated into the TINE-based accelerator control system via MATLAB codes.

OVERALL STRUCTURE OF THE CONTROL ALGORITHM

A modern method for the control of complex processes is *model predictive control* (MPC), also referred to as *receding horizon control* (RHC)[2, 3]. Model predictive control uses a time-discrete dynamic model of the process to be controlled to calculate its future states and output values as a function of the input signals. Using this prediction, in particular suitable input signals for desired output values can be found. While the model behavior will be predicated several steps ahead till a certain time frame, the input signal is usually only searched for the next time step and then the optimization is repeated. For the calculations of the next time step then the actual measured state is used, resulting in a feedback and thus a closed loop. Model predictive control technology offers a number of advantages that have made it one of the most widely used advanced control methods in the process industry. It can calculate control variables where classical nonlinear control techniques fail, is easily extended to multivariable problems, can take restrictions on the actuators into account, permits the operation near the constraints, allows a flexible specification of the objective function, delivers optimum control devices and is last not least model based. A typical controller structure to build a

DRIVE SYSTEM CONTROL FOR KOLKATA SUPERCONDUCTING CYCLOTRON EXTRACTION SYSTEM

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Abstract

The K500 Superconducting Cyclotron at VECC, Kolkata uses two electrostatic deflectors, eight passive magnetic channels, one active magnetic channel and two compensating bars as its extraction elements. Except the active magnetic channel, all the other elements can be moved radially, typically by ± 6 mm around a centre position. This maneuverability is due to the fact that not all the ions, spanning the operating region of the cyclotron, will have the same optimum beam extraction radius. At the end of the beam extraction channel, the beam is shaped and aligned by a pair of water cooled slit. The slit movement is pneumatically controlled as it has to be operated in high magnetic field. The computer controlled drive system can move the elements precisely. The paper will describe the drive system and its control mechanism.

INTRODUCTION

The extraction system in superconducting cyclotron [1] is required to extract the beam from the cyclotron. The extraction system layout is shown in fig. 1.

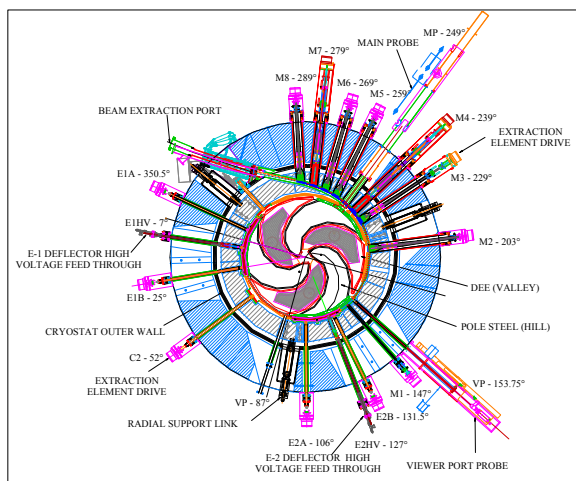


Figure 1: Extraction system layout.

It is inherently difficult to extract beam because of the high magnetic field and small turn separation. The high magnetic field itself exerts a strong centripetal force that has to be encountered to deflect the beam out of the cyclotron [2]. Because of the very restricted space in the cyclotron, the deflectors must be built with utmost care with proper

surface finish to achieve a high electric field gradient. After deflecting the beam to suitable radius using electrostatic deflectors (Fig. 2), magnetic devices called magnetic channels (Fig. 3) can complete the task of deflection. Compensating bars have to be judiciously installed to compensate addition of magnetic material due to magnetic channels.



Figure 2: Electrostatic deflector.

Beam dynamics demand that extraction components viz. electrostatic deflectors, magnetic channels and compensating bars should have accurate movement mechanism.



Figure 3: Magnetic channel.

SYSTEM DESCRIPTION

The magnetic channels are required to be moveable to suit extraction conditions of different beams. The movement mechanism has to be reproducible and precise. The drive

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RF DISTRIBUTION AND CONTROL SYSTEM FOR ACCELERATORS OF THE VEC-RIB FACILITY

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Abstract

RIB facility at VECC has several heavy ion linear accelerators like RFQ, two IH-LINACs and one buncher cavity operating at 37.8 MHz and two IH-LINACs with one buncher cavity at 75.6 MHz. Some more RF cavities are being designed at the third harmonic of 37.8 MHz and will be added in the RIB beam line [1]. All the cavities have separate RF power amplifiers with proper amplitude, phase and resonance frequency tuning and control system for efficient and stable operation. The Low Level RF control system has been operational for the power amplifiers of the existing RF cavities and improved design and development is carried out. An embedded controller based data acquisition and processing system is being used for control and local/remote operation. The RF distribution system as well as the design details of RF control system and remote control system will be presented in this paper.

RF DISTRIBUTION SYSTEM

The RF sources for the RIB accelerators consist of three 30 kW RF transmitters operating at 37.8 MHz, one 2 kW RF transmitter operating at 37.8 MHz and a 5 kW RF transmitter operating at 75.6 MHz [2]. A single oscillator at 37.8 MHz drives all the RF power amplifiers of the RIB facility. This is done using a 6-way power splitter

which divides the RF signal to the respective power amplifiers. For LINAC 3, which operates at 75.6 MHz, a frequency doubler is used to convert the 37.8 MHz signal to 75.6 MHz [3]. The forward and reflected power samples and pick-up signal from each of the RF accelerator cavities are fed to the low level RF control modules of the RF amplifiers. The schematic diagram for RF distribution is shown in Figure 1.

LOW LEVEL RF CONTROL

The Low Level RF (LLRF) control system regulates the amplitude and phase of the RF cavity voltage through fast electronic feedback mechanism. The frequency of the cavity is regulated through mechanical movement of a tuner loop in appropriate direction by sensing the frequency deviation. At present the control is based on the conventional amplitude and phase loop method. The scheme of the LLRF control is shown in Figure 2.

Amplitude Control

The important components in amplitude control comprises of the amplitude detector (realized with Schottky diodes HP5082-2835), PI controller and voltage controlled attenuators (realized with pin diodes based π configuration circuitry).

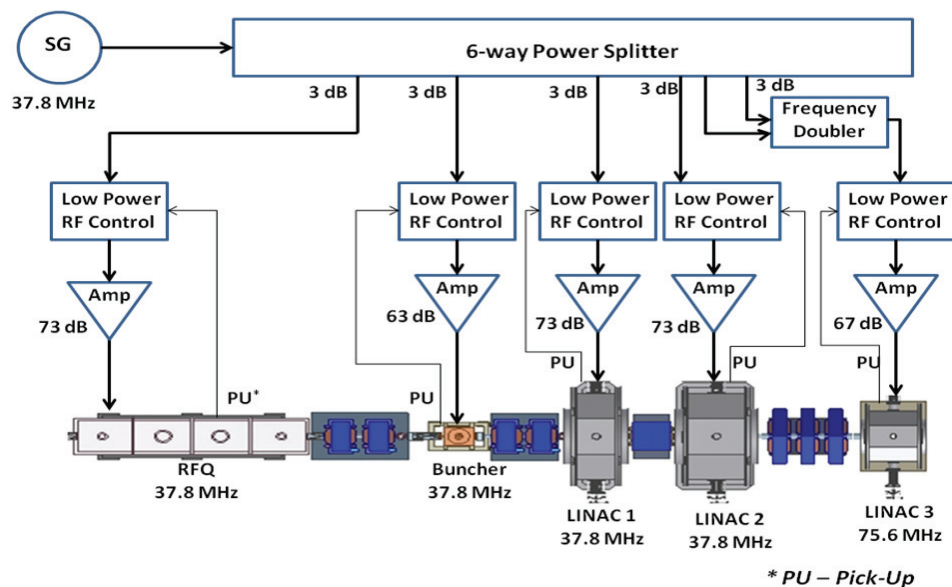


Figure 1: RF Distribution scheme for VEC-RIB accelerators.

TESTING OF INDUCTIVE OUTPUT TUBE BASED RF AMPLIFIER FOR 650 MHz SRF CAVITIES

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Abstract

A 650 MHz IOT based RF amplifier has been developed in VECC. It can be used to power several cavity modules in high energy high current proton linear accelerator to be built for ADSS programme in India and in Project-X at Fermilab, USA. The IOT based amplifier requires different powers supplies, water cooling and forced air cooling for its operation. A Programmable Logic Controller (PLC) based interlocks has been incorporated to take care of systematic on/off of the power supplies and driver amplifier, water flow, air flow and other interlocks for the safe operation of the RF System. In addition to that EPICS based RF operating console and data logging/monitoring system has been added.

INTRODUCTION

IOT based high frequency amplifier has been developed in VECC to power several 650 MHz high beta ($\beta=0.61$) RF cavities in ADSS programme and Project-X at Fermilab, USA. The amplifier uses the TH 793-1 Inductive Output Tube that delivers an output power of typically 85 kW in CW operation [1]. Specifications are given in Table 1. In addition to this, the amplifier is equipped with various impedance matching and biasing networks and two resonant cavities for input and output tuning. This water cooled amplifier requires five different power supplies naming filament PS, ion-pump PS, Grid PS, Collector PS and focus Coil PS. Among these auxiliary power supplies filament, ion-pump and grid are floating are in high voltage potential, i.e. collector/beam voltage (36 kV) and therefore mounted in an isolated frame in a separated cabinet called high voltage deck. The whole scheme is shown in Figure 1. The mains inputs of High voltage deck are electrically isolated by means of an isolating transformer. The amplifier is cooled by low conductivity water ($<2 \mu\text{S}$) and forced air. Water flow switches and air flow switches are installed at proper locations to have safety interlocks. In addition to that a PLC works as main control device. It acquires and controls all the analogue and digital readings and settings, supervises and interlocks the slower signals and handles the interfaces to the remote interlocking unit and the local control consol.

CONTROL SYSTEM OVERVIEW

Control architecture of our IOT based amplifier test system is a three layer architecture comprising of device

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Table 1: IOT Specifications

Output Power	70	kW
Frequency Range	650	MHz
Bandwidth	6	MHz
Beam Voltage	36	kV
Beam Current	3.4	A
Body Current	50	mA
Grid Current	-40	mA
Filament Current	24	A
Focusing Current	18	A
Efficiency	69.4	% typ
Gain	23.2	dB typ

layer, IOC server layer and user Interface layer. The device layer consists of PLCs which controls the automatic process sequence operations. The PLCs and the process components are configured to satisfy fail-safe operation. The user interface layer consists of the control computers where the operators issue the set points and the mode of operation commands. The system is controlled by means of Siemens S7-300 PLC which is handling all the field I/Os. PLC takes care of all safety interlocks of the amplifier like over-voltage, over-current, water flow and airflow. The PLC is programmed using Simatic manager Step7 [2]. All PLC programmes are written in STL (Statement List) i.e. the program consists of a sequence of mnemonic codes of the commands executed one after another by the PLC. Three auxiliary power supplies for the amplifier are located at high voltage deck floating at 36 kV. These power supplies and other instruments located at high voltage deck are powered through an isolation transformer (isolation: 40 kV). An ethernet to optical and optical to ethernet channel is used to navigate the control signals from HV deck to PLC. Two ethernet-optical fibre media converters and a 3 meter fibre optic cable are used to have the isolation between HV deck and PLC located at ground level. A siemens distributed I/O module (ET200) with ethernet takes care of all the I/Os at HV deck. The scheme used for HV isolation is given in Figure 2.

SUPERVISORY CONTROL

Supervisory control is the user interface layer part. In this layer the PLCs are being monitored and controlled

CONTROLS FOR A 10 PETAWATT CLASS LASER FACILITY

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Abstract

Computerised controls are vital to the operability and flexibility of large-scale physics facilities (such as accelerators, synchrotrons and high-power lasers) in providing fundamental services, for example: automatic configuring of specialist hardware; motion control; firing of shot sequences; enabling precision trigger distribution; vacuum monitoring and control, data acquisition and analysis.

The proposed 10 PW Laser Facility (300 J, 30 fs, 10^{16} W), in line with other major physics facilities around the world, will require a complex computer control system. This is expected to be modelled on the existing Vulcan Laser [1] computer control system and consist of a dozen or so Windows based PCs each of which will be running a separate and dedicated application to control a particular area or function of the facility.

This paper will present an overview of the existing Vulcan laser and provide a status report on the development towards the 10 PW which will require the control system to be designed to allow autonomous operation of the 10 PW Facility as well as to be fully integrated with the existing Vulcan laser controls for combined and synchronised 10 PW plus 1 PW operations.

INTRODUCTION

The Vulcan Laser

Vulcan is an high-power Nd:glass near-infrared laser with a physical footprint 75 m by 50 m (about the size of a couple of Olympic-sized swimming pools). It has roughly 250 m of optical beam path from the various laser oscillator sources through the numerous laser

amplification stages and on to the target areas. The laser is a multi-beam pulsed system with 'long' pulses of 0.3 ns to 6 ns duration synchronised with 'short' pulses of 500 fs to 20 ps duration. The initial short pulses start at the nJ level with 1 mm ~ 2 mm diameter beams and are amplified up to 500 J at 600 mm beam diameter providing a peak power of 10^{15} W i.e. a Petawatt. Using a large (1 m diameter) off-axis parabola, this beam is then focussed down to 5 microns onto various targets, where an intensity of up to 10^{21} Wcm⁻² is obtained. The facility is primarily used by university researchers working in the field of plasma physics to conduct fundamental research in particle acceleration, astrophysics and fusion energy.

The Vulcan Control System

The present control system as indicated above allows for a significant number of operational features to be manipulated. This is done either locally to the equipment or, more normally, remotely from the main control area as personnel are not permitted to be inside the laser area when high-power shots are being fired. In the main control room the laser operator is able to interrogate or change the status of equipment, change beam line parameters and initiate shot sequences. For this, the operators are presented with a number of control screens (generally touch activated) which gives them access to a real-time overview and control of the current state of the laser hardware. Figure 1 shows two of the central control interfaces used by the operators. These and other key control applications have been written in-house using Delphi 7 (visual Pascal) a choice that has allowed the development of a very robust and flexible operational system.

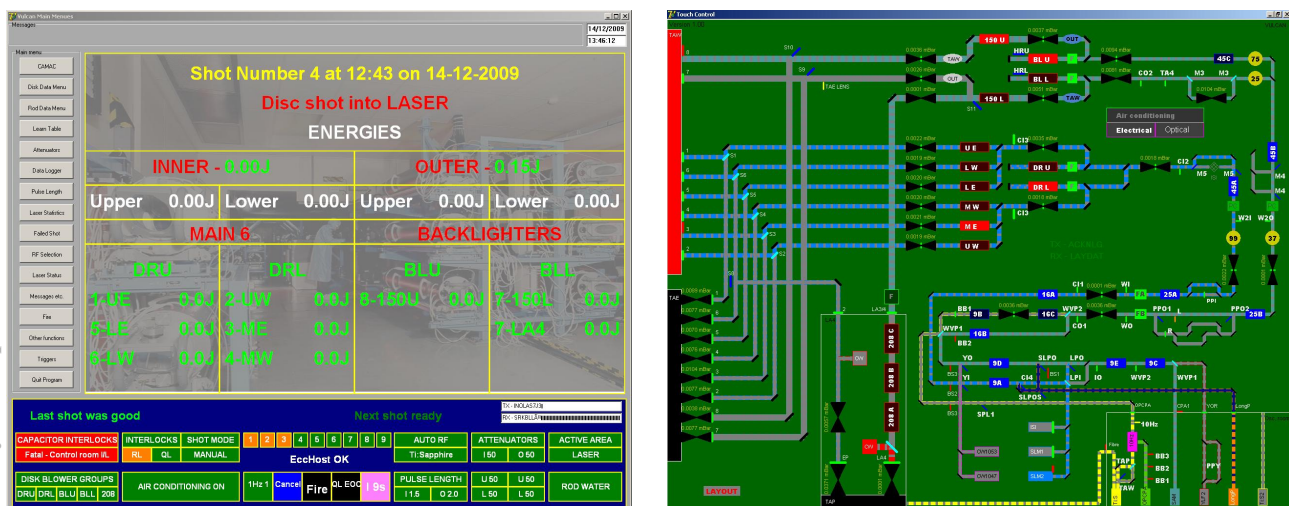


Figure 1: Laser Operators central control screens for (left) the main control, data acquisition and diagnostic interface; and (right) the system schematic showing overall active status of individual components.

INTEGRATED CONTROL SYSTEM FOR LEHIPA

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Abstract

The Low Energy High Intensity Proton Accelerator (LEHIPA) is a 20 MeV 30 mA proton accelerator which will be achieved in multiple stages [1]. LEHIPA consists of several sub systems/devices located at different positions of the beam path which includes ION source, RF Power, RF Protection Interlock System, Low Conductivity Water plant, Low Level RF control Systems, Vacuum System, Beam Diagnostics & Beam Line Devices. All these subsystems have their own local control systems (LCS) which will coordinate the operation of the corresponding subsystem. The control system for LEHIPA is thus being designed as a Distributed Control System with different teams developing each LCS. The control system will assist the operator to achieve a beam of desired characteristics by interacting with various sub systems of the accelerator in a seamless manner, protect the various parts of machine by generating the necessary interlocks, keep track of various parameters monitored periodically by suitably archiving them, alarms annunciation and trouble shoot from the control room. This paper describes approach to system design of ICS.

SYSTEM DESCRIPTION

The Low Energy High Intensity Proton Accelerator (LEHIPA) is a 20 MeV 30 mA proton accelerator. An overall design of the LEHIPA is given in Fig. 1. Electron Cyclotron Resonance (ECR) ion source gives DC proton beam of energy 50 keV and current of 30 mA. The low-energy beam transport (LEBT) system will consist of a magnetic system comprising of two solenoids that will transport the beam from the ion source, and match the beam into the acceptance of the RFQ. It will also have various beam diagnostic systems. For the acceleration of the proton beam at low energy, a four-vane RFQ (3 MeV, 30 mA, 350 MHz) is used. A Drift-Tube Linac (DTL) structure will accelerate the beam up to 20 MeV. The DTL is preceded by medium-energy beam transport (MEBT) section. The MEBT section will consist of four magnetic quadrupoles and a rebuncher cavity that will transport the beam from the RFQ to the DTL structures that follow, and match the beam into the acceptance of the DTL. For both the RFQ and the DTL high-power CW klystrons are used to generate the CW power of around 2 MW CW, at 350 MHz, along with high-power microwave lines to transport the RF to the accelerating structures.

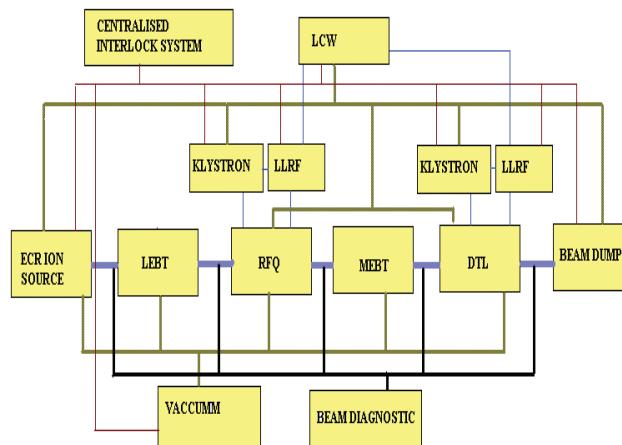


Figure 1: LEHIPA subsystems.

INTEGRATED CONTROL SYSTEM (ICS)

The integrated control system is designed as a 3 tier architecture depicted in Fig 2. The OWS layer hosts the presentation applications and run manager which is used by operators for machine run. The middle layer is the server layer where command control, parameter and configuration servers are hosted. The command control server is responsible for permitting commands to the equipment server depending upon macro level machine state logic. Parameter server is a data concentrator which collects data from different equipment servers, arrange data as per properties and present it to OWS layer. The equipment layer is the lowest layer. It is presented to the server and OWS layer through standard interface, it receives commands from higher layers and multicast its parameters to OWS layer. It hosts the access to the hardware. At the equipment level, the various actuators, sensors and measurement devices are interfaced to the control system through three different types of front-end computers.

CPCI computers dealing with high performance acquisitions and real-time processing; these employ a large variety of I/O modules. Typically, the LEHIPA beam instrumentation, RF Electronics System and the LEHIPA beam interlock systems use CPCI front-ends.

Systems like LCW System, ECR Injector uses PC based gateways interfacing systems as a large quantity of identical equipment is controlled through field buses.

CONTROL SCHEME FOR REMOTE OPERATION OF MAGNET POWER SUPPLIES FOR INFRARED FREE ELECTRON LASER

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Abstract

Infrared Free Electron Laser (IRFEL) is under development at MAASD, RRCAT Indore. The IRFEL machine consists of 90keV thermionic gun as electron source, beam transport line, 25MeV Linear Accelerator (LINAC) and an undulator magnet. There are fifty magnets on beam transport line. These magnets are energized by precision power supplies. These power supplies have local as well as remote control and will be located at equipment hall. The control room and equipment hall are at approximate distance of 300 m. We have planned a three layer structure for centralized operation of Beam Transport line Magnet Power Supplies (BTMPS). These layers are device interface layer, the equipment control layer and the presentation layer. Presentation layer is linked with equipment control layer on Ethernet. Whereas equipment control layer will be linked to device interface layer by RS-485. Device interface layer consist Magnet Power Supply Controllers (MPSC). Each MPSC has one master and five slave controllers linked on isolated SPI bus, which will control five BTMPS. We have developed slave controllers and a master as prototype of MPSC. This paper describes MPSC prototype and proposed control scheme.

INTRODUCTION

The Free Electron Laser (FEL) laboratory is developing Infrared Free Electron Laser (IRFEL) as part of their ongoing development activity. The machine is having a 90Kev thermionic gun as an electron source, beam transport line, 25Mev linear accelerator (linac) and an undulator magnet. The beam transport line for the FEL has two parts: a low energy part & a high energy part. Low energy part has solenoids to transport a beam from the thermionic gun to the linac entrance. A high energy beam transport line consisting of dipoles, quadrupoles and steering magnets for transporting beam from the linac exit to the entrance of the undulator. These magnets are energized by Beam Transport line Magnet Power Supplies (BTMPS). There are fifty numbers of such BTMPS. These BTMPS have local as well as remote control. BTMPS are located in equipment hall. BTMPS will be controlled from control room located at a distance of approximately 300 meters from equipment hall. These BTMPS are remotely operated by Magnet Power Supply Controller (MPSC) connected to control computer on RS-485 network. Inside MPSC, there is one master and five slave controllers linked on isolated SPI bus. Each MPSC is designed to control five BTMPS.

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BEAM TRANSPORT LINE MAGNET POWER SUPPLY (BTMPS)

Several types of magnets are required to transport the beam through beam line. For these magnets, numbers of supplies of various voltage and current ratings are required. We have listed power supply types and there important parameters in Table 1.

Table 1: BTMPS Parameters.

Magnetic element	Qty	Current rating	Voltage rating	Required Stability
Corrector Magnets	15	7 A	+/- 15V	100PPM
Dipole Bending Magnets	5	20 A	30V	100PPM
Quadrupole Magnets	15	13 A	+/- 15V	100PPM
Steering Magnets	15	10 A	+/- 10V	100PPM

Presently five power supply units are mounted in a 6U card frame. Hence there are ten such card frames, housing 50 supplies. Each power supply can be operated in local mode from front panel and in remote mode from PC. There is a 25-pin sub-D connector provided on the power supply which has digital & analog I/O signals for power supply remote operation. Each power supply has one analog input signal in the range of 0-10V to set the current output, 0-10V analog output signal which is proportional to set current. There are four digital inputs to power supply. These inputs are used to switch on power supply, to switch off power supply, one input to reset power supply faults and one for changing polarity of power supply current output. Power supply provides three digital status lines with galvanic isolation. They are ON/OFF indicator, Fault indicator, and Remote/Local indicator.

MAGNET POWER SUPPLY CONTROLLER (MPSC)

Keeping power supply configuration in mind we have designed MPSC in standard 3U card frame. Each MPSC card frame has five independent power supply controllers (slave controllers) and one master controller as shown in Figure 1. Master controller accepts command from PC located at control room via RS-485 port and then sends these commands to appropriate power supply controller over a local isolated SPI bus. We have planned to place these MPSC in 19" rack of 32U height. This implies 15

A DISTRIBUTED CAN BUS BASED EMBEDDED CONTROL SYSTEM FOR 750 keV DC ACCELERATOR

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Abstract

This paper describes a distributed embedded system that uses a high performance mixed signal controller C8051F040 for its DAQ nodes and is based on CAN bus protocol for remote monitoring and controlling of various subsystems of 750 keV DC accelerator based irradiation facility at RRCAT, Indore. A PC with integrated PCI CAN card communicates with intelligent DAQ nodes over CAN bus and each node is interfaced with a subsystem. An opto isolated SN65HVD230 CAN driver is interfaced between each node and physical bus. Remote frames and message prioritising are used for efficient control. The PC application is developed using LabVIEW 8.6. The proposed system is more reliable and noise immune as compared to previously used systems that initially used a centralized system based on C8051 controller. This was then upgraded to a distributed system that used microcontroller AduC812 and communicated over RS485 link. The new system has been integrated and tested satisfactorily for its designed performance with test jigs that simulated the actual subsystems with a bus length of 75 meters. First the complete scheme of the system is presented, and then the hardware and software designs are discussed.

INTRODUCTION

A 750 keV 5 mA electron beam accelerator has been developed and commissioned for industrial processing application at RRCAT, Indore. In this accelerator a directly heated diode gun is used as an electron emitter, which is floating at minus 750 keV DC with respect to the earth. The accelerating voltage for the accelerator is generated using a 12-stage symmetrical voltage multiplier stack. The input to the multiplier stack is derived from a high frequency resonant inverter through ferrite core high voltage transformer. The inverter output and hence the high voltage is varied by controlling the DC bus voltage of a three phase fully controlled converter which feeds the inverter. The filament power supply is derived from the top of the multiplier stack across its isolation columns, which has an inherent isolation of 750 kV with respect to the earth. The accelerated electron beam is focused by two focusing coils and is made to scan the material under process with the help of a scanning magnet field. The high voltage stack, the accelerating column and the filament power supply are closed in a pressure vessel, which is filled with SF₆ gas at a pressure of 5 atmospheres. The accelerator, which is under operation at RRCAT, Indore since 2002 is being used for research and development in the field of irradiation processing.

The PC based control and monitoring system of this DC Accelerator is being upgraded for easier operation and

better control and monitoring of different parameters of the accelerator and allied subsystems.

HARDWARE DESCRIPTION

The PC based system, controls and monitors different parameters of various subsystems of the DC accelerator which includes different power supplies, various control units, transducers, on/off controls, search and scram system etc. The analog parameters, which are being controlled and monitored, include accelerating voltage, emission current, filament current, scanning coil current among others.

In the proposed scheme that uses a distributed control system communicating over CAN(Controller Area Network) bus, each power supply and subsystem which is to be monitored and controlled through PC is interfaced with a data acquisition card (DAQ node). The DAQ node implements a microconverter C8051F040 from Silicon laboratories, which has an inbuilt high speed 8051-compatible CIP-51 core and a CAN controller. It also has a 12 bit ADC with 8-channel analog multiplexer and two 12-bit DACs. All analog inputs are taken in through differential amplifiers to reduce the effects of common mode noise. The DAQ node can also monitor eight digital inputs and control eight digital outputs.

All the DAQ nodes are connected on a common CAN bus line. The control PC is connected on the same CAN bus through an integrated PCI CAN card. CAN bus message based communication protocol is used for communication between PC and the DAQ nodes.

Each DAQ node will be allocated messages with specific addresses and will act as a slave. The PC is the master and communicates with the power supplies and other subsystems through this known message addresses using normal and remote frames. The data will be embedded into the well-framed message packets. As a result of the content-oriented addressing scheme, a high degree of system and configuration flexibility is achieved.

CAN is a distributed serial bus system widely used in industrial control applications, where robust environment exists. It provides high level of data integrity and automatic bus arbitration. It supports a multi-master hierarchy, which allows building intelligent and redundant systems with broadcast communication. It provides sophisticated error detecting mechanisms and re-transmission of faulty messages. For error detection the CAN protocol implements three mechanisms at the message level: Cyclic Redundancy Check (CRC), Frame check, ACK errors. The CAN protocol also implements two mechanisms for error detection at the bit level: Monitoring: Each station that transmits also observes the bus level and thus detects difference between the bit sent

HIGH VOLTAGE CONTROLLER SYSTEM FOR SPECTROSCOPY DIAGNOSTICS OF SST-1

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Abstract

We have developed special instrumentation for spectroscopy diagnostics of the SST-1 Tokamak. Light output in the visible spectrum is guided through fiber optics from the Tokamak ports to the diagnostics Hall, where photo multipliers tubes and other instrumentation electronics are kept. High Voltage (0 - 1500 V) bias generation electronics is required to bias these PMTs. Total 14 PMTs to be biased for overall requirements of the diagnostics. We have developed modular electronics for HV bias generation, which consist of one controller and seven HV modules. We have designed and developed FPGA based controller card which controls seven HV modules. The Slot-0 card is having Spartan 3E FPGA and Standalone Controller Area Networking (CAN) controller. 32-bit RISC processor Microblaze has been deployed into the FPGA. We have used Hitek make HV supply modules which is programmable. In the HV modules, Analog Device Inc. make iCoupler, digital isolators are used to break the ground loops and to avoid ground-lifting problem. Various features like Manual mode/Remote mode operation, HV ON/OFF, HV Value setting through remote GUI have been developed on LabVIEW software.

SPECTROSCOPY DIAGNOSTICS ON SST

Spectroscopic diagnostic is an important tool to know about impurity content in plasma and other plasma parameter like electron and ion temperature, electron density, Z-effective. Light from plasma is been transported from a glass window through optical fiber and lens arrangement up to the detector, (photo-multiplier tube). In order to detect a range of signal we need to keep options of variable gain and filter bandwidth, programmable biasing of PMT to detect weak signals. This helps to study some of the perturbation at faster time scale.

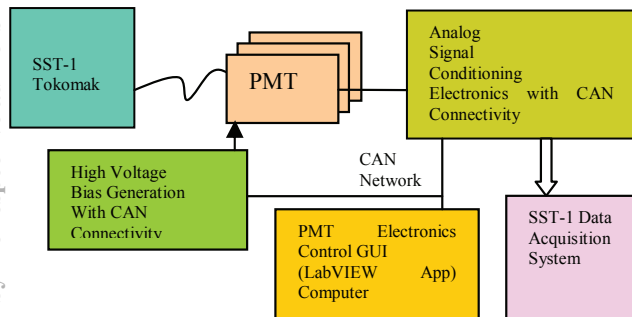


Figure: 1 Spectroscopy Diagnostics scheme of SST-1.

So we need to design electronics system with which we can play to study and monitor this phenomenon in plasma and characterize it during experimental campaigns. Total seven optical ports will be used for spectroscopy diagnostics of Phase-1 of SST-1 development. Figure 1 shows the diagnostics general block diagram.

HV ELECTRONICS DESIGN

The SST-1 spectroscopy diagnostics requires two types of electronics, one is analog signal conditioning, which is responsible for amplifying PMT current output and converting into voltage. The second one is high voltage bias generation. To meet the physic experimental requirements it was decided to keep the high voltage remotely programmable. To achieve the above mentioned goal modular electronics development was chosen. The 4U/10T size modular chassis is housing of the electronics pcbs. This chassis has total eight 4U slots, The Slot-0 is Microprocessor based card. Remaining seven slots (Slot-1 to Slot-7) are high voltage generation modules. The Slot-0 controller is intelligent device and is responsible for overall control of all seven HV modules and also communicates with remote computer with Controller Area Networking (CAN) protocol. We have chosen 32 bit RISC architecture based MicroBlaze soft processor on FPGA as main control unit. Because it is soft processor we could add many soft peripherals to it according to requirements of controlling seven HV modules.

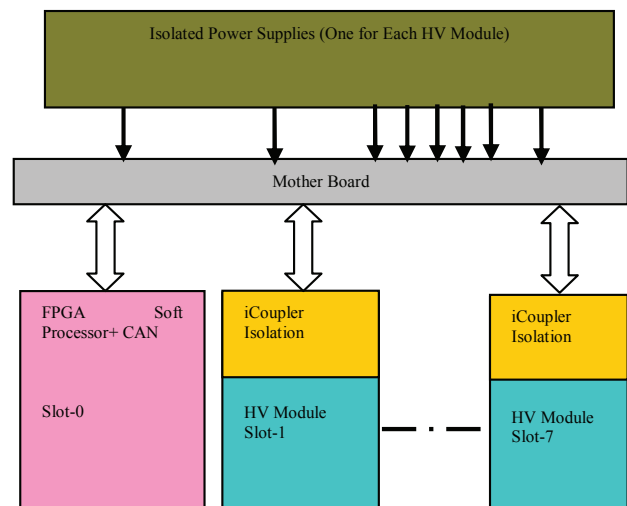


Figure: 2 Modular structure of HV Electronics.

At the time of designing electronics we also considered grounding issues, PMTs are connected to not only HV modules but also seven different transconductance

PROGRESS OF THE JINR e-LINAC ACCELERATOR TEST-BENCH CONTROL SYSTEMS

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Abstract

Due to Joint Institute for Nuclear Research participation in ILC collaboration, e-linac accelerator test-bench is being created in the Laboratory of high energy physics of JINR. The bench is designed for several goals: accelerating structures and diagnostics testing, photoinjector prototype creation and investigation, radiation resistance studies of different materials etc. In addition, several proposals of FEL creation on the basis of the e-linac exist. Current setup, results of the test-bench control systems evolution since 2009 and future plans are presented. The most important updates include radiation control system calibration, verification and installation and an upgrade of the video control system.

INTRODUCTION

Linear accelerator test-bench in the Joint Institute for Nuclear Research is based on the so called MEA accelerator [1] – part of the accelerator complex which was transferred to the possession of JINR by the National Institute for Subatomic Physics (NIKHEF, Amsterdam).

In 2009 successful commissioning of the test-bench injector with beam energy of 400 keV was performed [2]. Since then a number of upgrades was done in bench control systems. Video and analog signals control system was substantially extended. Another major upgrade was calibration and verification of the Automatic system of radiation safety control gamma-detectors in JINR Radiation Safety Department and start of this system operational testing. The short description of non-upgraded since 2009 Electron gun control system is also given.

At the present time the injector (composed of electron gun, chopper, prebuncher and buncher) and the first accelerating section are assembled and put into operation. Estimated beam energy is about 25 MeV. In the short term it is planned to use the bench as a driver for the infrared FEL. The undulator of the IR range (transferred to JINR by NPO of automatic systems, Samara; $E = 25$ MeV, $\lambda = 18.7 \mu\text{m}$) is going to be installed.

VIDEO AND ANALOG SIGNALS CONTROL SYSTEM

While only electron gun was in operation, the video system was composed of two IP-cameras (both are still working at the same places):

- Aviosys 9060 A is used for bench room general surveillance;
- Aviosys 9000 is installed next to the prebuncher and used for observing initial beam profile. The screen position in the beamline can be controlled remotely from the control room.

Both cameras are connected to the video control system computer by LAN. Aviosys Surf16Ch software is used for imaging.

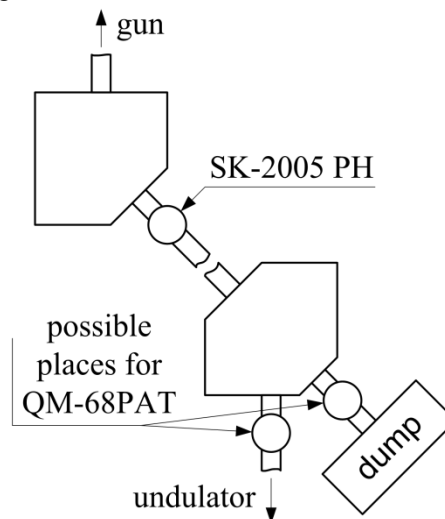


Figure 1: Analog cameras arrangement (top view).

After installation of the two bending magnets in 2012 two more cameras were installed:

- Sun Kwang SK-2005 PH analog camera is installed next to the first bending magnet;
- Q-cam QM-68PAT analog camera can be installed in two places (manually) which are shown in Fig. 1.

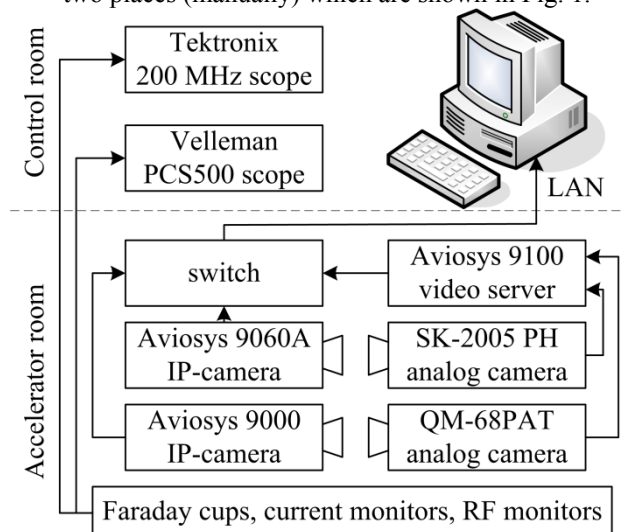


Figure 2: Scheme of the VASCS.

Until October 2012 both analog cameras were connected to the video control system computer using BeholdTV 409 FM TV-tuner (with manual switching between cameras). Now the video server Aviosys IP Video 9100 is being used. This server allows

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Qt BASED CONTROL SYSTEM SOFTWARE FOR LOW ENERGY ACCELERATOR FACILITY

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Abstract

Qt based control system software for Low Energy Accelerating Facility (LEAF) is operational at Bhabha Atomic Research Centre (BARC), Trombay, Mumbai. LEAF is a 50 keV negative ion electrostatic accelerator based on SNICS ion source. Control system uses Nokia Trolltech's QT 4.x API for control system software. Ni 6008 USB based multifunction cards has been used for control and read back field equipments such as power supplies, pumps, valves etc. Control system architecture is designed to be client server. Qt is chosen for its excellent GUI capability and platform independent nature. Control system follows client server architecture. Following paper will describe the control system.

INTRODUCTION

Low Energy Accelerating Facility (Figure 1) is a 50 keV DC electrostatic accelerator operational at Van de Graaff building in Bhabha Atomic Research Centre, Trombay, Mumbai [1]. LEAF can accelerate various beams across periodic table. A sputtered negative ion source generates negative ions which are accelerated using high voltage. For this purpose entire ion source floats at negative high voltage (typically -50 kV). Extracted ion beams are bent by a 90 degree magnet which acts as mass analyzer and selects desired mass to deliver at target. Ion currents delivered at target is micro amperes of particle current for prolific beams such as C⁻ or H⁻ and for difficult beams such as Li⁻, delivered current at target is few hundred nano amperes. This accelerator has already delivered negative ion beams of Hydrogen, Lithium, Carbon, Sulphur, Tellurium, Gold, and Silver etc. This accelerator is used for various experiments in material science and atomic physics studies using ion clusters [1].

Though LEAF is a small accelerator but smooth and efficient running of this accelerator requires robust control system. To deliver the various energies and

masses of the ion beams at the target it is required to tune the beam by changing various power supply voltages and currents. Control System receives operator command and set the values on field devices. Data acquired from the field devices are displayed on the GUI and used for the interlocking system. LEAF control system consists of a data acquisition and operator command execution module and Graphic User Interface (GUI) based analog and digital control interface.

One of the aims of the LEAF control system was to make it automatic, so that a good set of parameter values can be automatically loaded by the control system in a gradual and safe way without the intervention of operator.

DESCRIPTION

Analog and digital field data is acquired from the field via National Instrument's micro-controller based (NI 6008) system. It is a low cost, USB powered multifunction DAQ. It has 8 analog input channels which gives 12 bit resolution for differential connection and 11 bit resolution for single ended connection. It has a sampling rate of 10kS/s which is sufficient for the control requirement of LEAF. NI 6008 has 12 digital channels which can be configured either digital in or digital out. Digital channels, in digital out mode are used to turn on and off devices. Digital input modes reads the actual on off status of the device. Single ended analog input channels are used to read the analog field signals [2].

LEAF control and instrumentation is physically divided into two parts because Ion source of LEAF and all power supplies are floating at negative 50 kV. Non ion Source parameters are at ground potential.

LEAF control software has the client server architecture (Figure 2). To Ensure proper galvanic isolation, a dedicated server is written for the ion source side. Another server deals all the other parameters at ground potential.



Figure 1: Low Energy Accelerator Facility.

MODELLING AND SIMULATION OF INDUS-2 RF FEEDBACK CONTROL SYSTEM

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Abstract

Indus-2 synchrotron radiation source has four RF stations along with their feedback control systems. For higher beam energy and current operation amplitude and phase feedback control systems of Indus-2 are being upgraded. To understand the behaviour of amplitude and phase control loop under different operating conditions, modelling and simulation of RF feedback control system is done. RF cavity baseband I/Q model has been created due to its close correspondence with actual implementation and better computational efficiency which makes the simulation faster. Correspondence between cavity baseband and RF model is confirmed by comparing their simulation results. Low Level RF (LLRF) feedback control system simulation is done using the same cavity baseband I/Q model. Error signals are intentionally generated and response of the closed loop system is observed. Simulation will help us in optimizing parameters of upgraded LLRF system for higher beam energy and current operation.

INTRODUCTION

Indus-2 is a synchrotron radiation source at Raja Ramanna Centre for Advanced Technology, Indore, India. Presently it is being regularly operated in round the clock mode with stored current of 100 mA at 2.5 GeV. The role of RF system at this facility is to boost the electron energy from 550 MeV to 2.5 GeV and compensate for synchrotron radiation losses. The RF system employs four numbers of elliptical cavities to generate sufficient accelerating RF voltage, each excited by individual RF station. Each station consists of a high power RF amplifier, solid state driver amplifier & LLRF feedback loops to keep the cavity RF field stable [1].

For higher beam current and better performance of LLRF feedback control loop it is being upgraded to digital feedback system. Inphase and Quadrature (I/Q) modulation technique is being implemented with FPGA based digital controller. To understand the behaviour of I/Q based feedback LLRF control system under different operating conditions, modelling and simulation is done. Modelling and simulation also helps in algorithm study, controller design and optimization. Baseband simulation has been performed as it makes the simulation faster due to better computational efficiency and for its close correspondence with the actual implementation. A description of the models and corresponding results has been discussed.

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RF CONTROL SYSTEM MODELLING

RF Cavity Model

Resonant modes of cavity can be described by means of resonant LCR circuits. In equivalent LCR model it is assumed that voltage across the resistor is the cavity gap voltage. A parallel LCR circuit with an input current source is shown in Fig. 1.

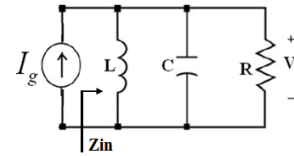


Figure 1: Parallel LCR resonant circuit.

The power source feeding power to RF cavity can be modeled as an LCR circuit driven by a current source I_g through transformer as a coupler [2]. An RF cavity resonator coupled by means of a $1:N$ transformer [3] to an input RF power source with internal impedance Z_o is shown in Fig. 2 and the same is simplified in Fig. 3.

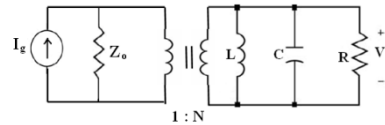


Figure 2: RF cavity coupled to an RF power source.

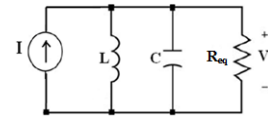


Figure 3: Equivalent circuit of Figure 2.

Where R_{eq} represents the equivalent impedance of the cavity under loaded condition. Cavity gap voltage is given by Eq. (1).

$$I = \frac{1}{L} \int V dt + C \frac{dV}{dt} + \frac{V}{R_{eq}} \quad (1)$$

Eq. (1) can also be rewritten in terms of bandwidth $\Delta\omega$ and resonance frequency ω_o as Eq. (2):

$$\frac{d^2V}{dt^2} + \Delta\omega \frac{dV}{dt} + \omega_o^2 V = \frac{1}{C} \frac{dI}{dt} \quad (2)$$

Laplace transform of Eq. (2) is given by

$$\frac{V(s)}{I(s)} = \frac{s/C}{s^2 + \Delta\omega s + \omega_o^2} \quad (3)$$

AN EMBEDDED SYSTEM BASED COMPUTER CONTROLLED PROCESS AUTOMATION FOR RECOVERY AND PURIFICATION OF ^{99m}Tc FROM $(n,\gamma)^{99}\text{Mo}$

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Abstract

^{99}Mo produced ^{99m}Tc ($t_{1/2}=6\text{hr}$, 140keV γ -ray) is the most useful radioisotope for nuclear diagnostics. High specific activity ^{99}Mo is supplied globally mainly by five old reactors whose routine or unscheduled maintenance shut-down causes supply irregularities that adversely affects patient management in nuclear medicine centres. ^{99m}Tc may also be produced via $^{98}\text{Mo}(n,\gamma)$ in a natural MoO_3 target in reactor or by $^{100}\text{Mo}(n,2n)^{99}\text{Mo}$ or $^{100}\text{Mo}(p,2n)^{99m}\text{Tc}$ reaction in cyclotron. To meet the crisis proposals are there to produce ^{99}Mo by $^{100}\text{Mo}(n,2n)^{99}\text{Mo}$ or ^{99m}Tc directly by $^{100}\text{Mo}(p,2n)^{99m}\text{Tc}$ in a cyclotron. Of the several separation methods of ^{99m}Tc from molybdenum, the most common are adsorption column chromatography, sublimation and liquid-liquid solvent extraction. The conventional methods besides being cumbersome are often hazardous, polluting, require skilled manpower and facilities like fume hood and so are not always practically feasible for hospitals. To address these, VECC and BRIT, Kolkata have collaborated to develop an embedded system based automated $^{99}\text{Mo}/^{99m}\text{Tc}$ generator from low specific activity ^{99}Mo using solvent extraction technique, supervised by a PC based GUI.

INTRODUCTION

Technetium-99m ($t_{1/2} = 6.02\text{h}$; 140.51 keV (89%), principle γ -emission energy) is known to be the most useful radioisotope in diagnostic nuclear medicine. More than 80% of all diagnostic procedures done worldwide in nuclear medicine centre are performed with ^{99m}Tc . There are several methods [1, 2, 3, 4, 5] for routine separation of ^{99m}Tc from ^{99}Mo , namely, alumina column chromatography technique based on the elution of ^{99m}Tc from high specific activity ^{99}Mo obtained by thermal fission of ^{235}U , the zirconium molybdate gel column chromatography technique based on the elution of ^{99m}Tc from the medium specific activity $(n,\gamma)^{99}\text{Mo}$ and solvent extraction technique based on extraction of ^{99m}Tc with methyl ethyl ketone (MEK) followed by removal of MEK from low-medium specific activity $(n,\gamma)^{99}\text{Mo}$. Currently the solvent extraction generators for the separation of ^{99m}Tc from ^{99}Mo produced by neutron activation of ^{98}Mo is achieved by manual solvent extraction with MEK in most of the hospitals in India and other developing countries. Though it is being practiced, but the method is not desirable in hospital set up as the MEK being inflammable solvent, the evaporation of MEK by heating is hazardous and environmentally

polluting. Not only is there the requirement of additional facilities such as fume hood and trained and skilled technicians, which may not always be practically feasible for hospitals but the process is cumbersome as well. There is also the possibility of bacterial contamination in the product and radiation exposure to the operating technicians.

To solve the abovementioned problems, an automated closed cyclic module for separation and recovery of various isotopes, radioactive or non-radioactive, using solvent extraction technique, and in particular, for separation and recovery of ^{99m}Tc from low-medium specific activity ^{99}Mo obtained in research reactor has been indigenously developed jointly by VECC and BRIT, Regional Centre, Kolkata. The module may also be used for separation of ^{99m}Tc produced in cyclotron. Its principle of working, scope and advantages are explained in the following sections with a discussion of the process chemistry as well.

PROCESS CHEMISTRY

The generator system is based on the selective extraction of pertechnetate ($^{99m}\text{TcO}_4^-$) in MEK from aqueous alkaline $(n,\gamma)\text{Na}_2^{99}\text{MoO}_4$ solution, subsequent purification of the organic phase by passing through an alumina column to remove traces of Mo, alkali etc. and careful evaporation of the organic phase. The residue obtained is reconstituted in physiological saline (10 ml), purified through an on-line $0.22\mu\text{m}$ membrane filter to obtain pharmaceutical grade ^{99m}Tc and collected in a vacuum vial.

AUTOMATION OVERVIEW

Scope

The process constitutes of sequential mixing, separation, evaporation and collection of various chemicals and their by-products. The mixing and directing the flow of chemicals to various parts of the system was achieved by a set of solenoid valves and a vacuum pump. By exploiting the difference in density and electrical conductivity of the organic and aqueous constituents, the phase separation was carried out online. The evaporation of the trace organic amount before the product collection was done by temperature controlled heater system set at the boiling point of the organic chemical. A clock system was designed to set the timings of each sequence of operation starting from the initial chemicals to the final product. The integrated design employing a microcontroller based embedded system with a compatible PC based GUI enabling the operator to programme and intervene the process remotely.

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INSTRUMENTATION ARCHITECTURE FOR ITER DIAGNOSTIC NEUTRAL BEAM POWER SUPPLY SYSTEM

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Abstract

A Neutral Beam (NB) Injection system is used for heating or diagnostics of the plasma in a Tokamak. The Diagnostics Neutral Beam (DNB) system for ITER (International Thermonuclear Experimental Reactor) based on acceleration of negative ions; injects a neutral (H_0) beam at 100keV with specified modulation into the plasma for charge exchange recombination spectroscopy. DNB Power Supply (DNBPS) system consists of various high voltage power supplies, high current power supplies and RF Generators. The system operates in a given operating sequence; very high electromagnetic transients are intrinsically generated during frequent short circuit at the accelerator grid (breakdowns) and sudden loss of load (Beam off).

Instrumentation is to be provided to operate the DNBPS system remotely with required control and protection in synchronisation with ITER operation as directed by CODAC (Control Data Access and Communication); the central control system for ITER. Instrumentation functionality includes 1.Operation and control of DNBPS

subsystems and associated auxiliaries 2.Protection of DNB components and power supplies using interlock system, 3.To ensure safe operation of high voltage hazardous systems 4. Acquisition of injector performance parameters and 5.To facilitate test and maintenance of individual subsystem.

This paper discusses about proposed DNBPS instrumentation architecture. The design generally follows the protocols from the ITER- Plant Control Design Handbook (PCDH).

INTRODUCTION

The DNB Power Supply system [1,2] feeds the required controllable electrical power to the DNB beam source (BS), the Residual Ion Dump (RID) and the Active Correction and Compensation coils (ACCC). The system comprises of various high voltage, High Current power supplies and RF generators for plasma generation in the ion source, with integrated controllers.

Table 1: DNBPS Main Subsystems, their control, monitoring and protection parameters

Sub Systems	Controlling parameter	Measurements	Protection events
Acceleration Grid PS (AGPS) 96kV, 75A	Voltage, Modulation	Voltage, Current, Cooling water parameters	Breakdown, Beam off, Failure in RID voltage, Short circuit at power supply end
Extractor Grid Power Supply (EGPS) 12kV, 140A	Voltage, Modulation	Voltage, Current, Cooling water parameters	Breakdown, Beam off, Short circuit at power supply end
Residual Ion Dump Power supply (RIDPS) 8kV, 60A	Voltage, Operation time	Voltage, Current, Cooling water parameters	Short circuit
RF Generators 4 X 200kW	Frequency, RF power, Modulation	Frequency, Phase, Power, Cooling water parameters	Break down, Beam off (Reduce RF power to notch level)
Active Correction Coil Power Supply (ACCPS) 1.4kV, 440A	Current	Current, Magnetic field around DNB cell, Cooling water parameters	Short circuit protection
Plasma Grid Bias Power Supply ; 30V, 600A	Current, Voltage	Current, Voltage, Cooling water parameters	Short circuit protection
Plasma Grid Filter Power Supply; 15V, 4kA	Current, Voltage	Current, Voltage, Cooling water parameters	Short circuit protection
Cs oven	Shutter control, Temperature	Temperature	-

ELECTRON CYCLOTRON RESONANCE ION SOURCE CONTROL SYSTEM

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Abstract

The ECR Ion source control system is a computer based control system. Main components of the ECR ion source are microwave generation, plasma chamber, solenoid magnets and power supplies, extraction electrodes and power supplies, beam measuring device and vacuum system (see Figure 1). All electronics devices have their built in microprocessor base electronic interface, which can be remotely accessed by serial or Ethernet link. Two Ethernet to four port serial converter are used to extend the serial port of the computer. Serial interface of all the devices are connected to the extended serial ports of the computer. A serial link of high voltage power supplies have provided optical isolation using serial to optical converter to overcome EMI and EMC problems. The software has been developed in house for remote operation of the ECR ion source.

INTRODUCTION

An ECR proton ion source has been developed for the Low Energy High Intensity Proton Accelerator (LEHIPA) [1]. The ion beam current of 42 mA (unanalyzed) has been extracted at 40 keV of beam energy. The three electrode extraction geometry has been used for ion extraction. For reliable, stable and longtime operations of the ion source it is mandatory to monitor forward and reflected microwave power, gas pressure, magnetic field and the beam parameters. The ECR ion source is sub divided in to microwave section, solenoid coil and its power supplies, high voltage power supplies, vacuum system and beam measuring device (Faraday cup). Remote operation of all section has been done using computer. Detailed control system is discussed in control system design.

CONTROL SYSTEM ARCHITECTURE

The control system of ECR ion source is computer based control system. Control system architecture is shown in Figure 2. Industrial Ethernet switch MOXA EDS208 [2] is connected to the computer. Two MOXA 5450I ethernet to 4 port serial converter is used to extend the serial port of the computer via Ethernet switch. All the five sections of ECR ion source are

Microwave Section

A 0-2 kilowatt microwave generator (magnetron) is used to feed microwave power to the plasma chamber. Microwave generator is remotely accessed via a serial

RS232 link. For monitoring of the microwave power a dual channel RF power meter is used which is also remotely accessed via serial RS232 link. Both microwave generator and RF power meter assigned their dedicated serial port which is shown in Fig. 2.

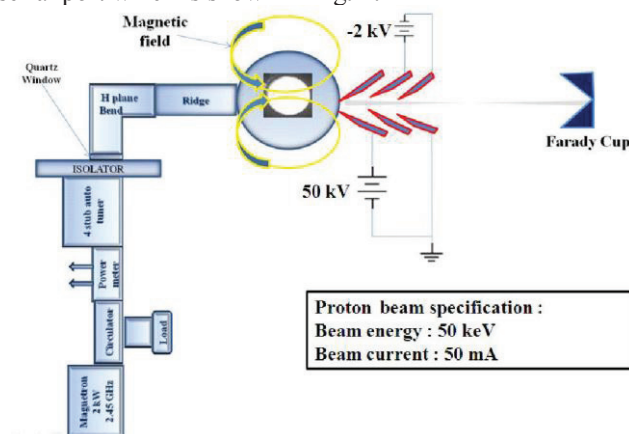


Figure 1 : ECR ion source.

Solenoid Magnet Power Supplies

For generating electron cyclotron resonance condition two solenoid coils are used to produce axial magnetic field of 832 Gauss on plasma chamber. High current power supplies of 800A, 10 V are used to supply high current in solenoid coils. Both high current power supplies are remotely accessed and have their dedicated comport.

High Voltage Power Supplies

Two high voltage power supplies rated 50 kV, 100 mA and -2kV, 100 mA are used for ion beam extraction. Both high voltage power supplies have given input power via isolation transformer to overcome ground loop problem. High voltage power supplies have remoter operation feature of 0-5 V analog input voltage type. Like 0-5 V analog input correspond to 0 – 50kV or 0 – (-2kV) V_{out}. Remote operation of HVPS is done using RS485 serial interface. Serial to optical conversion using MOXA TCF 142 has been done to provide isolation of HVPS and automation computer. An ADAM 4017+ [3] is used to provide analog output 0-5 V to HVPS. For voltage read back of 0-5V ADAM 4024 analog input module is used. Switching between remote and local mode is done using an ADAM 4068 relay module. All these ADAM modules are controlled from a single RS485 serial interface link.

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THE CS FRAMEWORK AS A CONTROL SYSTEM FOR THE HITRAP FACILITY AT GSI

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Abstract

At GSI Darmstadt the linear decelerator HITRAP is currently under commissioning. The aim is to decelerate heavy, highly charged ions up to U^{92+} , which come from the experimental storage ring (ESR) at an energy of 4 MeV/u, in several distinct steps down to less than one meV. In the end, bunches of up to 10^5 ions are captured and stored in a Penning trap from where they can be delivered to different experiments, which perform for example studies for ion-gas and ion-surface interactions, precision mass measurements, laser spectroscopy, or g-factor measurements. The low-energy part of HITRAP is controlled by an adapted version of the CS framework developed at GSI which is an object-oriented, event-driven and multithreaded framework, based on National Instruments LabVIEW 2009 and designed for small and medium size experiments. The object-oriented approach of the CS framework makes the system very flexible with respect to changes in the configuration. The DIM protocol used as communication layer makes it possible to distribute it across a large network. For HITRAP new classes were implemented in order to read out a new type of detector and to fulfil the specific needs of this facility. This paper will give a short overview about those developments.

THE HITRAP FACILITY

The HITRAP [1] project at the GSI Helmholtzzentrum für Schwerionenforschung in Darmstadt/Germany is dedicated to make heavy, highly-charged ions accessible to precision experiments. The bare U^{92+} core represents the strongest electric field which can be produced in the laboratory. Therefore experiments with such ions at rest can test a number of physical theories, like the QED with an enormous precision [2].

HITRAP is installed behind the experimental storage ring ESR and is composed of three main parts: (i) a linear deceleration stage consisting of an IH-structure and a 4-rod RFQ which decelerates the beam coming from the ESR at 4 MeV/u down to 6 keV/u, (ii) a cylindrical Penning trap to accumulate and cool down the ions via electron and resistive cooling to 4 K, and (iii) a section which transfers the cooled ions to the different experiments. A sketch of the setup is shown in Fig. 1. Parts (ii) and (iii) are controlled with a control system based on the CS framework.

The ions from the ESR reach the HITRAP facility with a repetition rate of not larger than one shot every 30 seconds. Once decelerated in the linear section they are

injected in the Penning trap where different cooling techniques are applied [3]. For beam monitoring at HITRAP in general a micro-channel plate (MCP) detector together with a phosphor screen and a CCD camera is used. These detector assemblies are mounted on a moveable feedthrough together with a faraday cup for an absolute current measurement. Because all with the setup connected devices are controllable within the control system, automated parameter scans can be performed, which improves the optimization procedure a lot.

THE CS FRAMEWORK

The CS framework [4,5] was developed at GSI/Darmstadt in order to provide a common platform for different experiments. Especially setups with a lot of ion optical elements and detectors can very easily benefit from the work already put in the CS. It is based on native LabVIEW from NI and uses object-oriented techniques in order to archive the needed flexibility for a general framework. The different objects use an event-driven mechanism to communicate with each other making it even possible to reconfigure the system on the fly. A class can for example represent a certain type of device and is used as a pattern to create objects, which are initialized with the help of a configuration database. The Data Logging and Supervisory Control (DSC) module of LabVIEW adds also an intrinsic possibility for alarming and historical trending.

Today, mainly trap experiments like SHIPTRAP [6] at GSI, ISOLTRAP [7] and WITCH [8] at CERN, TRIGATRAN [9] at the University of Mainz, LEBIT [10] at NSCL/MSU, PENTATRAN [11] at MPIK/Heidelberg, but also experiments like PHELIX [12] at GSI or Polarix [13] in Jena trigger further developments of the framework. In general, the similarities between these experiments make it easy to reuse code from one experiment at another one. This means that adding a new device to a setup is very often not linked with additional programmers work, an advantage since at many of these experiments PhD students have to maintain the control system additionally to their scientific work. Already available are classes for many different power supplies, frequency generators but also other devices such as a pulsed pattern generator on an FPGA card [14], capable of producing pulses with a precision of several ns, or a sequencer class to control the behaviour of an automated measurement.

Comparable to the situations at the other experiments, several specific add-ons had to be implemented for HITRAP.

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OVERVIEW OF CONTROL SYSTEM FOR 30MeV RF SOURCE

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Abstract

Control system for RF source of 30 MeV, 3 kW RF Linac for neutron generation is being developed. The system consists of two 15 MeV linac structures, each powered independently with klystron rated for 7.5 MW(pk)/7.5 kW(avg). Two klystron modulators of 160kV, 110A, 7 μ s and 250Hz feed pulsed power into the klystron, which produces RF power at 2856 MHz. The klystrons will be driven by low power RF driver amplifiers programmed for matching phase, frequency and power into the linac. Both the driver amplifiers are controlled through RS-232 Protocol. The HV pulsing and RF drive for the klystron has been interlocked with water flow, arc detector, SF₆ gas pressure etc. The control system is designed using Real time embedded controller, where pulses for synchronization are being generated in FPGA. Most of the power supplies like electromagnet, HVDC, etc. are on RS-232 protocol. These power supplies are controlled via suitable RS-232 to Ethernet converter. State machine topology is being used to design the logic. The database for logging data is developed in SQL. This paper describes the details of the software implementation and hardware used to realize the control of the RF power source.

INTRODUCTION

A 30MeV, 3kW Linac is being developed. The thermionic diode gun of 85 kV, 1 A based on indirectly heated LaB₆ cathode of pierce geometry will be directly coupled to the linac system, which will inject a train of pulses into the linac at the rate of 250 PRF, each having a pulse width of $\sim 7\mu$ s. The beam will be further accelerated to 30MeV by two 15MeV RF coupled cavity linac structures, each powered independently with klystron rated for 7.5MW (pk)/7.5kW (avg). The RF power at 2856MHz to the linac will be fed via a wave guide, Circulator, Dual Directional Coupler, H Bends and E Bends. Arc detector is located at the bend of the RF line to detect any arc in the RF Line. SF₆ gas at 28 psi pressure is maintained in the RF waveguide line to withstand high RF Power. A vacuum of $\sim 4 \times 10^{-7}$ torr will be maintained with the help of a turbo/sputter ion pump (TP/SIP) combination system.

SYSTEM REQUIREMENT

The major tasks to be accomplished in control system of RF Source include:

- Generation of pulses with synchronization
- Monitoring in real time mode of all the interlocks /

critical parameters like vacuum, Arc, water temperature etc

- Control / monitoring of High voltage supplies, e-gun supplies, Electromagnet power supplies, etc.
- Monitoring of RF Microwave parameters like forward power, reflected power, etc.
- Transmission of the trigger pulses through EMI prone area.
- Protection of the controller from radiated and conducted noise.
- RF phase matching between both the linacs
- Data logging of the parameters

Figure 1 shows the schematic of 30MeV RF source.

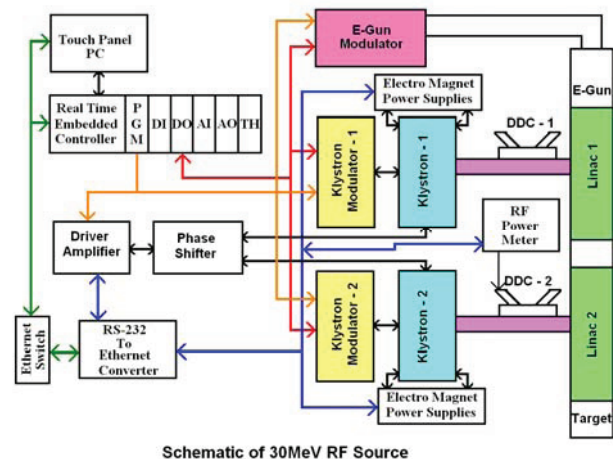


Figure 1: Schematic of 30MeV RF Source.

DESIGN ASPECTS

Hardware

The system consists of Real time embedded controller with FPGA for pulse generation logic. The controller is connected to the input output modules with 8 slot chassis. As per the requirement provision for IPGM (Pulse Generation Module) 16DI, 16DO, 8 AI, 4 AO and 4 Thermocouple channels has been given. Two 4-ports RS-232 to Ethernet converter is used for controlling RS-232 protocol devices like electromagnet power supplies, driver amplifier, RF power Meter etc.

Software

The design is based on State Machine Architecture. It gives an abstract description of the behavior of the system. This behavior is analyzed and represented in series of events that occur in one or more possible states.

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SIMULATION ANALYSIS OF ANALOG IQ BASED LLRF CONTROL OF RF CAVITY

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Abstract

This paper presents the simulation work and results in Matlab Simulink for the analogue Inphase-Quadrature (IQ) based Low Level Radio Frequency (LLRF) control of RF cavity voltage. The RF cavity chosen here is the Radio Frequency Quadrupole (RFQ) cavity in our RIB project. All the subsystems in the IQ based RF control were modelled using the Simulink blocks/components. The envelope simulation was carried out using the IQ model of RF cavity. The PI controller was properly tuned to achieve good control performance in time. The simulation graphs showing the time evolution of the RF cavity voltage with a step change of the input reference signal is presented. The simulation graphs showing the control response time needed to correct a disturbance is presented. The simulation results showing Nichols plots of the control loop and the gain and phase margin values obtained from them are presented, which are good enough for stability considerations.

INTRODUCTION

An ISOL type RIB facility is presently being developed at VECC. At present the RIB facility comprises of a RFQ (3.4m), three rebunchers and three Linacs. A schematic of the RIB facility is shown in Figure 1. The RFQ, first rebuncher, and first two Linacs operate at 37.8 MHz, while the third Linac and the other two rebunchers were designed to operate in the second harmonic at 75.8 MHz. For proper beam acceleration it is essential to regulate the RF cavity voltage at proper amplitude and phase. At present the RF cavity voltage are controlled in the conventional amplitude and phase loop control method and it is planned to upgrade the LLRF control to analog/digital IQ method.

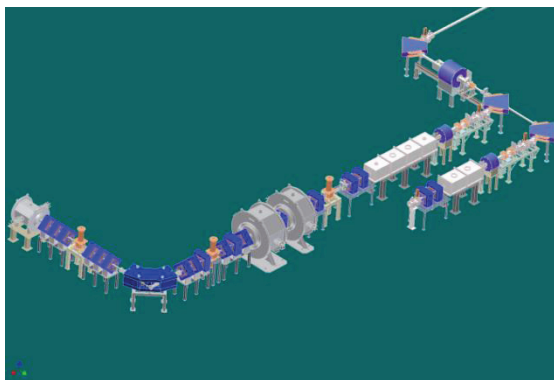


Figure 1: Schematic of RIB Facility at VECC.

In this paper the IQ based LLRF control simulation work is presented for the RFQ cavity. The advantage of RFQ is its high beam transmission efficiency for low velocity, high current beams, and the fact that a single structure is used for bunching, focusing, and acceleration of ions. Some of the important RFQ parameters are presented in Table 1.

Table 1: RFQ Parameters

Parameter	Value
Frequency	37.83 MHz
Q_o (measured)	5393
R_{sh} (measured)	42 K Ω
Input energy	1.68 keV/u
Output energy	95.7 keV/u

IQ METHOD OF LLRF CONTROL

The IQ LLRF control method is based on the principle that we can control the amplitude (A) and phase (ϕ) of a RF voltage i.e., $V = A \sin(\omega t + \phi) = (A \cos \phi) \sin \omega t + (A \sin \phi) \cos \omega t = I \sin \omega t + Q \cos \omega t$ by controlling the Inphase ($I = A \sin \phi$) and Quadrature ($Q = A \cos \phi$) components of the RF signal fed to the high power amplifier. The RF cavities are operated at a particular frequency. The advantage of this method is that I and Q components can be controlled in two paths using two set points for I and Q components. The In-Phase (I) and Quadrature (Q) signals could be obtained by passing the RF signal through a IQ demodulator device. The schematic of the analog IQ LLRF control system is shown in Figure 2.

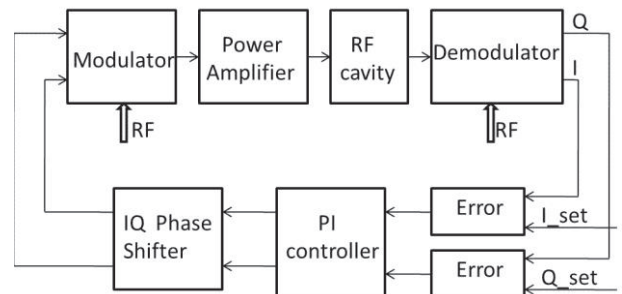


Figure 2: Schematic of analog IQ LLRF control.

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INTRODUCTION OF NON-STANDARD EPICS CONTROLLERS

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Abstract

Although EPICS is a mature software framework, the study and validation of new configurations of EPICS systems is very valuable, since new ideas open its evolution and improvement. Therefore, the goal of the present work is to introduce new technologies under EPICS control structures and test different configurations with innovative hardware in this kind of applications. Specifically, it is intended to validate the use of non-standard EPICS controllers. This paper presents a testbench using LabVIEW together with EPICS. LabVIEW eases and speeds up the development of control structures, avoids the hardware dependent developing costs and offers almost absolute compatibility with a high variety of hardware devices used in control and data acquisition. To validate its use in a real environment, is mandatory to make a study facing this solution and EPICS standard methodology, specifically CO-DAC system used in ITER. With such objective in mind, a testbench is implemented running both configurations and its results are compared. Following this scheme, as conclusions, the next step must be to implement exactly the same hardware-level structure for both approaches to improve the comparison.

INTRODUCTION

EPICS is one of the most important and widely used control systems oriented to large scientific facilities. This is a Big Physics standard based on a middleware approach, used worldwide on large scientific plants such as particle accelerators and telescopes and and it can be described as a set of open source tools, libraries and applications to create soft real-time distributed control systems. Nowadays, it offers solutions for most of the control needs and is compatible with a large variety of hardware platforms and operating systems (Linux, Windows, VxWorks...) available in the market.

Summarizing, EPICS is a mature software framework. The study and validation of new configurations valid for EPICS systems is always a very valuable research, since new ideas open its evolution and improvement. In this sense, the main objective of the work sustaining this paper is the study of the inclusion of non-standard control structures in EPICS networks. Here, the first steps towards this direction are presented. Two main schemes are considered: the standard architecture of EPICS systems using classical IOCs under Linux machines, and a system which integrates LabVIEW and EPICS. The validation of the proposed system is made by comparing their reliability to the classical scheme. The hardware setup differs as in the LabVIEW approach I/O signals are software generated instead of using

real DAQ. However, from a EPICS level view, both systems are completely analog... A testbench has been implemented for such comparing process.

The classic EPICS methodology shows a set of distributed Linux machines implementing IOCs. They are responsible for communicating EPICS with the control system tools and devices (motors, sensors, data acquisition systems, switches etc.). This approach requires the development of drivers (or equivalent mechanisms as EPICS devices) for each new device, which are the interface between EPICS records (set of process variables) and hardware (or 3rd party software). These drivers can be split into two parts: device support and driver. The first one is the interface for records and hardware independent. The second one provides low level software access to the hardware. The development of these drivers requires C language notions, EPICS knowledge (records, scan methods, Channel Access) and experience with I/O hardware (I/O registers, buses, interrupts). That means an extra effort every time a new device is added to the control structure.

The second architecture consists of using LabVIEW together with EPICS. This approach avoids the hardware dependent developing costs of the previous architecture. National Instruments (NI) hardware and software offer support for a high variety of devices and cards, and therefore, there is no need to write specific drivers. Moreover, the use of LabVIEW simplifies the development of the control structures. NI provides an EPICS server integrated in the LabVIEW solution which is based on the LabVIEW DSC module, and runs on the real time system in the PXI controller. The Real Time controller publishes EPICS PVs taking data from LabVIEW's Shared Variables. This scheme shows interesting advantages, but, before adopting this method of working, it must be validated. To do so, it is proposed to perform two parallel implementations in the testbench: the first one following the classic methodology and the other one using LabVIEW.

In the next section a thorough explanation of the two experimental setups for the validation of each proposed scheme is included, and some comments about the implementation. The last section is dedicated to the future plans for this experiment and conclusions.

EXPERIMENTAL SETUP

The experimental setup that has been developed implements a reduced local controller, which includes data acquisition, sequencing and control. The typical signals involved in a local controller are present in the emulated system. These signals will be the Process Variables (PVs) of the EPICS system. The generation of these signals can be performed by other devices such as signal generators, but,

REACHABILITY IN A FINITE DISTRIBUTED SYSTEM PROTOCOL MODEL BY BACKWARD TRAVERSAL

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Abstract

Distributed system protocol verification has the intrinsic problem in mechanizing the reasoning pattern and the resultant state space exploration. The former arises in case of theorem proving approach due to the ingenuity involved in constructing a proof and the latter is encountered in model checking approach while carrying out composition of a large number of processes that constitute a typical distributed system. A combined approach of the above two methods has been devised that eventually considers the reachability in finite distributed system protocol model. It computes the reachability in backward traversal on the fly. In this paper a C++ implementation of the on-the-fly backward traversal algorithm is reported.

INTRODUCTION

A wide class of distributed system protocols comprises a large no. of identical processes, each with an identical behaviour having finite state-space. Behaviour of each of the processes can be captured by a state transition diagram defined in terms of a FSM structure. Since a distributed system model is having a state-space of the order m^n where m is the state-space of an individual constituent process and n is the number of constituent processes which is typically few hundreds. Due to this state-space explosion [1, 2] while composing the FSMs for large number of processes, the reachability analysis suffers from large computational complexity. The framework [3] explores the merits of tableau proof framework and devises a new backward traversal algorithm to improvise a completely mechanized verification technique containing the state-space explosion problem for distributed system protocols having identical participants. In [3] the observation is made that if a flat composition can be avoided and selective composition, as and when necessary, can be computed, then the state-space explosion can be contained to a great extent. In this paper, we present a C++ implementation of the backward traversal process which basically tests on-the fly the reachability of an atomic predicate in a given distributed system protocol model.

The paper is organized in the following way: Section 2 briefly explains the C++ implementation details of the Modified Backward Traversal Algorithm followed by an example of the implementation of the Backward Traversal Algorithm in the Section 3.

A C++ IMPLEMENTATION OF THE BACKWARD TRAVERSAL FOR LEADER ELECTION PROTOCOL

Data Structure Used in the Modified Algorithm

1. Class Table - In this program, for the FSM (Finite State Machine) structure of the processes, we take the input from fsm.data file and have stored it in the class Table. The class Table contains static vector containers (dynamic lists) those store the state, transition, guard and action conditions of the transitions as state, transition, guard and action objects respectively
2. Class Network - To store the Network structure of the Distributed system, we have used class Network to store the input from the NetworkFile.data
3. Class triplet - To store the Triplet node that contains a node's information in the form, $\langle \text{EndState}, \text{Process}, \text{TransitionIndex} \rangle$ we have declared the class triplet. In the class Table, there is a static vector $\langle \text{triplet} \rangle$ Triplet list that stores all the nodes of the computational paths.
4. Class tranCont - The class tranCont stores index of two transitions (in $\text{vector} \langle \text{transition} \rangle \text{ Table::transitions}$) those are contradictory to each other. The static vector $\langle \text{tranCont} \rangle \text{ Table::TranContradiction}$ stores all the contradictory transition pairs of the system.
5. Class stateCont - The class stateCont stores index of two states (in $\text{vector} \langle \text{state} \rangle \text{ Table::states}$) those are contradictory to each other. The static vector $\langle \text{stateCont} \rangle \text{ Table::StateContradiction}$ stores all the contradictory state pairs for any process of the system.
6. Class stReachability - The class stReachability stores the lists of states of each process that has been reached so far. This helps to check if for any computational path, a process's current state contradicts with the states that had been so far reached by that process. This keeps track of the process's states so that if there is any state contradiction, then the path can be flagged as invalid.

Functional Construct of the Modified Backward Traversal Algorithm

Let ξ be the set of states where atomic predicate $\neg p_i$ holds. For each $s_j \in \xi$, construct a backward forest by invoking the functions:

1. i) `FSM * fsm = new FSM("/home/.... /fsm.data");` // Creates objects of the FSM class taking input from fsm.data file

DESIGN CONSIDERATIONS FOR DEVELOPMENT OF DISTRIBUTED DATA ACQUISITION AND CONTROL SYSTEM (DDACS) FOR RADIO-ACTIVE ION BEAM (RIB) FACILITY

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Abstract

The Radioactive Ion Beam (RIB) facility is being constructed by the Department of Atomic Energy (DAE) of India at Variable Energy Cyclotron Centre (VECC), Kolkata. The RIB facility at VECC consists of various subsystems like Electron Cyclotron Resonance Ion Source (ECR-IS), Radio Frequency Quadrupole Linear Accelerator (RFQ LINAC), Rebunchers, Inter-digital H-mode Linear Accelerators (IH LINACs) etc., which are required to produce and accelerate the energetic beam of radioactive ions for different experiments. In technical collaboration with VECC, Kolkata, a unique system called “Distributed Data Acquisition and Control System (D-DACS)” was developed. This paper is indented to bring out the design considerations in developing distributed control systems and qualification requirements with reference to functional, environmental and Electromagnetic Compatibility (EMC) standards.

RIB FACILITY – AN OVERVIEW

The RIB facility (Fig. 1) at VECC is an ISOL type RIB facility. Radioactive isotopes are first produced in a target from nuclear reaction with the primary beam. Radioactive atoms diffusing from the target are ionized initially in an integrated 1^+ ion-source and then in ECR ion-source. After mass separation, the low energy RIB is accelerated from 1.75 KeV/u to about 100 KeV/u in a RFQ LINAC. Three IH LINAC modules raise the energy up to around 415 keV/u. Subsequent LINAC modules are to be used to achieve the final beam energy of 1 to 5 MeV/u [1].

The RIB beam line is equipped with state of the art systems to produce and accelerate Radio-active Ion Beam. The major systems are broadly listed below:

- Linear Accelerators (LINACs)
- RF Quadrupole (RFQ)
- Rebunchers
- Faraday Cup, Vacuum Pump, Gate Valve systems etc., and theses beam line systems are powered with:
- Klystron High Power Amplifier (KHPA)
- High power RF Transmitters
- High voltage sources
- High current power sources

Majority of the systems used in the RIB are potential sources of Electromagnetic Interference (EMI). to meet the functional, environmental and Electromagnetic Compatibility (EMC) standards in development of systems for RIB facility need expertise on multiple domains, covering data acquisition, instrumentation and control system.

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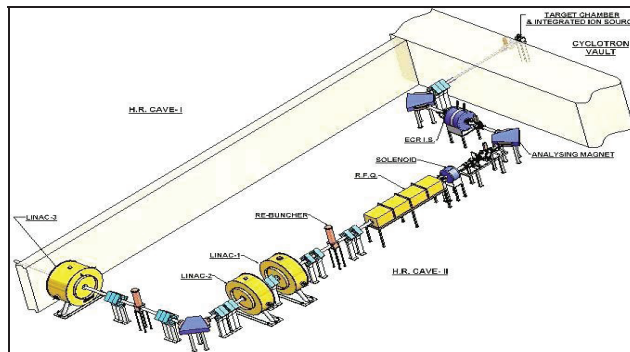


Figure 1: Layout of RIB facility with subsystems.

NEED FOR DDACS SYSTEM

The RIB facility integrates many Electronics Sub-systems procured from different international sources. Each system has its own interface for remote controlling the system parameters. Some of the systems like RF Transmitters do not have provision for remote control. Hence, the DDACS system is aimed to develop all necessary systems, sub-systems and interface circuits to monitor and control the RIB systems. The software developed for DDACS system helps an easy way of controlling the parameters at sub-system level and system level with necessary Graphical User Interface (GUI). An Embedded Controller planned at the Control Room (CR) shall control all the RIB systems and associated equipments [2].

DDACS SYSTEM DESIGN APPROACH

The RIB beam line systems and associated control parameters are shown in Fig.2. The design approaches followed are detailed below.

- The DDACS System is required to control all the equipments of RIB beam line systems and also to monitor the status of the systems continuously.
- The design is planned to support Distributed Data Acquisition considering the physical locations and number of associated RIB systems
- Entire RIB beam line systems are divided in to eight sections depending on the process flow and the equipments connected to it.
- Each section will have one Data Acquisition Front end module with all necessary interface circuits to

FPGA BASED AMPLITUDE CONTROL SYSTEM FOR ACCELERATING CAVITIES

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Abstract

The FPGA (Field Programmable Gate Array) based digital controller has been implemented for low level RF voltage control of a 650 MHz cavity. Implementing amplitude control in a compact single board solution, FPGA is chosen. The Superconducting cavity is designed to be operated at 650 MHz and 30kW, CW mode. The voltage from pick-up coil has been fed to the controller after down conversion; the signal is digitized using high speed ADCs. The controller has been simulated with different set points and gain parameters. The FPGA signal processing has been simulated according to the required strategy of the reference controller. Some simulation results have been presented for different cavity operational conditions.

BRIEF THEORY OF TRANSFER FUNCTION

Suppose the input to the cavity be an amplitude modulated (AM) signal with carrier frequency ω_c , exactly tuned to the cavity. The AM input signal is expressed mathematically as:

$$V_i = A_i[1 + a_i(t)] \cos \omega_c t$$

The output of cavity will also be an AM signal with carrier same as above and is expressed mathematically as:

$$V_o = A_o[1 + a_o(t)] \cos \omega_c t$$

On demodulating the output AM signal we will get the output baseband signal $a_o(t)$. It can be verified that the cavity action on baseband input signal $a_i(t)$ is a low pass filter whose cut-off depends upon the cavity resonant frequency and quality factor. Thus the baseband transfer function of the cavity model can be expressed as:

$$G(s) = \frac{a_o(s)}{a_i(s)} = \frac{1}{1 + s/\sigma}, \text{ where } \sigma = \frac{\omega_r}{2Q_L}$$

SYSTEM LEVEL IMPLEMENTATION ON FPGA

The implementation of the cavity control loop requires a modulator and demodulator along with a controller with an external set point and gain. Figure 1 shows the system level block diagram. There are three parts in the block diagram comprising of firmware, RF cavity and the portion that implemented outside the FPGA. The components outside the FPGA firmware are the ADC-DAC add-on modules, PC running the software and the RF cavity system.

The control loop parameters like set-point, gain and loop control action are controlled by the user through an

RS232 serial port. Control loop implemented using FPGA firmware and a proportional controller at the current stage as in Figure 2, the set-point is compared with the demodulated cavity output in FPGA, and the error data after multiplying by the gain parameter 'G', goes outside the FPGA for modulation since the DAC input is AC-coupled. The DAC output after modulation with a 5 MHz carrier goes into the cavity.

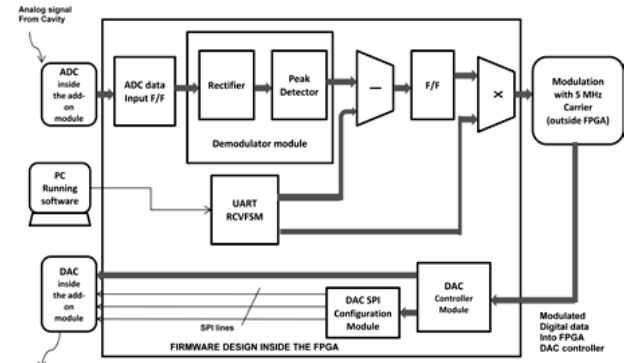


Figure 1: System level block diagram.

FPGA Hardware and Firmware Details

Hardware details: The hardware components of the implementation mainly consist of a FPGA (Virtex4) MB development board and an ADC-DAC add-on module. ADC accepts analog input of 1.8 Vpp, and outputs digital data in 2's complement format. It has a conversion delay of $17.5 \times T_{CLK}$. ADC output clock acts as the FPGA clock @ 100 MHz; DAC accepts a 16-bit digital input in 2's complement format and outputs pk-pk value of 500mV.

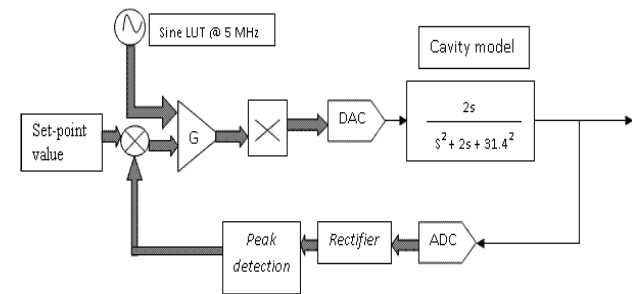


Figure 2: Block diagram of the control loop implementation using FPGA.

Firmware details: The FPGA firmware is designed to capture the high speed ADC data followed by its demodulation and then applying the digital control action.

THE NEW WHITE RABBIT BASED TIMING SYSTEM FOR THE FAIR FACILITY

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Abstract

A new timestamp and event distribution system for the upcoming FAIR facility is being developed at GSI. This timing system is based on White Rabbit (WR), which is a fully deterministic Ethernet-based network for clock and time distribution. WR is developed by CERN, GSI and other institutes as well as partners from industry based on Synchronous Ethernet and PTP [1].

The main tasks of the General Machine Timing (GMT) system are time synchronization of more than 2000 nodes with nanosecond accuracy, distribution of timing messages and subsequent generation of real-time actions (interrupts, digital signals...) by the nodes of the timing system. This allows precise real-time control of the accelerator equipment according to the beam production schedule. Furthermore the timing system must support other accelerator systems like post-mortem [2] and interlock [3]. It also provides interfaces between the accelerator control system and experiments at FAIR.

INTRODUCTION

The GMT triggers and synchronizes accelerator equipment, timed according to the accelerator cycles [4]. Cycle lengths range from 20 ms (present UNILAC), several seconds (synchrotrons SIS18 and SIS100/300) to several hours (storage rings). An important concept of the accelerator control system is the one of the so called *beam production chain*, which describes the production of a beam from an ion source through the accelerators to a target. Properties of such a beam production chain include the ion type (from protons to uranium), energy, intensity, focus and emittance at the final destination and other parameters. This is mapped to the GMT, which has an integral view on the tightly synchronized accelerators and beam transfer sections. The GMT must take into account the execution of several beam production chains in the accelerator complex at the same time. For each part of the machine, switching between different beam production chains will be possible between cycles, which implies a high degree of true parallel operation.

For all components, set values or ramp data for the different beam production chains are preloaded in the Front-End Controllers (FECs). This is done by the control system via its general purpose network. The task of the GMT is to trigger and synchronize the FECs in real-time via *timing events*, which carry additional information like machine ID or event numbers. After parameterization of the facility by the top and middle layer of the control system, it is finally the GMT which autonomously operates the accelerator complex in real-time.

Besides the GMT, the so-called Bunch phase Timing System (BuTiS) serves as a campus-wide distribution system for clock signals. BuTiS is focussed at synchronizing the radio-frequency systems of the accelerator and provides distributed and synchronized clock signals with a precision in the low picoseconds and jitter in the low femtoseconds range [5].

REQUIREMENTS

The requirements of the GMT have been described in the detailed specifications [6]. About 2000 FECs and other equipment are connected to the GMT, a distance of up to 2 km between the nodes has to be covered. In most of the cases a precision of 1 μ s is sufficient. However, some equipment like kicker magnets for transferring bunches between machines require nanosecond precision.

Besides supporting control system features like equipment triggering and synchronization, parallel execution, varying machine cycle times and scalability, other key features are the following: *Robustness* - At most one timing event per year may be lost. *Determinism* - Time critical information from must be distributed to the nodes with an upper bound latency. *Redundancy* - Core components of the GMT must be implemented with redundant equipment. *Availability* - The GMT must be capable of distributing events for testing and commissioning equipment, even when the accelerator does not produce beam. *Plan B Execution* - The GMT must react on external signals like interlock signals or malfunctioning equipment by executing predefined alternatives in the schedule. Other important features include integration of the existing machines and control system as well as interfaces to many other subsystems like the interlock system and BuTiS.

DESIGN

The main idea is to build the GMT based on the notion of absolute time. Nodes in a network share the same clock and time. By this, distribution of information and timely triggering are decoupled. This is achieved by pre-programming timing receivers for autonomous execution of actions at a given time and date.

White Rabbit as Field Bus

The new timing system for FAIR is based on a White Rabbit network. The focus of WR is on clock and timestamp distribution, thus synchronizing nodes of a network [1, 7]. WR employs Gigabit-Ethernet, IEEE1588-2008 (PTP), precise knowledge of the link delay and Synchronous Ethernet. The idea is to adjust the clock phase

STATUS REPORT, FUTURE PLANS AND MAINTENANCE ISSUES OF VME BASED CRYOGENIC CONTROL SYSTEM AT IUAC

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Abstract

The Cryogenic Data Acquisition and Control system (CRYO-DACS) at IUAC was commissioned successfully in the year 2002 and has been continuously in operation since then with uptime better than 95%. The aim of CRYO-DACS is to control and acquire many critical analogue and digital cryogenic parameters of super conducting LINAC and related equipments like beam-line cryostats, helium compressors, liquefier, cryogenic distribution line etc. from a central control room, without fail. The system monitors analog parameters like cryogenic temperature, pressure, vacuum and controls cryogenic fluid levels inside the cryostats and performs closed loop controls of cryogenic valves. The complete system is implemented using two distributed VME crates, housing I/O modules, placed far apart and interconnected using Ethernet. The entire system is still operational with a very few failure issues in last ten years due to high dust environment. The software implementation and maintenance have also been easy and trouble-free as we used some commercial software tools from m/s VMIC called IOWORKS for development. In summary, this paper will elaborate the implementation, use and related failures faced for last 10 years and the subsequent corrective actions taken to keep the system running for such a long time round the clock along with some future plans.

INTRODUCTION

The Super conducting booster linac project [1] at Inter University Accelerator Centre (IUAC) uses niobium quarter wave resonators for the acceleration of heavy ions to high energies [2]. A cryogenic facility has been setup for maintaining the above system at helium temperatures during normal operations. This facility include five beam line cryostats namely Buncher, Linac1, Linac2, Linac3 & Re-buncher, Nitrogen & Helium plants and distribution lines etc. In order to monitor, control and analyze all the above system from a central control room, the Cryogenic data Control network has been setup as shown in Fig. 1.

DEVELOPMENT TOOLS

IOWorks is a suite of PC-based software development and run-time tools for end-users and systems integrators to create affordable, scalable, and high-performance automation applications. IOWorks takes advantage of the PC platform and its wide range of supported software applications to provide an open system for automation and control environments. IOWorks board drivers are M/s VMIC (now GE) Intelligent Platform's data acquisition and control (DAQC) software driver. It is a hardware and



Figure 1: A view of Cryogenic control room at IUAC.

operating system-independent driver designed to support the widest variety of I/O in the industry.

CRYO-DACS used VMIC's Intel-based VME CPUs (VMIVME-7698) using VMIC's VMISFT-package, which consists of a set of functions and utilities to easily develop, debug, and run standard VxWorks applications that access VMIC's broad line of I/O boards.

The VMISFT supported Visual Basic, C/C++, the IOWorks Soft Logic Link, and other languages that can call functions in a dynamic link library or connect to a DDE server. C function library provided a common interface to VMIC I/O products for reading, writing, and configuring.

VME H/W of CRYO-DACS

The hardware architecture of CRYO-DACS is single-host multi-crate distributed VME with CPU (VMIVME-7698) running embedded VxWorks, all linked by workstation clients in 100 Mbps private LAN for distributed logging, historical trending, analysis, alarm management and control GUIs. The crates and modules are procured from M/s VMIC USA. The modules used are Analog inputs, Digital inputs and outputs. The AI modules used are VMIVME 3113-A & 3801 both 12 bit differential ADCs and VMIVME 2536 for digital input-outputs. The CPU used is INTEL based VMIVME 7698. Two windows PCs have been installed in the central cryogenic control room to act as development and operator consoles.

Front-end Instrumentation

To accomplish the task of low temperature measurements, each cryostat is installed with several silicon diode sensors and are connected to one or more sixteen channel temperature linearizer units which have built-in current sources and 0 to 10V dc linear outputs. Cryogenic level meters with 4-20 mA outputs for level measurements are also developed in-house. Voltage outputs are processed using VME ADCs.

DEVELOPMENT OF THE CAR-BORNE SURVEY SYSTEM KURAMA

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Abstract

We have developed a car-borne survey system named as KURAMA (Kyoto University RADiation Mapping system) for the establishment of air dose rate map in Fukushima and surrounding area as a response to the nuclear accident at TEPCO Fukushima Daiichi Nuclear Power Plant on March 11, 2011. KURAMA is developed with LabVIEW. The monitoring data tagged by GPS location data are shared with remote servers over 3G mobile network, then processed by servers for a real time plot on Google Earth and other various purposes. A CompactRIO-based KURAMA-II is developed for the autonomous operation in public vehicles. More than a hundred of KURAMA and KURAMA-II now serve for the drawing up the radiation map in the East Japan by the Ministry of Education, Culture, Sports, Science and Technology in Japan. The outline and present status of KURAMA and KURAMA-II are introduced.

INTRODUCTION

The magnitude-9 earthquake in east Japan and the following massive tsunami caused the serious nuclear disaster of Fukushima Daiichi nuclear power plant, which Japan had never experienced before. Huge amounts of radioactive isotopes were released in Fukushima and the surrounding prefectures.

In such nuclear disasters, air dose rate maps are quite important to help take measures to deal with the incident, such as assessing the radiological dose to the public, making plans for minimizing exposure to the public, or establishing procedures for environmental reclamation. The car-borne γ -ray survey technique is known to be one of the effective methods to make air dose-rate maps [1]. In this technique, a continuous radiation measurement with location data throughout the subject area is performed by one or more monitoring cars equipped with radiation detectors. Unfortunately, the existing monitoring system didn't work well in the incident. Such monitoring cars tend to be multi-functional, thus too expensive to own multiple monitoring cars in a prefecture. Fukushima was the case, and to their worse, the only monitoring car and the data center were contaminated by radioactive materials released by the hydrogen explosions of the nuclear power plant.

KURAMA was developed to overcome such difficulties in radiation surveys and for establishing air dose-rate maps during the present incident. KURAMA was designed based on consumer products, enabling a lot of in-vehicle apparatus to be prepared within a short period. KURAMA real-

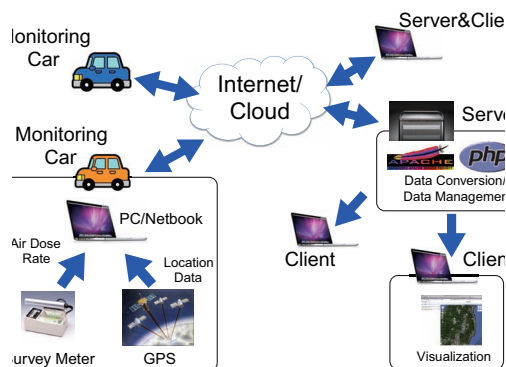


Figure 1: KURAMA system. Monitoring cars and servers are connected over the Internet by cloud technology.

izes high flexibility in the configuration of data-processing hubs or monitoring cars with the help of cloud technology. In the present paper, an outline of KURAMA as well as discussions regarding car-borne surveys performed by KURAMA are presented.

KURAMA

KURAMA is a γ -ray survey system with GPS and up-to-date network technologies developed for a primary use of car-borne surveys. A typical configuration of KURAMA is shown in Fig. 1.

An in-vehicle unit of KURAMA consists of a conventional NaI scintillation survey meter with an appropriate energy compensation, an interface box for the analog voltage output of the detector to a USB port of PC, a GPS unit, a laptop PC, and a mobile wi-fi router (Fig. 2). Its simple and compact configuration allows users to set up an in-vehicle unit in a common automobile. The software of in-vehicle part is developed with LabVIEW. The radiation data collected every three seconds is tagged by its respective location data obtained by the Global Positioning System (GPS) and stored in a csv file. The csv files updated by respective monitoring cars are simultaneously shared with remote servers by Dropbox over a 3G network, unlike other typical car-borne survey systems in which a special telemetry system or peer-to-peer radio communication is used. With this feature, the system obtains much more flexibility in the configuration and operation than other conventional car-borne systems. The radiation data is displayed in real time on Google Earth in client PCs after the dynamic generation of KML files in servers (Fig. 3).

KURAMA has served for monitoring activities in Fukushima and surrounding prefectures employed by Fukushima prefectural government and the Ministry of Ed-

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CONTROL SYSTEM FOR BARC-TIFR PELLETRON

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Abstract

BARC-TIFR Pelletron is a 14 MV tandem accelerator in operation from more than 20 years. It was having a DOS based control system software which was running on a 486 PC and it was not possible to port it on new PCs. It was based on serial highway and Uport adapter based CAMAC crate controller which are now not available and all spares were used. Hence We have changed CAMAC controller with in house developed Ethernet based CAMAC controller and new software has been developed. New Control system software is based on LINUX operating system with Graphical user interface developed using Trolltech's QT API, but can be easily ported on MS Windows.

INTRODUCTION

Pelletron is a 14 MV tandem accelerator located in TIFR, Colaba, Mumbai. It's an electrostatics accelerator which is further augmented by a superconducting booster. Both the facilities have their own control system and it was not possible to integrate both in older control system of pelletron. Control system is a tool to sense the status and to achieve the desired beam from the machine. It consists of control electronics hardware, control software and user interface. It also consists of databases to store system configuration and machine status.

Pelletron control system has been developed on LINUX operating system. LINUX is becoming very popular for particle accelerator control system, because of its stability and Open source nature [1].

SYSTEM ARCHITECTURE

A layered Architecture has been used in this system Figure 1. In a standard way control system can be partitioned in three layers presentation layer (operator interface), application layer (Server Layer/Device control unit) and resource layer (Equipment Interface Unit) [2], [3].

Equipment interface unit is the lowest level of control system which is interconnected to the accelerator equipment and sensors. In Pelletron CAMAC (Computer automated Measurement and control) is used.

Application Layer (Device control unit) provides different services to the other part of the control system like remote booting and configuration of Equipment layer and provides service to operator interface.

Operator interface unit is the layer which connects the accelerator with human and provides interaction with the machine. It consists of many displays (graphical screens, Scopes etc.) and knobs (Virtual panels and hardware knobs) for control and monitoring of the control system.

There is a communication link and communication protocol is the basis of multilayer system. Depending upon interaction between different layers it can be

categorised as centralized system or distributed system. The Pelletron control system is a centralized control system. It has three CAMAC crates which are physically distributed at three different places (Ion source room, Bottom of accelerator tank and pelletron beam HALL) and are interconnected via Ethernet LAN communicating via TCP/IP protocol suit. Though the crates are distributed at different places but still it is a centralized control system as all communication between different crates and operator user interface are possible only via a centralized

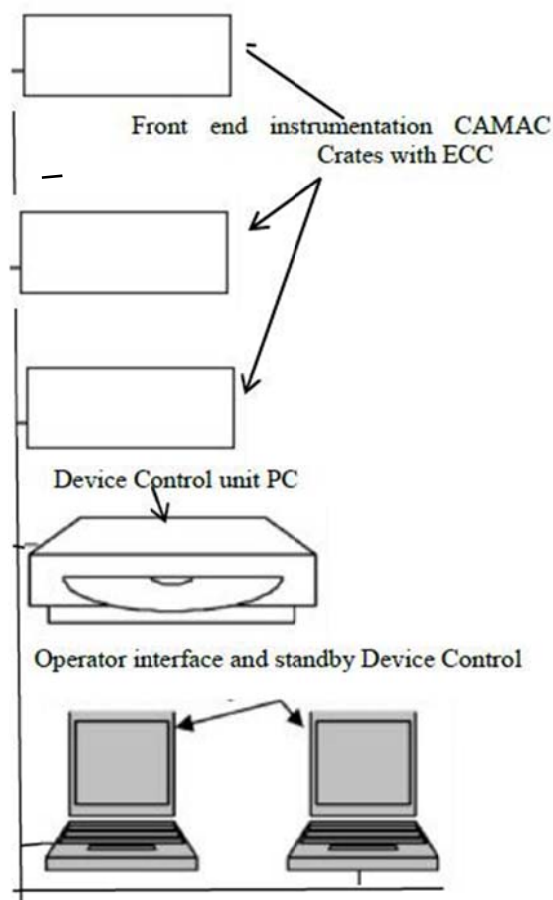


Figure 1: System Architecture.

Front End Equipment Interface Unit

CAMAC crates are the major constituent of this unit, with ADC, DAC and Digital input/output modules. Field instruments and sensors /actuators are connected to CAMAC cards. Crate Controller is having an embedded processor with CAMAC controller electronics which interacts with CAMAC modules and provides interface to the user (Device Control Unit) over 100 mbps Ethernet link. It provides connection oriented TCP server Socket interface to interact with the CAMAC system. It can be

MAINTAINING AN EFFECTIVE AND EFFICIENT CONTROL SYSTEM FOR THE ELECTROMAGNETIC CALORIMETER OF THE COMPACT MUON SOLENOID EXPERIMENT DURING LONG-TERM OPERATIONS OF CERN'S LARGE HADRON COLLIDER*

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Abstract

The sub-detectors of the Compact Muon Solenoid (CMS) multi-purpose particle detector at the CERN Large Hadron Collider (LHC) have been collecting physics data from particle collisions for almost three years. During this period, the CMS Electromagnetic Calorimeter (ECAL) Detector Control System (DCS) has contributed to the high level of availability of the experiment. This paper presents the current architecture of this distributed and heterogeneous control system alongside plans and developments for future improvements. To ensure that the system can efficiently operate and adapt to changes throughout the required operation lifetime of more than a decade, the potential legacy aspects of this kind of control system must be carefully managed. Such issues include evolving system requirements, turnover of staff members, potential benefits from new technologies and the need to follow release schedules of external software dependencies. The techniques and results of the work to continually maintain, improve and streamline the control system are presented, including the use of metrics to evaluate the impact of this effort.

INTRODUCTION

The CMS ECAL consists of three partitions: the barrel (EB), the endcaps (EE) and the preshower (ES). The EB and EE are based on lead tungstate scintillator crystals, with the generated light being measured by Avalanche Photo Diodes (APDs) and Vacuum Photo Triodes (VPTs) respectively. The ES uses reversed biased silicon sensors as the detection devices. The differing technologies of the three partitions imply specific control system needs; however there are common features such as the requirement for low voltage (LV) to power the data acquisition (DAQ) electronics and bias voltage (BV) to bias the particular type of sensor. All CMS ECAL partitions are vulnerable to overheating and require constant cooling during operation. Additionally, the humidity level of the air in the detector can provide further important information. For these reasons, the cooling systems and environmental conditions inside each of the partitions must be carefully monitored.

The prevention of damage to the detector is delegated to Programmable Logic Controller (PLC) based safety systems [1], which monitor detector conditions and can act by interlocking the powering devices and the cooling systems. The DCS monitors the same data as used by the

safety PLCs and can take pre-emptive actions before safety actions would be required. Importantly, this enables less abrupt actions to be performed, reducing risks of hardware damage and in some cases speeding up recovery to a fully operational state.

ARCHITECTURE

The CMS ECAL DCS consists of both software and hardware elements. The architecture was implemented with existing designs and technology where possible, either from commercial vendors or from high energy physics collaborations. This approach accelerated and simplified the implementation and continues to have a positive impact on the maintenance load of the system.

The role of the hardware is to host the software and to gather or send the data required to operate and monitor the detector. Currently one DELL PE2950 and 14 DELL PE1950 servers running Windows XP are used to execute the DCS software. The readout of data is performed using Ethernet and Controller Area Network (CAN) bus, according to the supported interfaces of existing hardware. In order to connect the CAN buses with the server PCs a suitable interfacing device must be chosen, with the existing solution being a CAN to USB adapter.

The BV and LV power supplies used in the CMS ECAL DCS are provided by commercial vendors together with Open Platform Communications Data Access (OPC DA) servers for monitoring and controlling the devices. The safety systems are based on Siemens PLCs and the standard S7 readout over Ethernet is used. For the remaining monitoring systems, custom electronics have been developed to read out several types of sensor inside the detector, such as the negative temperature coefficient (NTC) probes used to precisely monitor the EB and EE environmental temperature. Where possible, development of completely custom electronics was avoided by making use of the Embedded Local Monitor Board (ELMB) [2] which is an input/output electronics board equipped with a CAN transceiver. Use of the ELMB enabled a considerable simplification in the DCS electronics design.

The software layer is used to combine data from all the sources and handle it according to the requirements. This data handling includes:

- Filtering and smoothing.
- Archiving.
- Generating alarms on abnormal conditions.
- Visualisation of the data in user interfaces panels, including graphical representations and plots.

*Work supported by the Swiss National Science Foundation

DEVELOPMENT OF THE CONTROL SYSTEM FOR PEFP 100 MeV PROTON LINEAR ACCELERATOR*

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Abstract

The 100 MeV proton linear accelerator of the Proton Engineering Frontier Project (PEFP) has been developed and will be installed in Gyeongju site. After the installation, the beam commissioning of the 100 MeV linac will be performed. The PEFP is currently developing control systems including the machine control system and user interface for remote control and monitoring. The final goal of the PEFP control system is to construct a network attached, distributed control system, and a standard communication protocol among the local subsystems. In this paper, we will present the details of the distributed control system development for PEFP 100 MeV proton linac.

INTRODUCTION

Proton Engineering Frontier Project is the 100 MeV proton linac development project which was launched at 2002 as a 21st century frontier R&D program of Korean government [1, 2]. The final goals of the project are constructing a proton linear accelerator with the final energy of 100 MeV and the peak beam current of 20 mA, developing technologies for the proton beam utilizations and the accelerator applications, and promoting industrial applications with the developed technologies.

The PEFP 100 MeV proton linac consists of two parts as shown in Fig. 1. One is the low energy components including a 50 keV ion source, a low energy beam transport (LEBT), a 3 MeV radio frequency quadrupole (RFQ), and a 20 MeV drift tube linac (DTL). The other part is the high energy components including seven DTL tanks which accelerator proton beams from 20 MeV to 100 MeV. The PEFP experiment hall includes 10 beam lines, 5 for 20 MeV beams and 5 for 100 MeV beams. One of the main characteristics of PEFP beam lines is using AC magnet to distribute proton beams into 3 target rooms in both 20 MeV and 100 MeV beam lines.

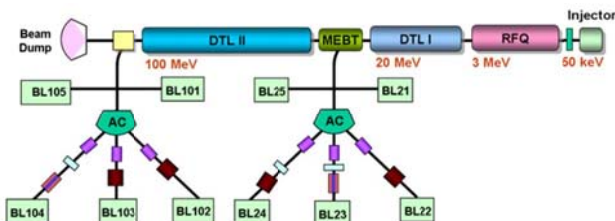


Figure 1: PEFP 100 MeV linac and extraction beam lines.

The 20 MeV linac has been successfully installed and

tested at the Daejeon site of Korea Atomic Energy Research Institute (KAERI). In this operation of the linac from 2007 to 2011, the 20 MeV linac control systems were used to control and monitor the facility for 5 years. The control system consists of ion source, vacuum, magnet power supply, and low-level RF. The 20 MeV linac control systems have been disintegrated and moved to Gyeongju site. Some of the control systems for 20 MeV linac will be expanded for 100 MeV proton linac and the control systems including vacuum, beam monitoring, and timing are upgraded. There are also many tools that can be used to make operator interface and to make an archiving system.

CONTROL SYSTEM OVERVIEW

For the networked control system, network architecture is very important as a key infrastructure which dominates total performance. Backbone switches and workgroup switches are installed as shown in Fig. 2. The remote control systems of the local devices should be connected to a local control network for Ethernet communication. Most control systems are developed with VME-based IOCs which include VME I/O boards and VME PMC boards. The integrated operation will be realized by the network connections and by the interactions among control systems.

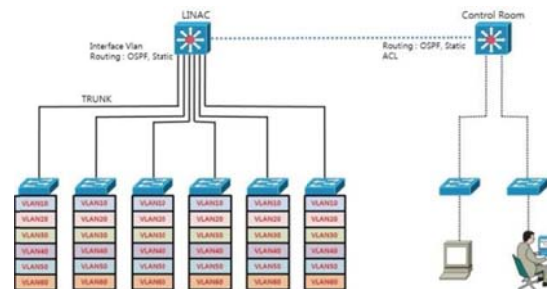


Figure 2: Schematic diagram of network architecture for PEFP 100 MeV proton linear accelerator.

The verified development tools, control infrastructure, and efficient maintenance are requirements for the PEFP software development tool. The EPICS tool provides the Channel Access (CA) communication protocol to make TCP/IP connections and transfer process variables among controllers [3, 4]. Figure 3 shows the schematic layout for the PEFP control system which is based on local control network, interlock network, and timing network. Most of communication is based on CA proton for a distributed control system.

*This work was supported by Ministry of Education, Science and Technology of the Korean government

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RF CONTROL SYSTEM FOR 400 keV RFQ

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Abstract

An RF control system has been developed for the 400 keV, 350 MHz RFQ coming up at BARC. This single cavity system consists of the functionalities of amplitude stabilization and frequency tracking for both continuous and pulsed mode of operation. The amplitude stabilization is implemented by modulating the attenuation across a fast modulator placed in the drive path. The frequency tracking is achieved by driving the FM port of a signal generator with a signal proportional to the phase shift across the resonator. The whole system is under computer control via CAMAC hardware. The paper describes the system architecture, housing & wiring of the system in a single instrumentation rack and development & testing of computer control.

INTRODUCTION

A 400 keV, 350 MHz Radio Frequency Quadrupole (RFQ) accelerator is being built at BARC, Mumbai as part of LEHIPA project. An RF control system is under development for this accelerator, which has only a single resonator, at Electronics Division, BARC [1]. The functionalities of amplitude stabilisation and frequency tracking are incorporated in the system [2]. The amplitude stabilisation is needed for a stable energy gain from the resonator. Frequency tracking system keeps the drive source-resonator system at resonance, leading to an efficient utilization of RF power to set up electric field in the resonator. Close to the resonant frequency, the phase difference between the transmitted wave and the forward wave is a sensitive indicator of the resonance condition. The system utilizes this phase difference to track the resonant frequency of the resonator by modulating the output frequency of the signal generator.

The RF control electronics is divided in a number of simple signal processing modules. This sub-division has made a number of signals available for monitoring during operation and setting up and also allowed parallel development of the hardware. These signal processing modules are under computer control via CAMAC interface.

SYSTEM DESCRIPTION

Figure 1 shows the block diagram of the overall RF control. The signal generator, operating at a constant output level, feeds RF power to the resonator via amplitude control elements. The amplitude loop compares the pick-up in the resonator with set point and generates the drive signal for the amplitude modulator. The quiescent values of the drive to the two power amplifiers used in the system can be independently set in both

amplitude and phase. For frequency tracking the resonator pick-up and the drive signal are down-converted to a convenient value of 10 MHz. The vector modulator generates the 10 MHz offset frequency required for down-conversion. The frequency loop generates the drive signal for the fm port of the signal generator by comparing the phase difference between these 10 MHz signals. The pulse generator, a part of the RF signal generator, is used for the pulsed operation of the system. All the control and monitoring signals of the amplitude and frequency loops are under computer control via CAMAC interface. The system utilises a number of functionalities available in the signal generator. These are under computer control as well. In Fig. 2 we show the control system view of the Low Level RF (LLRF) system.

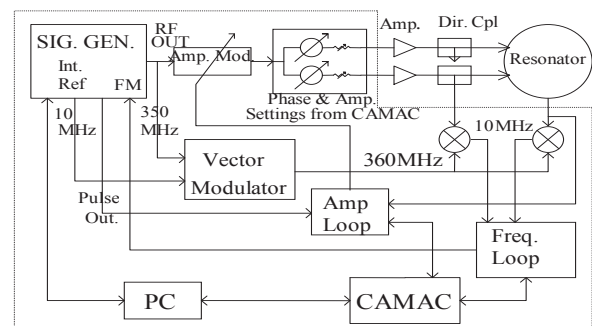


Fig. 1: RF Control System – hardware

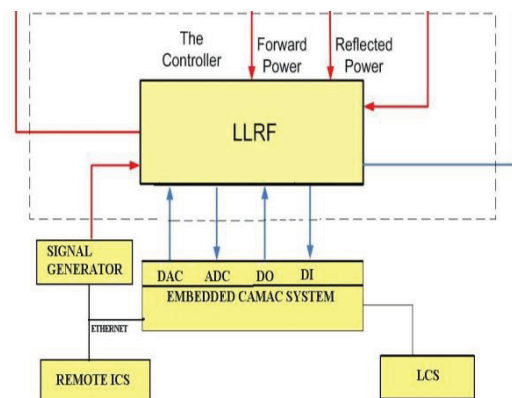


Figure 2: RF Control System – computer control.

CONTROL ARCHITECTURE

The control system is designed as 3 tier architecture as depicted in Fig 3. The OWS layer hosts the presentation applications and run manager which is used by operators

VEPP-2000 COLLIDER CONTROL SYSTEM*

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Abstract

Electron-positron collider VEPP-2000 has been commissioned at Budker Institute of Nuclear Physics. The first experiments on high energy physics has been started at the end of 2009. The paper presents architecture, implementation and functionality of hardware and software of the collider control system. The hardware of the system consists of high current main field power supplies, steering coils power supplies, pulse-elements, RF subsystems and some other special subsystems (such as vacuum, temperature, etc.). The system is based on modern industrial protocol CAN-bus and specialized electronic BINP manufactured blocks according to the standard. The paper describes implementation of different subsystems based on CANbus devices, and operating characteristics and their possibilities. Other standards and protocols like CAMAC, VME and so on also used in the system. The software according to hardware system consists of interacting subsystems responding on different acceleration facility parts. Control system software is based on several TCP/IP connected PC platforms under operating system Linux and uses client-server techniques.

VEPP-2000 PROJECT

VEPP-2000 is a new collider with luminosity up to $10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ and the beam energy up to $2 \times 1 \text{ GeV}$ [1, 2].

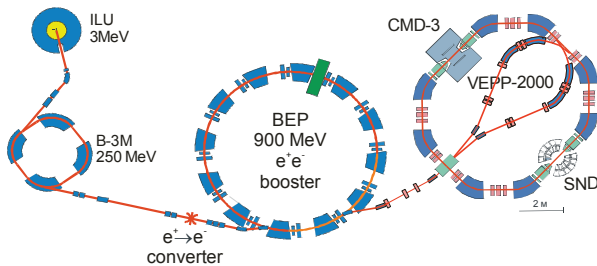


Figure 1: VEPP-2000 facility layout.

This project is a development of a previous facility of VEPP-2M which has worked at BINP over 25 years in energy range up to 1.4 GeV in c.m.s. and has collected of about 75 pb^{-1} integrated luminosity. New collider uses the existing beam production chain of accelerators: ILU – a pulsed RF cavity with a voltage of 2.5 – 3 MeV, a 250 MeV synchrotron B-3M and a booster storage ring BEP with the maximum project beam energy of 900 MeV (see Figure 1 and Table 1). The lattice of VEPP-2000 has a

two-fold symmetry with two experimental straight sections of 3m length, where Cryogenic Magnetic Detector [3] and Spherical Neutral Detector [4] are located. Two other long straights (2.5m) are designed for injection of beams and RF cavity, and 4 short technical straight sections accommodate triplets of quadrupole.

To avoid dispersion in the detectors, RF cavity and injection straights, a pair of dipoles together with the triplet in between constitute 4 achromats. Chromaticity corrections are performed by two families of sextupole magnets located in the technical straight section, where the dispersion is high.

The closed orbit steering and gradient corrections are done with 1-2% coils placed in the dipole and quadrupole magnets.

The accelerating HOM-damping RF cavity operates at the 14-th harmonic of the revolution frequency (172.0MHz). It provides for a bunch length of about 3 cm at the top energy and stability of design bunch current of 200 mA.

Beam diagnostics is based on 16 optical CCD cameras that register the synchrotron light from either end of the bending magnets and give the full information about beam positions, intensities and profiles. In addition to optical BPMs, there are also 4 pick-up stations in the technical straight sections and one current transformer as an absolute current monitor.

The magnetic field of 2.4 T in the bends is required to reach the design energy of 1 GeV in the constrained area of the experimental hall.

Table 1: VEPP-2000 Collider Main Parameters

Parameter	Value
Circumference, Π	24.39 m
Energy, E	1 GeV
Betatron functions at IP, $\beta_{x,z}^*$	10 cm
Betatron tunes, $\nu_{x,z}$	4.1, 2.1
Beam emittance, ε	$1.4 \times 10^{-7} \text{ m} \cdot \text{rad}$
Particles per beam, N	1×10^{11}
Momentum compaction, α	0.036
Synchrotron tune, ν_s	0.0035
Energy spread, $\sigma_{AE/E}$	6.4×10^{-4}
Beam-beam parameters, ξ	0.075
Luminosity, L	$10^{32} \text{ cm}^{-2} \text{ s}^{-1}$

* Work partially supported by Russian Ministry of Education and Science, basic project of BINP SB RAS 13.3.1, Physics branch of RAS project OFN.1.1.2, Scientific school NS-5207.2912.2 and Grant of the Novosibirsk region Government 2012

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DESIGN OF THE DATA ACQUISITION SYSTEM FOR THE NUCLEAR PHYSICS EXPERIMENTS AT VECC

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Abstract

The beam from K130 room temperature cyclotron is being extensively used for nuclear physics experiments for last three decades. The typical beam energy for the experiments is approximately 7-10MeV/nucleon for heavy ions and 8-20MeV/nucleon for light ions. The number of detectors used, may vary from one channel to few hundreds of detector channels. The proposed detector system for experiments with the superconducting cyclotron may have more than 1200 detector channels, and may be generating more than one million parameters per second. The VME (Versa Module Europa) and CAMAC (Computer Automated Measurement and Control) based data acquisition system (DAQ) is being used to cater the experimental needs. The current system has been designed based on various commercially available modules in NIM (Nuclear Instrumentation Module), CAMAC and VME form factor. This type of setup becomes very complicated to maintain for large number of detectors. Alternatively, the distributed DAQ system based on embedded technology is proposed. The traditional analog processing may be replaced by digital filters based FPGA (Field Programmable Gate Array) boards. This paper describes the design of current DAQ system and the status of the proposed scheme for distributed DAQ system with capability of handling heterogeneous detector systems.

INTRODUCTION

The data acquisition system at VECC (Variable Energy Cyclotron Centre) has been designed using standard commercially available hardware modules suitable for low energy nuclear physics experiments. The software has been indigenously developed at VECC for VME [1] and CAMAC [2] based system. Though the system is well proven for all the experimental needs; but the setup and management of this system for large number of detector channels becomes difficult job. The digital filter based FPGA boards may be very conveniently used instead of large number of analog modules. Different types of detector system may be used independently in the same experiment. This type of heterogeneous detector system needs a high precision time-stamping mechanism to synchronise the data.

CAMAC SYSTEM

The CAMAC is an old standard developed by ESONE (European Standards on Nuclear Electronics) committee in 1972. It is a 19" crate system with 25 slots to attach the modules. The slot 24 and 25 is used by the CAMAC crate controller. The CAMAC modules are independent functional units that can be accessed through crate

controller. The crate controller is generally interfaced with the computer through a PCI card. The Ethernet based crate controller are also available, and popularly being used for slow control of different devices. The CAMAC solution consists of a Hytec 5331 CAMAC controller with PCI interface and a Hytec 1341 List Processor.

Each CAMAC module is addressed by a group of three signals N , A and F . The N is the slot number. Each module can host sixteen sub-units; which are selected by 4-bit signal A . Each sub-unit can perform 32 functions; which are selected by 5-bit signal F . There are separate 24bit *Read* and *Write* bus. The crate controller also issues six control signals, $S1$ (strobe), $S2$ (strobe), Z (initialize), C (clear), B (busy) and I (inhibit). The CAMAC module responds with three signals; L (Look At Me, LAM), X (command status) and Q (operation status).

The typical CAMAC read cycle can be executed by the controller in 1μsec. In effect, a 24bit data read will result maximum data transfer rate of 3MB/sec. But the actual data transfer rate from the application software is determined by the software overhead. The single read takes 10μsec per word. The faster data rate is achieved by using List Processor module. This module can perform CAMAC operations as auxiliary controller and store the data in local buffer. The data is then read from the computer in block transfer. It takes average 2.14μsec for single read.

CAMAC Software

The CAMAC system is being used over decades at VECC. The CAMAC applications are built using the ESONE standard API. This makes the CAMAC system highly portable on different controller and operating systems. There are two versions of software:

- **T32:** It is the 32bit version of CAMAC developed using Windows SDK. The development life-cycle is over and only a limited support is offered for some old installations.
- **CAMACDAQ:** This is the currently supported version of the CAMAC system. It runs on both 32bit Linux and Windows machine. The software is the common framework for different DAQ hardware both VME and CAMAC system. A CAMAC crate is viewed as a single hardware module with multiple channels and inbuilt buffer. The list processor acquires the data independently from various modules inside the crate and stores them into the buffer. The software reads data from the list processor. So, the individual modules are isolated from the software perspective; thus, a wide variety of hardware modules are easily supported.

A FPGA BASED HIGH SPEED DATA ACQUISITION CARD

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Abstract

A FPGA based, high speed, two channel, analog input card with a maximum input sampling rate of 1 Giga samples per second (Gsp/s) per channel has been designed and tested. The card has got an on-board cPCI interface but has been designed in a way that it can also work as a stand-alone system. The card can function as a platform for developing and evaluating different FPGA based hardware designs. Recently, the card has been used to develop a direct sampling Low Level RF (LLRF) controller for controlling the electromagnetic fields of a prototype heavy ion RFQ. It has also been tested for acquisition of data in nuclear physics experiments. Pulses from surface barrier and silicon strip detectors were acquired at an input sampling rate of 1 Gs/s employing ^{241}Am and Am-Pu sources. The design developed for this makes use of pre-triggering. This paper discusses the functionality, salient design issues and features of the card. Finally the hardware designs of above mentioned applications related to different areas of LLRF control and nuclear pulse acquisition are explained and the results obtained are presented.

INTRODUCTION

A data acquisition system consists of a ADC driver, a programmable data processing and storage unit, and also a data transfer stage. The advent of FPGA and subsequent progress in related technology has enabled the data processing stage to be easily adapted to different applications.

The FPGA based high speed data acquisition card can function as a platform for designing and evaluating different FPGA based hardware designs. Features and design issues relevant to data acquisition are briefly presented. The card has been used to develop a LLRF controller and also has been used to acquire data in nuclear physics experiments. These applications are briefly described.

FUNCTIONALITY & SALIENT DESIGN ISSUES

The card consists of the following features:

- FPGA: VIRTEX-5 XC5VFX100T
- cPCI interface: 32 bit, 33MHz master interface with DMA transfer capability using *PCI 9054* from PLX Technology.
- Clock: 156.25 MHz clock oscillator for SFP; 40 MHz clock oscillator for PCI; 32 MHz system clock; Clock distribution for ADC and DAC.
- Rocket IO interface: Two SFP connectors are provided for SFP modules

- Memory: 2GB DDR2 – SDRAM; 256Mb flash Memory
- Analog Input: Two channels using 12 bit, 1.0 GSPS ADC: ADC12D1000 from National Semiconductor
- Configuration: JTAG Mode; Using On-board Configuration *PROM*.

Analog input data can be sampled and stored in the DDR2 memory. After the memory is filled, data transfer is done using the PCI interface in the DMA mode. The design thus involves sampling of incoming data in ADC (any one channel at a time) and acquiring the digital samples inside FPGA. The digitized data is then stored for further processing. Thus the path of data traversal is from ADC to FPGA to DDR2 to back to FPGA. Afterwards, the data can be processed at a relatively slow speed and then transferred to the PC via a cPCI interface.

The data acquisition hardware design consists of the following hardware entities:

1. Configuration and calibration of external clock synthesizer (**AD9520 -3**)
2. Configuration of ADC (**ADC12D1000**)
3. Data acquisition of digital samples within the FPGA.
4. Sample rearrangement and concatenation for writing to DDR2
5. Write operation to DDR2 memory via Memory Interface Generator (MIG) core [1].
6. Read operation from DDR2 memory via MIG core
7. Rearrangement of samples to obtain the final stream of digital samples.
8. Transferring data via cPCI interface.

The block diagram of the hardware design is shown in Figure 1.

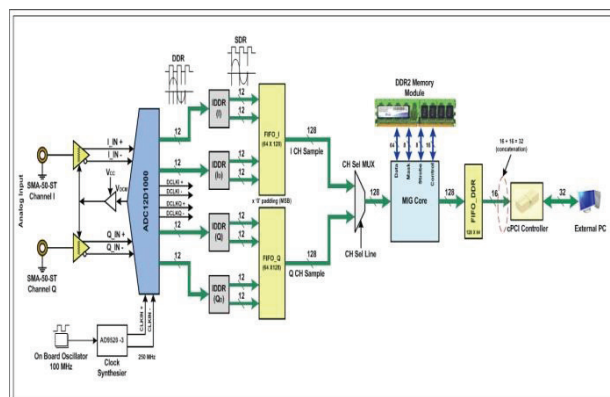


Figure 1: Hardware design for data acquisition.

DEVELOPMENT AND PERFORMANCE ANALYSIS OF EPICS CHANNEL ACCESS SERVER ON FPGA BASED SOFT-CORE PROCESSOR

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Abstract

A soft core processor is a flexible hardware description language (HDL) model of a specific processor (CPU) that can be customized for a given application and synthesized for an FPGA as opposed to a hard core processor which is fixed in silicon. Combined with an on-board ethernet port, the technology incorporates integrating the IOC and digital control hardware within a single FPGA thus reducing the overall hardware complexities of field devices. In this paper, the technical details of porting EPICS Channel Access Server on MicroBlaze soft-core processor are explained. The EPICS performance on the MicroBlaze processor is analyzed. For this, the CPU load and server processing time for different numbers of Process Variables (PVs) have been studied for this platform. On the basis of the analysis, critical parameters of EPICS on this embedded platform have been derived and a few modifications in the channel access protocol are proposed for MicroBlaze soft-core processor.

INTRODUCTION

Experimental Physics and Industrial Control System (EPICS) has been used in many accelerator laboratories to design the control system of accelerator under a unified architecture for better reliability, integrity and security of the overall control system of an accelerator.

The Input Output Controller (IOC) is the heart of an EPICS distributed control system and many such IOCs can be distributed over the control network. These IOCs are generally loaded in Personal Computers (PCs) running windows or linux operating system and placed near the field devices. Nowadays, the PC-based EPICS IOC is used in many laboratories, but it has many maintainability issues.

A soft core processor is a flexible CPU architecture that is configured in the FPGA as opposed to a hard core processor which is fixed in silicon. Combined with an on-board Ethernet port, the technology incorporates the IOC and digital control hardware within a single FPGA [1]. Nios II (by Altera), MicroBlaze (by Xilinx), OpenRISC 1200 (by OpenCores.org), LatticeMicro32 (by Lattice Semiconductors) and Cortex-M1 (by ARM Limited) are some of the soft-core processors that are targeted mainly for FPGA implementation. On the basis of various features like portability of Linux operating system, availability of FPU (Floating Point Unit) and MMU (Memory management Unit) and number of logic elements occupied, it has been seen that MicroBlaze

processor core is the most optimized target soft-core processor for our application. The use of MicroBlaze processor and the uC-linux operating system has been very successful to date [2]. Also placing the processor and the user-defined hardware on the same device does offer many benefits and better reflects the state-of-the-art in systems-on-chip [3]. Our 62.5 MHz MicroBlaze provides a great deal of processing power, the Spartan-3A FPGA provides the capability to implement a significant amount of user-logic, and the uC-linux operating system provides a good platform for software development and debugging.

The scope of this paper includes porting EPICS on FPGA based MicroBlaze soft-core processor and analyze the EPICS record processing and channel access performance on it. To achieve this, broad steps which are necessary to be performed are described in the subsequent sections.

BUILDING MICROBLAZE PROCESSOR

We have used mainly Xilinx Platform studio for building the MicroBlaze system [4] (i.e. the processor along with the peripherals and interconnects). Figure1 is the basic flow diagram representing the steps involved in building a MicroBlaze system that has been customized as per requirements in our case.

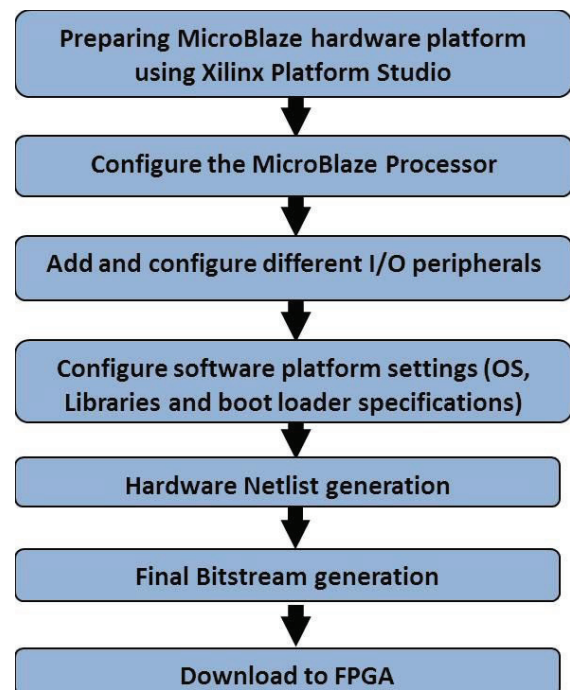


Figure 1: Flow Diagram for Building MicroBlaze System.

DIGITAL PULSE PROCESSING TECHNIQUES FOR HIGH RESOLUTION AMPLITUDE MEASUREMENT OF RADIATION DETECTOR

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Abstract

The digital pulse processing techniques for high resolution amplitude measurement of radiation detector pulse is an effective replacement of expensive and bulky analog processing as the digital domain offers higher channel density and at the same time it is cheaper. We have demonstrated a prototype digital setup with high-speed sampling ADC with sampling frequency of 80-125 MHz followed by series of IIR filters for pulse shaping in a trigger-less acquisition mode. The IIR filters, peak detection algorithm and the data write-out logic was written on VHDL and implemented on FPGA. We used CAMAC as the read out platform. In conjunction with the full hardware implementation we also used a mixed-platform with VME digitizer card with raw-sample read out using C code. The rationale behind this mixed platform is to test out various filter algorithms quickly on C and also to benchmark the performance of the chip level ADCs against the standard commercial digitizer in terms of noise or resolution. The paper describes implementation of both the methods with performance obtained in both the methods.

INTRODUCTION

In digital pulse processing technique, detector or preamplifier output signals are directly digitized and processed to extract quantities of interest. Our concern is to detect energy of the particle, which is proportional to amplitude of preamplifier output pulse. Traditional analog electronics is here replaced by programmable digital filters. Most of the typical processing features, e.g., pole-zero cancellation, baseline restoration, and shaping are digitally implemented and optimized. Costly peak sensing ADC is replaced by low cost fast ADC. It has been suggested that, typical fast AD converter should have resolution of 10–12 effective number of bits and sampling frequency 50–200 MSPS, for accurate energy measurement [1, 2]. Two digital pulse processing techniques - software based and hardware based, using such ADCs, are proposed and demonstrated for high resolution amplitude measurement of radiation detector pulse.

SOFTWARE BASED PULSE PROCESSING

In first technique of digital pulse processing, digital filters and peak detection algorithm was designed and implemented at software level. It is easy to start with such flexible system as various pulse processing features like pulse shape, shaping time, pole-zero compensation can be easily modified and tested by varying the parameters for various detector systems and various ADCs. Figure 1

shows the block diagram of software based pulse processing system.

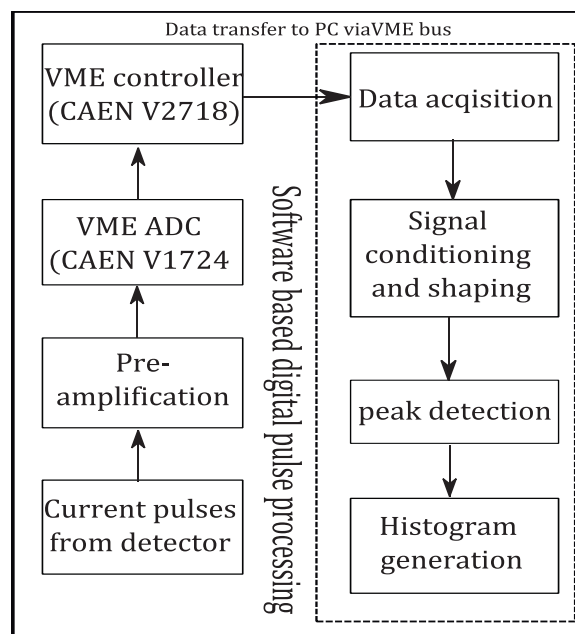


Figure 1: Software based pulse processing system.

Data is sampled by a 14 bit 100 MSPS VME ADC. The data stream is continuously written in a circular memory buffer and read via VME. The major problem of software based system is that the amount of data to readout is extremely high. It is not possible to sustain a continuous acquisition and transfer all the data to the computers. Therefore the data is acquired through block transfer mode at the cost of loss of many events. Fragmented data is discarded at the beginning and end of the block. All pulse processing features are designed at software level using 'C' programming. Codes are written to implement digital filters for CR-RC shaping of pulse, along with pole-zero compensation, whose difference equation is represented by equation 1.

$$y(n) = b_1 \times y(n-1) + b_2 \times y(n-2) + a_0 \times x(n) + a_1 \times x(n-1) + a_2 \times x(n-2) \quad (1)$$

Shaping time of filter is decided by coefficients b_1 , b_2 and pole-zero compensation depends on a_0 , a_1 and a_2 for a certain sampling frequency.

Figure 2(a) shows two overlapped preamplifier pulses at the input of digital CR-RC filter and 2(b) shows clearly resolved pulses with better SNR at the output of filter. A trigger less peak detection logic is developed to measure amplitude of filtered pulse. The peak detector logic is one

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INTRODUCING THE !CHAOS CONTROL SYSTEM FRAMEWORK

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Abstract

The analysis of most recent developments on high-performance software technologies suggests that new a design of distributed control systems (DCS) for particle accelerators and large experimental apparatuses can profit from solutions borrowed from cutting-edge Internet services. To fully profit from this new technologies the DCS model should be reconsidered, thus leading to the definition of a new paradigm. In this paper we present the conceptual design of a new control system for a particle accelerator and associated machine data acquisition system (DAQ), based on a synergic combination of a non-relational key/value database (KVDB) and network distributed object caching (DOC). The use of these technologies, to implement continuous data archiving and data distribution between components respectively, brought about the definition of a new control system concept offering a number of interesting features such as a high level of abstraction of services and components and their integration in a framework that can be seen as a comprehensive control services provider for GUI applications, front-end controllers, measurement and feedback procedures etc. The work is under development by a collaboration of INFN-LNF and INFN-Roma Tor Vergata with growing contributions from other academic and industrial partners.

THE !CHAOS FRAMEWORK

A typical example of software technology emerging from developments of Internet services is the class of non-relational databases known as key/value database. They offer an alternative to relational databases (RDMS) that is having a growing success and interest among developers of web services due to of their high throughput, scalability and flexibility. Another example are the distributed memory object caching systems. They provide in-memory key/value store for small chunks of frequently requested sets of information in order to both respond faster to requests and to distribute the load of the main server to a scalable cluster of cache servers.

These two software technologies represent the core components in the design of this new control system we named !CHAOS [1] (i.e. “not” CHAOS, where CHAOS acronym stands for Control system based on Highly Abstract Open Structure) [2, 3].

In particular, the KVDB is used by DAQ for managing what we call *history data*, while the DOC implements the service for distributing *live data* from the front-end controllers to clients, thus replacing the client/server communication.

Datasets that need to be updated are identically pushed,

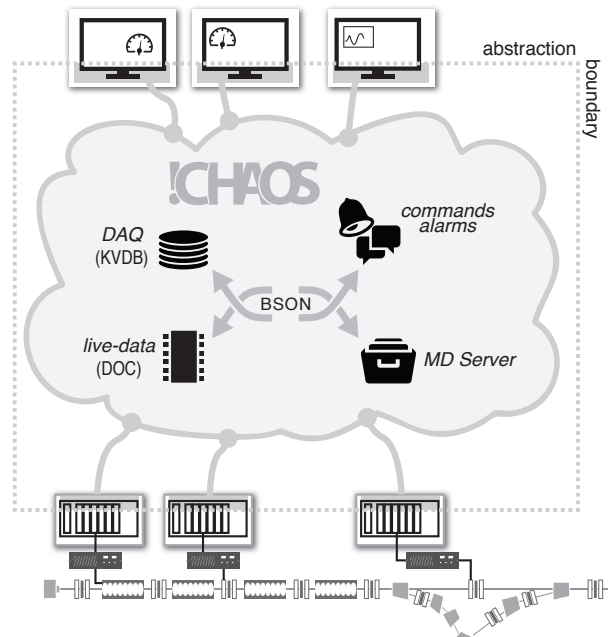


Figure 1: The “control service provider” model and the !CHAOS framework abstraction boundaries.

by front-end controllers, to both DOC and KVDB servers by issuing *set* commands. It means that data collection mechanism for DAQ is inherently included in the !CHAOS communication framework because both *live* and *history* data are pushed by the data source (the front-end controllers) to similarly distributed caching and storage systems. Moreover, since both DOC and KVDB use key/value data storage, formatting and serialization of datasets can be done once for both.

It is important noting that both the client applications and the front-end controllers are simple clients of the distributed object caching and DAQ. In particular, provided the DOC has an object container for each dataset of the DCS, defined by its unique key, a GUI client simply sends to the !CHAOS DOC service a *get* request for the object identified by that particular key, i.e. the dataset describing the associated device. On the other side the controller responsible for that device updates the correspondent dataset, according to the push rate defined for it, by issuing *set* commands to the DOC.

Data refresh rates, as well as other meta-data such as global parameters, CU configuration, commands and data syntax and semantic etc. will be managed by the meta-data server (MDS). The Meta Data Server will be also the central authority for !CHAOS components. It will keep track, for instance, of the Control Units instantiations. As su-

PROCESS CONTROL FOR PARALLEL RUN OF TWO HELIUM LIQUEFIERS AT VEC CENTRE, KOLKATA

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Abstract

Two helium liquefiers are working in tandem while one is always connected with the superconducting cyclotron at VECC. High pressure (HP) and low pressure (LP) controls are necessary to maintain varying helium flow to the cold box. Since these two liquefiers share the same HP and LP pipelines, any pressure fluctuation due to rapid change in flow sometimes causes trip of the liquefiers. To overcome this problem there is a need for fast responsive HP control. Introduction of derivative gain in the PID loop for fast action is not desirable as it creates instability to the control system. This problem was rectified by introducing a novel control scheme based on the forced opening of the unloading valve to push back helium gas to buffer tank by changing the offset of PI control as a function of Buffer Tank pressure. A simulation using Matlab Simulink was performed initially to check the performance of pressure control loop. The same is implemented in the control loop of the new liquefier and an experiment was performed. The experimental results obtained will be discussed in this paper.

INTRODUCTION

One helium liquefier is operational in VECC since 2001 [1]. The main application of this liquefier was to cater the cryoloads of the superconducting cyclotron in the form of superconducting magnet and cryopanel situated in main beam chamber for acceleration [2]. Another liquefier has been commissioned in VECC for redundancy purposes and for catering more refrigeration load [3]. Helium liquefiers are running in parallel – one running in refrigeration mode for the superconducting cyclotron and other running in liquefaction mode for supplying liquid helium to other users. The older liquefier cold box requires 50 g/s helium flow rate which is fed by either of the two cycle compressors of same capacity. The newly commissioned liquefier demands maximum 85 g/s flow rate of helium at refrigeration mode of operation. This requirement could be fulfilled either by a higher capacity compressor (85 g/s or above) or by two parallel connected compressors of lower capacity (50 g/s) as available earlier at VECC. In order to save expenditure, add reliability to the system and make use of the available compressors, a compressor of similar capacity was procured along with the new liquefier. For incorporating maximum flexibility to the cryogenic process, common warm pipelines are adopted and compressors are selected on *ad hoc* basis – one for old liquefier and two for new

liquefier [4]. On the other hand, any flow instability, e.g. emergency stop of the compressor or cold box disconnection creates pressure fluctuation, that in turn causes trip of other liquefier. The trip of the liquefier connected with the cyclotron is totally undesirable as it results in uncontrolled release of pure helium gas from the cryostat and converts a significant amount of pure helium gas to impure form. A fast responsive control is necessary to cater these types of fluctuations. A newly adopted method is discussed here both with the simulation and experimental results.

SYSTEM DESCRIPTION

Figure 1 shows the cryogenic system of the superconducting cyclotron, it has pure gas management system (buffer tanks and pure cylinder quad for low and high pressure storage respectively), Oil Removal System (ORS), pressure control loops, cold boxes of two liquefiers, helium storage Dewars, distribution box and cryoloads.

The gas management system consists of two control valves,

- one unloading valve which automatically sends excess helium inventory to the buffers when the helium gas generated is in excess compared to the refrigeration system capacity; and
- one loading valve which adds helium inventory to the system from the buffer tank when the liquefaction capacity is higher than the flow recovered from the cryomodels.

These two valves work in concert with the by-pass valve, which automatically recycles excess flow from compressor discharge to suction.

Pressure control loops play a significant role to maintain the compressor suction and delivery pressure (LP and HP respectively) so that the flow rate to one cold box is independent to the fluctuation of the other. The pressure variation from the set-point also degrades the liquefier performance.

There are few alarms in compressor and cold box control depending on the suction and delivery pressure. Each cold box is equipped with two turbo-expanders for isentropic expansion and subsequent cool down of helium gas. These turbo-expanders' operation is very sensitive to pressure, as high inlet wheel pressure, high delivery pressure, low bearing pressure, break pressure beyond safe limit may cause damage to the turbines. Therefore, every fluctuation in pressure causes stoppage of the turbo-expanders leading to the disconnection of the cold box.

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