RHIC BEAM LOSS MONITOR SYSTEM DESIGN

R. Witkover, E. Zitvogel, R. Michnoff
Brookhaven National Laboratory
Upton, NY, USA 11973

Abstract
The Beam Loss Monitor (BLM) System is designed to prevent the quenching of RHIC magnets due to beam loss, provide quantitative loss data, and the loss history in the event of a beam abort. The system uses 400 ion chambers of a modified Tevatron design. To satisfy fast (single turn) and slow (100 msec) loss beam criteria and provide sensitivity for studies measurements, a range of over 8 decades is needed. An RC pre- integrator reduces the dynamic range for a low current amplifier. This is digitized for data logging.. The output is also applied to an analog multiplier which compensates the energy dependence, extending the range of the abort comparators. High and low pass filters separate the signal to dual comparators with independent programmable trip levels. Up to 64 channels, on 8 VME boards, are controlled by a micro-controller based VME module, decoupling it from the front-end computer (FEC) for real-time operation. Results with the detectors in the RHIC Sextant Test and the electronics in the AGS-to-RHIC (AtR) transfer line will be presented.

SYSTEM DESIGN

It has been estimated that the RHIC superconducting magnets will quench for a fast loss > 2 mJ/g or a slow loss > 8 mW/g. This is equivalent to 78.3 krad/s at injection (49.3 krad/s at 100 GeV/c) for uniform loss over a single turn and 0.25 rad/s at injection (4.07 rad/s at 100 GeV/c) for slow losses. An input RC matched to the magnet thermal time constant compresses this range in a meaningful way. The amplified signal is digitized at 720 Hz by a standard RHIC VME multiplexed ADC (MADC) [1. The analog signal is also applied to high and low-pass filters preceding respective fast and slow loss comparators with independent programmable references. These can pull down the Beam Permit Link dumping the beam and halting data acquisition by the MADC. This provides a 10 second loss history preceding the abort.

Since RHIC is an accelerator storage collider some BLM parameters must be adjusted during the injection and acceleration phases. The BLM system uses predefined write lists to set gains, fast and slow loss thresholds and abort mask bits when specific RHIC Event Codes are detected.

*Work performed under the auspices of the U. S. Department of energy

The electronics, including the analog signal circuitry is packaged in VME format. A BNL designed micro-controller board manages all digital functions of the analog board independent of the crate CPU once the write list values have been set through the high level code. This insulates the real-time operations from the control system I/O functions even allowing the BLM system to continue operating during a FEC hangup. Sixty-four BLM channels will be serviced from each crate. Electronics will be located in 7 service buildings (2,4,5,7,8 10 and 12 o'clock) allowing access while beam is on.

THE DETECTOR

Ion chambers were chosen as the detectors in RHIC because they are economical, reproducible, require low maintenance and are well matched to the expected dose rates. The units were originally designed by R. Shafer for the Tevatron at FNAL [2] . For RHIC the packaging was modified, eliminating PTFE in the BNC and SHV connectors, using dual connectors to allow daisy-chaining, and isolating the BNCs to break the ground loops caused by the HV and signal cables. The ion chamber consists of a 113 cc glass tube containing argon at 725 mm Hg. The inner and outer electrodes are 0.25" and 1.5" diameter, 4" long, nickel cylinders. For the first 100 detectors the mean sensitivity was 19.6 pA/R/hr with 95% within ±1.5 pA/R/hr at 1450 V, roughly the plateau mid-point.

There are 120 detectors installed in the AGS-to-RHIC (AtR) transfer line which are independent of the RHIC Ring BLM system.[3] A total of 400 BLMs will be installed in the RHIC ring: 198 at standard quadrupoles (midway between rings), 96 at insertion region quads and dipoles, 68 at specific components in the warm regions and 38 relocatable units in the warm and insertion regions. BLMs located at cryostats are secured using 1.5"-wide stainless steel "belly-bands" to which an insulated mount is attached. In the warm regions the BLMs are typically secured to the vacuum flanges with hose clamps and similar insulated mounts.

Alternate detectors, daisy chained on two cables, each with its own HV bias supply provide redundancy. Since the electronics are accessible during operation, circuit modules or high voltage bias supplies can be readily replaced. Because the system will be used only for magnet protection and not personnel safety, higher levels of redundancy are not required.

0-7803-4376-X/98/$10.00 © 1998 IEEE

ANALOG FRONT END

The V119 Loss Monitor Analog Module contains 8 analog channels, all the data registers and the digital interface to the V118 Control Module. Mostly surface mount components were used because of the limited space. Figure 1 is a simplified schematic diagram showing one analog channel.

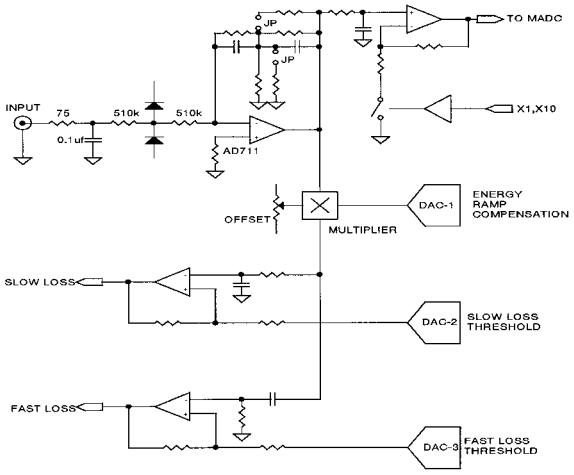

Figure 1. Simplified analog schematic.

The fast loss threshold at injection is equivalent to 5.5 mA from the detector, while the full energy , slow loss threshold corresponds to only 17.6 nA.. This wide range is reduced by pre-integrating with a 0.1 μF capacitor at the input. A low triboelectric cable, Belden 9504 was used to minimize noise. A 75Ω cable matching resistor prevents ringing while the back-to-back diodes protect the input. The capacitor rapidly charges for a fast loss. The charge is bled off through the 1.2 MΩ, matching the RHIC magnet thermal time constant. The circuit is a voltage amplifier for a fast loss, but behaves like a current amplifier for a slow loss. A "tee" configuration is used for the AD711 feedback to allow low valued resistors with reasonable roll off capacitors and to reduce thermal noise and parasitic capacitance. Two jumpers allow gains of one-tenth or 2 times greater than for the typical installation at a superconducting magnet since some monitors are not shielded by the cryostat and require less gain. Individual channel gains are recorded in the system data base. Data logging is via the MADC at 720 Hz through a programmable x1, x10 amplifier and a 360 Hz anti-aliasing filter. The slow and fast loss signals are separated by filters prior to the comparators. Each comparator derives an abort threshold reference from an associated programable 8-bit DAC. This provides sufficient settability for the storage mode, but not for the change in quench sensitivity during the magnet ramp. To compensate for this the signals to the comparators are processed by an AD734 analog multiplier which adjusts the gain as a function of magnet current in response to an event driven DAC, common to all channels on the board. The comparators incorporate hysteresis to eliminate spurious trips due to noise. All logic on the board is incorporated into an on-board ALTERA chip.

CONTROL SYSTEM INTERFACE

At each location the Loss Monitor System is housed in a standard RHIC VME chassis, including the Motorola 162 Front End Computer (FEC). Commercial digital I/O and DAC modules will be used. The standard RHIC MADC set consisting of a V113 Controller and V114 Analog Module will be housed in this chassis, along with up to 8 V119 RHIC Loss Monitor Analog Modules. The BNL designed V119 modules condition the detector outputs to 0-10 V signals for digitization and storage by the MADC for later analysis. These modules do not provide a standard VME interface: only the power pins on the VME bus are used. Registers totaling 256 bytes on the V119's are controlled by the V118 through user defined pins on the P2 connector. This P2 interface includes an 8-biy I/O bus to allow either the V118 on-board Microchip PIC16C64 microcontroller or the FEC to access the following registers on each V119 module:

- Enable/Disable Slow Loss Detection (1 bit/chan)
- Enable/Disable Fast Loss Detection (1 bit/chan)
- Slow Loss Threshold Setting (8-bit register/chan)
- Fast Loss Threshold Setting (8-bit register/chan)
- MADC Input Gain Setting (1-bit/chan)
- Loss Threshold Gain Setting (8-bit register/module)
- Slow Loss Status Latch (read only) (1-bit/chan)
- Fast Loss Status Latch (read only) (1-bit/chan)

The V118 module provides a 64k x 16 bit memory mapped to the VME space for I/O bus write lists of up to 255 address/data values for each of the 256 RHIC event codes. For each event the on-board microcontroller sequences through the associated write list, sending each data value to the specified address. This allows modification of all registers for each occurrence of a RHIC event code. An important feature of the V118 Control module is that a VME reset or FEC reboot will not affect operation of the I/O bus write list sequencing.The P2 interface includes a loss bit for each V119 module. When a trip occurs on an enabled channel, the V118 latches the loss status registers on all analog modules, allowing determination of the first loss channel. The FEC then resets the status registers allowing further trips to be detected.

TEST RESULTS

In addition to the BLMs in the AtR, 52 detectors were installed for first RHIC Sextant Test. Since the beam would make only a single pass the integrator electronics were used. The insitu noise observed was of the order of an MADC LSB (13-bit plus sign). Figure 2 shows the signal from a channel with the detector mounted in the AGS ring observing losses from the circulating gold beam with the MADC read at 100 μsec intervals.

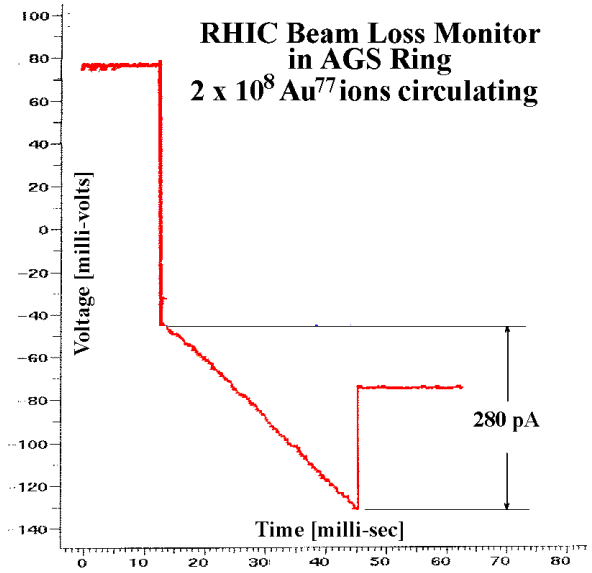

Figure 2.

During the Sextant Test the beam was purposely steered to produce losses along the RHIC magnet string. Figure 3 shows the results of the average of 2 runs normalized to 10^8 Au^{79}. The data spans the full range of the MADC. The beam direction can be determined from the asymmetry in the up and downstream loss patterns even though most detectors are mounted midway between the rings.

A VME crate containing the prototype Micro-controller, 8-channel analog module and an MADC was installed in the upstream AtR line allowing observation of slow losses due to the circulating beam in the AGS and fast extracted bunches down the AtR line. Measurements made with the low intensity gold beam verified the design bandwidth and sensitivity**.** Excessive noise was found to be coming from the 12 V crate switcher power supply, but chokes on the power supply lines reduced this considerably. The signals observed on the analog output were consistent with an LSB of the MADC. Noise at the input to the Slow Trip comparator circuit was also within an LSB of the threshold DAC, however, the Fast Trip circuit 30 kHz bandpass filter allowed noise equivalent to several LSBs to come through. This included residual switcher noise of the same order as thermal noise from the first stage

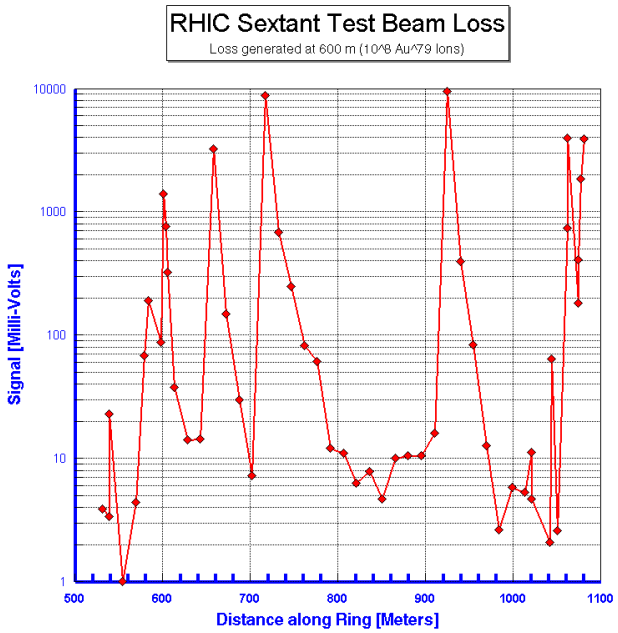

Figure 3.

resistors. The circuit will be redesigned using smaller resistor values to decrease the thermal noise to meet the 1 LSB requirement. Better power supply filtering or on-board DC-DC converters are being studied to eliminate the observed power supply noise.

ACKNOWLEDGEMENTS

The high level coding for the workstations and system commissioning was done by Dejan Trbojevic for the AtR tests and Pat Thompson for the First Sextant test. Barry Clay was a major contributor to the analog design and testing. Paul Ziminski did most of the detector testing.

REFERENCES

[1] R. Michnoff, "The RHIC General Purpose Multiplexed Analog-to-Digital Converter System", Proc. 1995 Particle Accel. Conf. 95CH35843, p2229

[2] R. E. Shafer, et al, "The Tevatron Beam Position and Beam Loss Monitoring Systems", Proc. 12th Int'l Conf on High-Energy Accel., Aug 1983, p609

[3] T. Shea, R. Witkover, R. Connelly, P. Cameron, W. Ryan, G. Smith, E. Zitvogel," Performance of the RHIC Injection Line Instrumentation Systems", These procedings.