# AN RF SYSTEM FOR A COMPACT SYNCHROTRON*

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*Abstract*

A 17.4 m circumference 200 MeV proton synchrotron, the Cooler Injector Synchrotron (CIS), is being commissioned at the Indiana University Cyclotron Facility. The compact synchrotron will be used as the injector for the electron-cooled IUCF Cooler Synchrotron. The RF system design uses digital signal processing (DSP) to directly modulate a digital rf synthesizer for beam feedback control. A wide band tunable rf cavity uses non-uniform ferrite biasing to achieve a 10:1 frequency coverage with good VSWR performance and low power requirement.

## 1 INTRODUCTION

The rf system[1] for the compact synchrotron[2] is designed to capture a 7 MeV proton beam from a two-stage linear accelerator consisting of an RFQ and a DTL or a 3 MeV proton beam directly from the RFQ. The beam from the linac injector has 425 MHz bunch structures which will coalesce into a near DC beam during the $H^-$ strip multi-turn injection. The ring rf system needs to adiabatically rebunch the beam into an $h = 1$ bucket and accelerate the beam to the desired extraction energy. The rf system supports a synchrotron cycle rate up to 5 Hz. Once the beam is bunched, the phase and radial loop beam feedback is used to suppress longitudinal phase space oscillations and to automatically center the beam orbit. For extraction, the rf system synchronizes and phase-locks the beam between the two synchrotrons to make bucket-to-bucket injection into the electron-cooled IUCF Cooler Synchrotron.

## 2 LOW LEVEL SYSTEM DESIGN

The low-level system design combines a digital signal processor with a direct digital rf synthesizer (DDS) for frequency ramp and beam feedback control. This results in a compact module that has powerful signal processing and interfacing capabilities. The DDS also has good frequency stability over the entire range of operating frequencies, making fixed intermediate frequency (IF) circuits and mixers unnecessary for the rf signal source. A block diagram of the beam control unit is shown in Figure 1.

The single-chip DDS synthesizer Analog Devices AD7008 was chosen for its good spectrum purity and high integration. A numerically controlled oscillator (NCO), a 10-bit high speed DAC, and phase and amplitude modulators have all been integrated in a single 44-pin PLCC. Our evaluation showed that the single chip integration technology achieved comparable specifications as separate NCO and DAC products.

A Motorola MC56002 digital signal processor (DSP) is used to perform the DSP functions. A variety of interface ports and interrupt capabilities of the DSP chip are also used for communication with the control computer, interfacing with the timing system, frequency ramp generation, and digital control of the rf synthesizer.

The built-in asynchronous serial port of the MC56002 down-loads commands and data directly from the control computer. The synchronization of command execution is accomplished via a hardware interrupt pin on MC56002. When a command that needs synchronization with the rest of the system, such as "start ramp" or "close loop", is received by the DSP, it is not immediately executed. Rather, the DSP waits for an appropriate interrupt signal provided by the timing system to start execution. Non-latency-critical commands (such as an operator manual change of rf frequency) are executed immediately upon reception by the DSP.

The analog interface of the beam-control module to the rf and beam parameters is via a 4-channel multiplexed 10-bit ADC. Important parameters such as the beam phase error, radial error, $\dot{B}$, etc. are processed by the DSP to generate feedback corrections to the frequency ramp-vectors. The beam feedback control is a digital implementation of "DC coupled VCO phase loop with radial correction."[3] The combined control loop transfer functions are designed to achieve a beam response of:

$$\frac{\phi_b}{\phi_r} = \frac{1}{1+\tau s} \tag{1}$$

where $\phi_b$ is the beam phase, $\phi_r$ the rf phase, and $\tau$ a time constant determined by the gain ratio between the phase and radial loops. It is desirable to set $\tau$ such that it is much greater than the synchrotron period. Rf and dipole magnet transients are thus filtered by the low-pass transfer function and the beam moves adiabatically in the phase space[3].

The entire control and signal processing software is stored in a 32 kB flash EEPROM that can be updated in-circuit quickly. The rf synthesizer, DSP and the multiplexed ADC are all housed in a single NIM module, making maintenance and repair relatively simple.

During the ramp, the rf synthesizer is guided by the frequency versus time ramp-vectors defined by the operator. Because of the fast computation speed of the DSP, it is possible to perform "real time" function synthesis, i.e., the actual frequency values are computed in real-time by the DSP during the ramp by an interpolation algorithm instead

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of being looked up from a memory based table. Only the end points of the ramp-vectors are down-loaded and stored in the DSP memory. The total length of frequency samples is thus essentially not limited by the DSP memory. With beam feedback, the interpolated frequency value is digitally corrected by the beam feedback loop using digitally processed beam radial and phase errors.

The binary input format of AD7008 DDS is preferred because it is native to the calculations of the DSP. However, a binary synthesizer requires a special binary clock to keep the output frequency increments in integers. For AD7008, the synthesizer output frequency is determined by:

$$f = \frac{\Delta\phi \times f_{clk}}{2^{32}} \text{ (Hz)} \qquad (2)$$

where $f$ is the synthesizer output frequency, $\Delta\phi$ an integer determining the synthesizer phase advance in a reference clock period, and $f_{clk}$ the reference clock frequency in Hz.

A voltage controlled crystal oscillator (VCXO) is used to generate a $2^{25}$ Hz clock that is locked to the 10 MHz laboratory time base. The phase locked loop uses a second binary DDS as a fractional frequency scaler.

Extraction for CIS is designed with a period of constant "flat top" dipole field at 1 Hz operation mode. Bucket-to-bucket synchronization between the two synchrotrons is accomplished by replacing the beam radial feedback loop with an rf phase locked loop between the two rf systems. At higher operation rates without a field "flat top" period, phase matching can be achieved by precise frequency control of the DDS just before extraction, steering the injector synchrotron rf phase toward that of the Cooler. To sequentially inject the Cooler Synchrotron rf buckets which operate at a harmonic five times the rf frequency of the CIS fundamental harmonic, a modulo-5 digital circuit is used to divide the Cooler rf reference to the same frequency as the CIS rf. For each extraction, the digital logic momentarily switches to modulo-6 and switches back to modulo-5, delaying exactly one Cooler rf bucket.

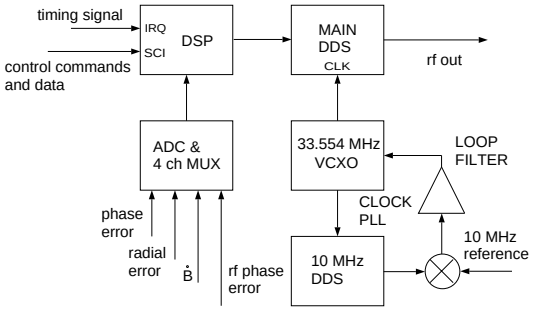


Figure 1: CIS rf source and beam control unit block diagram.

## 3 HIGH LEVEL ELECTRONICS AND RF CAVITY

A tuned ferrite cavity design is chosen for a higher gap impedance and smaller power requirement. An ENI A300 broadband amplifier can drive the cavity up to 500 V, which is more than enough to develop a required 0.015 eVs fundamental harmonic stationary or accelerating rf bucket.

The tuned cavity uses an external quadrupole biasing magnet design which places a magnet and the bias windings outside the coaxial rf resonant structure. This avoids potential rf resonances and arcing of the biasing structure, especially when there are many turns of bias windings[4]. With 40 to 50 turns on each quadrupole magnet tip coil, a compact power supply rated at 20 A can be used to achieve sufficient ampere-turns for ferrite ring biasing[5].

A common problem with driving a tuned ferrite cavity with a solid state amplifier is that it is difficult to achieve a low VSWR over a wide range of frequencies as the ferrite loss is heavily frequency dependent. In the design of this cavity, the rf $\mu$ of the ferrite rings enclosed by the driving loop is independently adjustable, varying the transformation ratio between the gap shunt impedance and the loop input impedance. This non-uniform biasing approach achieves good impedance matching of the driving loop throughout the operating band and makes the reflected rf drive power insignificant[6].

Figure 2 is a mechanical illustration of the construction of the cavity. The quarter-wave-length coaxial rf cavity consists of a perforated inner conductor, an outer conductor made of copper strips, and loading variable vacuum capacitors. 10 Phillips 8C12 ferrite rings are stacked axially with spacings. Cooling air enters the cavity between the outer conductor copper strips, flows through the surface of the ferrite rings, and exits the cavity through the holes on the inner conductor. The biasing quadrupole magnet uses 1 mm steel laminations and forms part of the rf shielding of the cavity. The laminations facing the two ferrite rings enclosed by the the driving loop are separated from the rest of the magnet by an aluminum spacer and its coils are also separate. The rf shield consisting of the magnet and aluminum lids is pressurized by a fan for air-cooling.

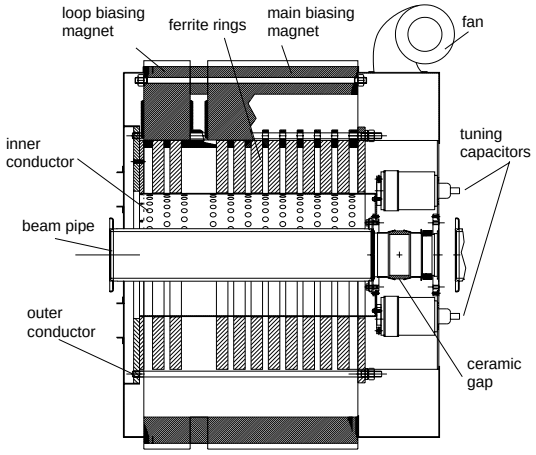


Figure 2: Rf cavity for CIS.

Figure 3 is a bias current versus frequency plot for the main and the driving loop biasing magnets for minimum

reflection ( less than 5% of driver power is reflected in most frequencies ). As the driving loop magnet current is almost always less than that of the main magnet, the two magnets can be connected in series using a single bias supply and power MOSFETs can be programmed to shunt a part of the current from the driving loop magnet to achieve good VSWR.

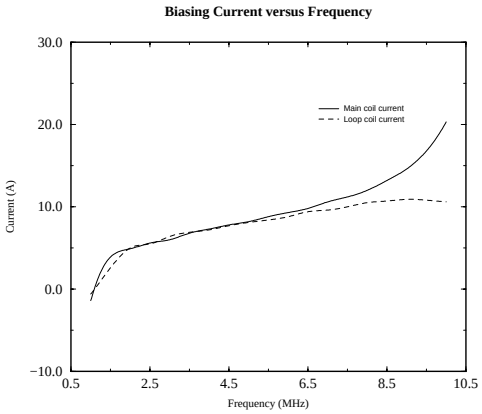


Figure 3: Biasing current versus frequency for optimum VSWR.

Figure 4 shows the shunt gap resistance of the cavity. The data were taken with 150 W of rf driving power. The loading capacitor was set at 570 pF to cover a frequency band of 1-10 MHz from zero to full bias.

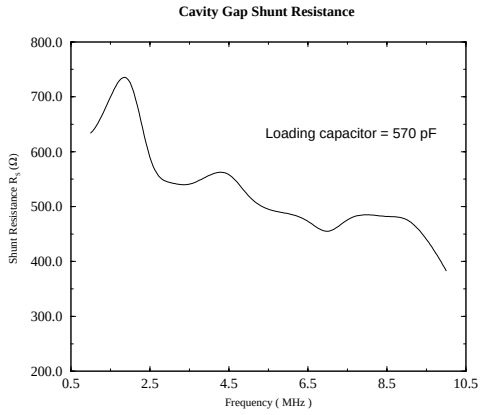


Figure 4: Measured cavity shunt resistance with 150 W driving power.

## 4 CONCLUSION

Most of the hardware for the rf system has been built and bench-tested. At the time of writing, the IUCF CIS ring has achieved bunched circulating beam with the rf cavity installed.

## 5 ACKNOWLEDGEMENTS

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