A PULSE AMPLIFIER FOR NUCLEAR INSTRUMENTATION

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Abstract

A Class-A, 1 Watt amplifier has been designed and optimized for nanosecond pulses. Spanning .01MHz to 1300Mhz, signal gain is 26dB with gain flatness of 1dB. The amplifier drives ± 10 volts across 50Ω with 350ps risetime. Each amplifier is housed in a 2-wide NIM.

Introduction

There exists a frequent need in accelerator systems to split and share fast pulse signals from various sources: stripline beam detectors, beam toroids, wall current monitors and RF clocks. To maintain reasonable signal levels and also to boost small signals, linear amplifiers are required. Although amplifiers satisfying the general requirements of nuclear instrumentation are commercially available, these devices are seldom optimal. It is not unusual, in fact, that purchased amplifiers are modified in some way prior to ever entering service.

Using standard circuits and techniques, we optimized the mechanical, electrical, thermal and RFI properties of a fast amplifier. For the described amplifier wide bandwidth was desired. The NAL Main Ring beam signals have frequency components starting at 47kHz and extending to the low microwave range. Amplifying these pulses with good fidelity requires good gain flatness. From past experience, a 1dB gain flatness specification seemed reasonable and achievable in production. In terms of power output, few wideband Class-A amplifiers provide much over two watts RF power without hybrid combining. (Few microwave power transistors will tolerate V_{CEO} much greater than 24V). Driving ±10V across 50Ω can be achieved with a single output device, and is a satisfactory signal level in a number of instrumentation systems.

Covering the intended frequency range calls for lumped circuit elements. Distributed microstrip or coax tuning elements may be used but are usually narrowband or unsatisfactory at low frequencies. Obtaining capacitors and inductors that possess textbook properties over several frequency decades involved an extensive survey of components. RF chokes were designed that maintain 1KΩ or more impedance across the band. The amplifier circuit relies on chip devices because their parasitic resonances are at very high frequencies, often above 10GHz. Chip blocking capacitors as large as 1μF were used and showed no resonances below 1.5GHz. Chip inductors might have been used, but were not. Instead, small toroids of 3E2A[1] type made excellent broadband chokes at the high end. In the power stages, large inductance and high dc current ability caused numerous resonances which were worked out.

The amplifier consists of four stages. The first two stages use Avantek's Monolithic Microwave Integrated Circuits (MSA-0420 and MSA-0470). These devices are single transistor, internally compensated amplifiers with single pole (2 GHz) frequency response. They contribute little gain/phase variation at 1300MHz. The low frequency corner is set by the required blocking capacitor and power supply choke. Latter stages employ Fujitsu FJ9200 series NPN bipolar transistors, designed for common emitter, Class-A operation. These transistors were chosen for their excellent power ability (FJ9225 34dBm), high gain (6.2dB at 1 GHz), and small size. Availability of a low capacitance emitter terminal was also essential for emitter degeneration, so an independent mounting stud, not connected to the emitter, was a prerequisite.

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Circuit Analysis

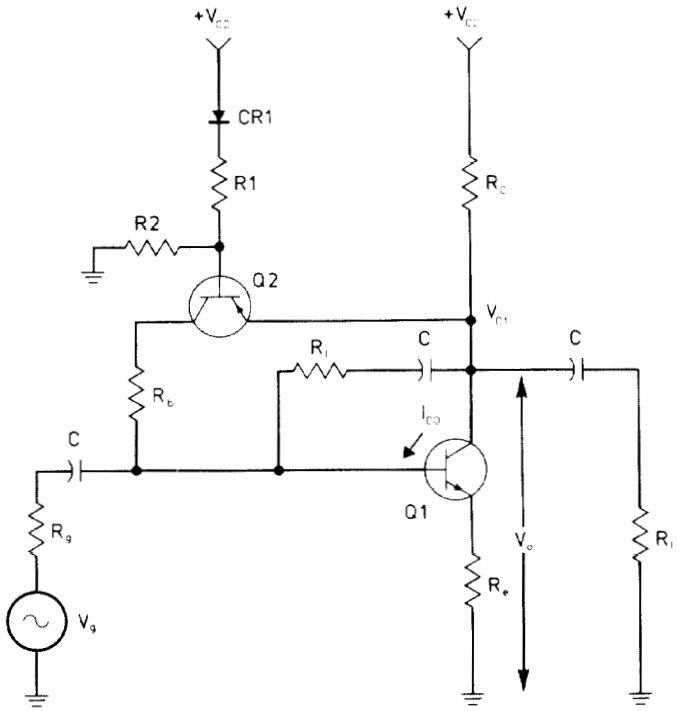

Figure 1.

Partial Schematic Diagram of Power Stages.

Figure 1 is a partial schematic diagram of the transistor amplifier power stages. Since there can be very little tuned impedance matching in the amplifier, resistors set the stage impedance and gain. Transistor ß is approximately a single pole response with the pole located at some low frequency. If the open loop transistor gain at 1.3GHz is 2, then that is the stage gain. Using the h-parameter low frequency model, three loop equations are written and solved simultaneously for R_e and R_f. Letting $h_{ie}=h_{oe}=0$ and approximating $R_e h_{fe} >> h_{ie}$:

$$R_f = \frac{A_v h_{fe} R_l (R_i + R_g)}{h_{fe} R_l - A_v (R_i + R_g - h_{ie})} \approx A_v R_i \qquad (1)$$

$$R_e = \frac{R_i - h_{ie}}{h_{fe}} + \frac{R_i R_l}{R_f} \approx \frac{R_l}{A_v} \qquad (2)$$

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For a desired input impedance R_i, stage gain $A_v = v_o/v_g$, low frequency current gain h_{fe}, and the transistor base spreading resistance h_{ie}, the feedback resistors may be calculated. With A_v=2, R_i=R_1=50Ω, R_g=0, measured values h_{ie}=4Ω and h_{fe}=45, then R_f=104Ω and R_e=25Ω. The capacitors in the circuit of Figure 1 are dc blocks, thus R_f doesn't effect transistor biasing. Collector biasing is accomplished independently by the PNP circuit.

Transistor ac characteristics are sensitive to temperature and operating point. A well designed bias circuit should maintain the chosen operating point, despite changes in V_{BE}, h_{FE}, or I_{CBO}. Resistors R_1 and R_2 are valued to set the collector current of Q_2, which is the base current of Q_1. An increase, for any reason, in the collector current of Q_1, causes lower V_{BE} in Q_2. As Q_2 shuts down, the increase in Q_1 is reversed. Q_2 may be considered a transistor amplifier in common-base configuration. It therefore has nearly unity current gain and large voltage gain. Calling the gain A and $\beta=h_{fe}$, the feedback network may be solved for I_{C1}.

$$I_{C1} = \frac{\beta A V_{CC} - \beta A V_{B2} - \beta V_{BE} + R_e(1+\beta)^2 I_{CO} + R_b(1+\beta) I_{CO}}{R_e(1+\beta) + R_b + A R_c \beta} \quad (3)$$

Thermal Stability

In power circuits where R_e and R_c are low, thermal stability becomes an important aspect of transistor design. Several bias stability factors can be considered. The factor for I_{CO} is:

$$S = \left.\frac{\partial I_{C1}}{\partial I_{CO}}\right|_{h_{FE}, V_{BE}} \approx \frac{R_e(1+\beta)^2 + R_b(1+\beta)}{R_e(1+\beta) + R_b + A R_c \beta} \quad (4)$$

Since Eqn. 4 indicates that larger gain A increases stability, an operational amplifier (of the high voltage type e.g. LM143) could effectively replace the PNP transistor. Equations 4 and 5 may be used to calculate the maximum transistor junction temperature, T_j. Eqn. 5 expresses the thermal stability requirement for transistor amplifiers.[2]

$$\frac{\partial P_C}{\partial I_C} \frac{\partial I_C}{\partial T_j} < \frac{1}{\Theta} \quad (5)$$

Θ is the junction to ambient thermal resistance and $P_C = I_C V_{CB}$. I_{CO} has the exponential dependence given by Eqn. 6[3].

$$I_{CO}(T_j) = I_{CO}(T_O)\exp\left[b\,(T_j - T_O)\right] \quad b \approx .07/°C \quad (6)$$

The stability requirement may then be written:

$$\left[V_{CC} - 2I_C(R_e + R_c)\right]\left[\frac{R_e(1+\beta)^2 + R_b(1+\beta)}{R_e(1+\beta) + R_b + A R_c \beta}\right] b I_{CO} < \frac{1}{\Theta} \quad (7)$$

Solving for T_j, Eqn. 7 prescribes a maximum junction temperature of 80°C. (V_{CC}=24V R_e=8.2Ω R_c=3.6Ω β=45 A=20 $I_{CO}(T_O)$=$I_{CBO}(T_O)$=.28mA (25°C) R_b=390Ω I_C=.38A Θ=8°C/W). The FJ9225 stud temperature measured 43°C after reaching thermal equilibrium. A junction temperature/ V_{BE} calibration could be made to measure junction temperature.

Mechanical

The 1-Watt amplifier is housed in a 6.9 in.x 2.2 in. x 2.1 in. milled aluminum enclosure, insuring low RFI, low EMI susceptibility, and good heat dissipation. Points on the stud flange of the RF transistors are grounded to the PC board by tack soldering. The studs pass through clearance holes in the PC board and the flanges are mated to smooth surfaces on the enclosure/heat sink. A surface finish of 32 μin. RMS was considered adequate and did not require special machining. The enclosure bolts to the inside surface of a 2-wide NIM front panel. The input N connector appears on the front panel. The output connector may be located either front or back. A 5.0 in. x 2.5 in. heat sink protrudes from the NIM front panel to increase heat transfer to the air.

The amplifier was originally designed as part of a larger module. Since the packaging arrangement occupies only 25% of the module volume, the remainder could be filled with additional circuits. The components used throughout are commercial grade though high quality, and the cost of a single module is about $600. Two versions of the amplifier exist; Four gain stages yield 26dB gain, three stages 20dB.

The circuit is constructed on an FR-4 printed circuit board of 12 $in.^2$. Short sections of microstrip (5 cm. total) bring the signals from the panel connectors to the active devices. Otherwise, the dielectric medium of the circuit is air. Although the FR-4 substrate is not recommended for UHF and microwave signals, dielectric loss in the microstrip sections was only .15dB at 1.3 GHz. Degradation of gain flatness was not apparent.

Summary

Eight amplifiers have been in service since Dec. 1986. At the date of this writing, one failure had been reported, which involved an overheated two-watt resistor. Table I and Figs. 2-4 document the measured performance of a typical amplifier.

TABLE I

3dB Bandwidth	.008 to 1400 Mhz
Gain	26 dB
Gain Flatness	1 dB
Noise Figure	7.5 dB
VSWR	Input < 1.4:1
	Output < 2.2:1
Reverse Isolation	>45 dB
Max. D.C. Input	±22 Volts

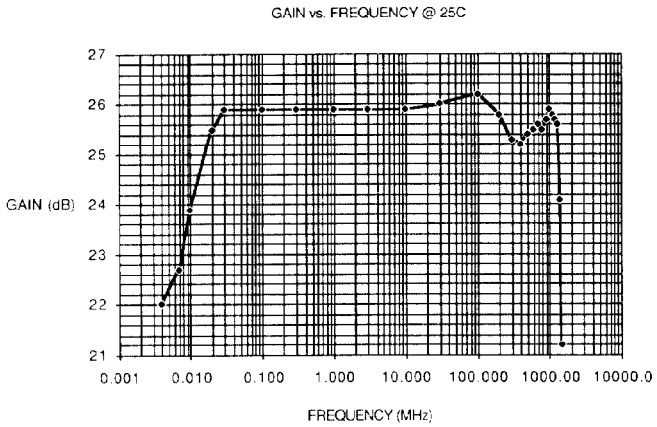

Figure 2

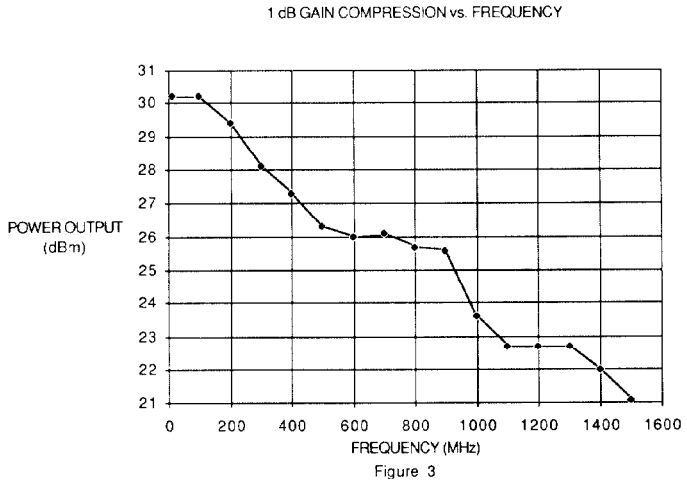

Figure 3

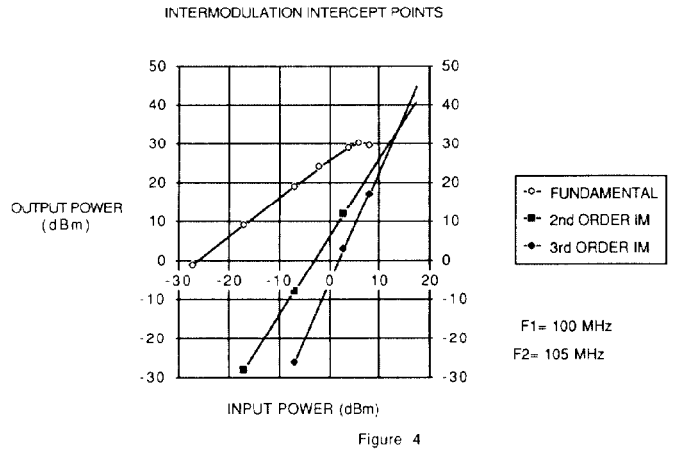

Figure 4

Acknowledgements

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