LOW-LEVEL RF SYSTEM FOR THE AGS LIGHT ION PROGRAM*

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Introduction

The new low level rf system for the light ion acceleration program features direct digital control of a phase continuous rf synthesizer clocked by finite changes in the B field. The data base is derived off line from a program[1] which resides in the microprocessor. Input parameters, such as mass and charge state, determine the correct frequency for each point. Gauss clock ticks from the main field are spaced 0.2 Gauss apart. The program will generate a digital word for each of these points if necessary. However, the digital hardware can, on command, divide the GC by 2^n. In addition to this division feature, other bits control the radial and phase loops, transition turn-on, and switching from the low frequency drive (550 kHz to 2.5 MHz) to the high frequency drive (2.5 MHz to 4.6 MHz). In all, there are 48 bits associated with each point (24 frequency bits and 24 control bits).

Corrected frequency bits are sent back to form a new data base that will be used to control the next acceleration cycle. This "learn mode" allows the system to operate open loop. Since each frequency point is clocked in by the Gauss clock, B field perturbations should (to a first approximation) not affect the acceleration. Figure 1 is a block diagram of the overall system.

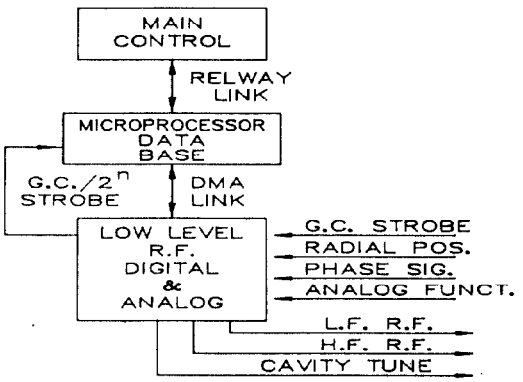

Fig. 1. Block diagram of overall system.

System Considerations

Gauss clock ticks are 0.2 Gauss apart. The corresponding frequency increments for each of these ticks at injection (0^{+8}) is about 1200 Hz. For this step change in frequency, the radial error that the beam would see is about 3.7 mm, or a phase error of about 0.8°. In order to minimize this error, an interpolation circuit was added to the system, which decreases the error by an order of magnitude.

Analog signals from the phase and radial loops have to be processed, digitized, and added to the programmed frequency. A fast A/D, arithmetic logic units, and a digital multiplier all have to be added to the circuit. The A/D should have the capability of digitizing the analog signal in less that a microsecond. Delays in the logic units and the digital multiplier should be kept to a minimum. In this way, they can be masked by the clock circuit that drives the A/D and the output latch.

The final system should also be able to retrieve each frequency point and store the corrected frequency point in the allotted time between each Gauss clock tick. Since the Gauss clock ticks are 20 μs apart, DMA transfer of the information is required.

System Description

Figure 2 is a block diagram of the system. The indicated frequencies are what one would expect to have in between each Gauss clock tick.

Latch one (L1) isolates the DMA inputs. It allows f_n to be updated in between the Gauss clock ticks ($GC/2^n$) and prevents any glitches from riding through the system. Latch two (L2) provides isolation between two consecutive frequency points. The difference in frequency is measured by an arithmetic logic unit. This difference is sent to the interpolation circuit. The bits are displaced, which effectively divides the value by 16. The other input to the interpolation multiplier comes from a counter. The input to the counter comes from another multiplier circuit which multiplies the modified Gauss clock ticks ($GC/2^n$) by 16. This counter is reset to zero at each Gauss clock count. Thus, the interpolation starts at zero and increments to the next frequency value in 1/16 steps. In the event that the delta frequency has a negative slope, the delta frequency bits and the counter bits are complemented. Now, the error starts at the maximum delta frequency and decrements down in steps of 1/16. To compensate for this delta frequency jump, another ALU subtracts out the total delta frequency during the interpolation.

The interpolation bits are added to the digitized error bits derived from the radial and phase error input. This sum in now added to the main frequency program. This corrected frequency is sent to latch four (L4) where it is retrieved at each $GC/2^n$ for storage in the "learned" data base. These same bits are also sent to the frequency synthesizer. They are moved over to effectively divide by 2 and then sent to a BIN to BCD converter. The output of the BCD is changed back to a BIN WORD format which is required for the input to the frequency synthesizer.

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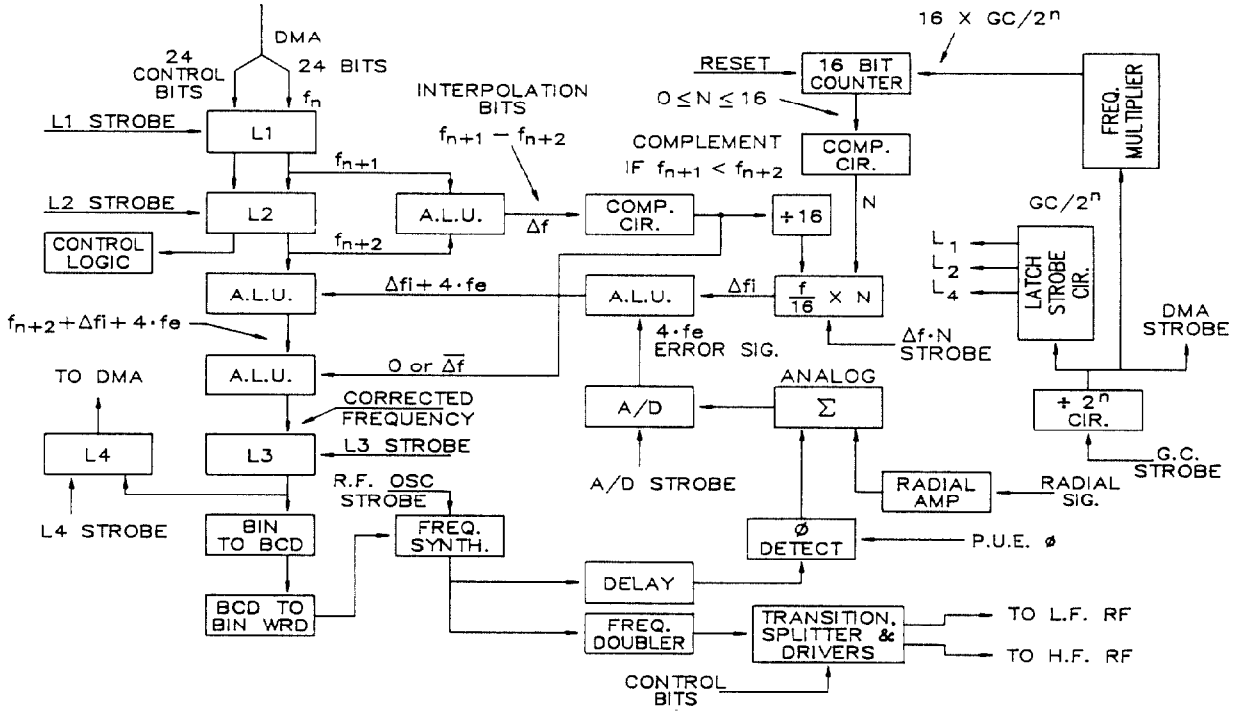

Fig. 2. Block diagram of system.

The rf output is doubled and sent to the drivers for the low frequency P.A. and high frequency P.A. Phase detection is accomplished by using a delayed signal from the frequency synthesizer and comparing it with the input from a PUE. The phase detector has a 360° range. The radial input to this system has been normalized, and its output is summed with the phase error before it is digitized. In addtion to the two error signals, another input has been provided to allow a programmed analog signal to be fed into the rf system. The summing amplifier output is sent to the A/D. The digital result is added to the interpolation bits.

System Operation and Tests

Figure 3 shows the relationship of the timing pulses to the various latches. The Gauss clock count

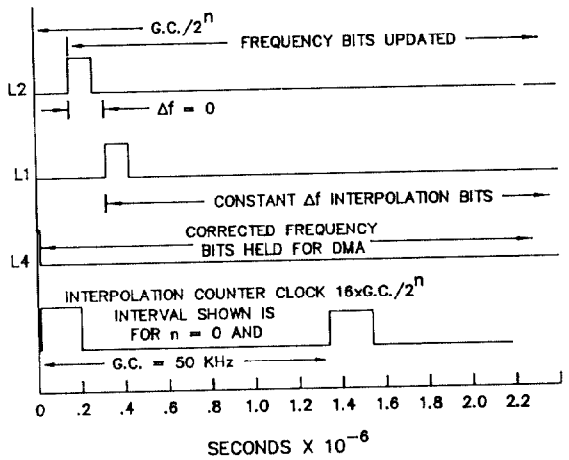

Fig. 3. Relationship of timing pulses to various latches.

that initiates these pulses is derived from a count-down circuit that allows division of the GC counts by 2^n. The initial count locks L4 and requests a DMA read cycle so the frequency information at this B field can be stored and used for the next acceleration cycle. At 150 ns after the Gauss clock count, the input bits of L2 are transferred to the output side of the latch. This causes the delta frequency to go to zero. 350 ns after the Gauss clock count, the input bits of L1 are transferred to the input side of L2. The difference in the bits between the input and output of L2 is the new delta frequency that is used in the interpolation circuit. L4 is still locked out while this is taking place. L1 and L2 have completed their timing cycles in 450 ns. The input bits to L1 can now be updated to reflect the next frequency. This update is done (via the DMA) after L4 has been read. It takes about 10 μs to complete the read cycle of L4 and about the same time to write the new bits to L1. In parallel with this latch timing circuit is another timing circuit which multiplies the frequency of the Gauss clock by 16. This is accomplished by a frequency-to-voltage converter which drives a voltage-to-frequency converter. The voltage-to-frequency converter is adjusted to multiply the Gauss clock counts by 16. These output counts are not synchronized to the Gauss clock counts, so errors of ±1/16 of delta frequency can be expected. Figure 4 compares the interpolated frequency changes to the frequency change without the interpolation circuit. For the expected delta frequency (1200 Hz) this results in an error of ±75 Hz.

L3, the A/D converter, the interpolation multiplier, and the frequency synthesizer are all clocked by a constant frequency oscillator. This was done to insure that the feedback loops were not dependent on the Gauss clock timing. At this present time, the frequency is about 735 kHz. At each clock pulse, L3 is held constant for 1.2 μs. This allows the BIN to BCD converter, the BCD to BIN WORD converter, and the frequency synthesizer to process the digital information and output the resulting rf signal. The A/D is

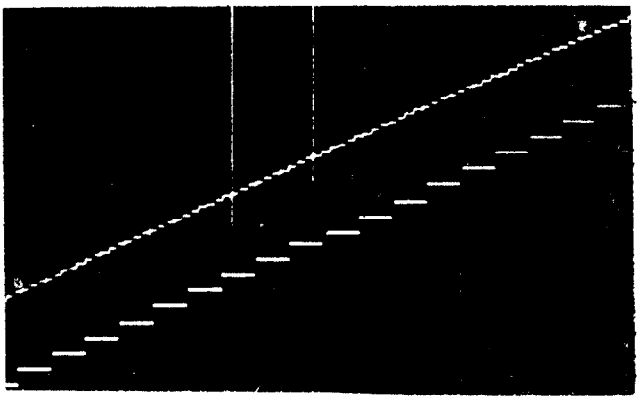

Fig. 4. Comparison of interpolated frequency changes to frequency change without interpolation circuit.

updated 1.1 μs after the initial latch trigger. During its update, the interpolation multiplier is updated. The main cause of delay in this system is the A/D clocking. Output information is delayed by 3 clock pulses, so it takes about 4 μs for phase and radial errors to be processed. By increasing the clock frequency of the A/D, this delay can be reduced to about 750 ns. The other main delay in the system is caused by the need to format the input to the frequency synthesizer and its inherent delay needed for processing the digital information. Measurements of the delay between the analog input to the A/D and the change in the rf signal indicate a delay of 7 μs. Figure 5 shows a negative DC pulse input to the A/D and the resulting change in the rf output of the synthesizer. The frequency change is from about 10 Hz to 270 kHz. Complete loops delays are now 11 μs. Figure 6 shows the phase loop response to a step

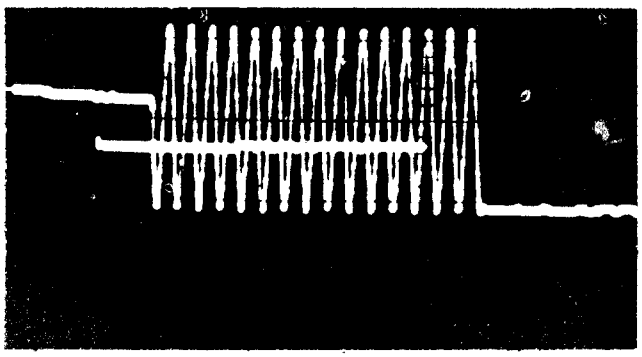

Fig. 5. Negative DC pulse input to the A/D.

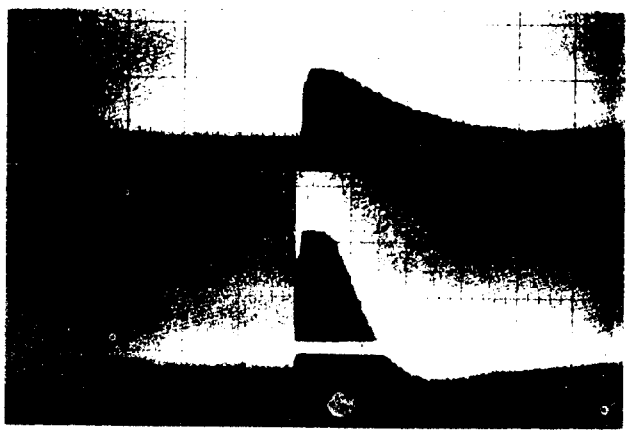

Fig. 6. Phase loop response to step change.

change of phase at the PUE (pick-up electrode) input to the phase detector. A constant frequency of 530 kHz is delayed by 230 ns (43° phase shift) at the step time. The unfiltered error signal comes back to zero in about 70 μs. At a higher gain (underdamped), the error signal returns to zero in about 36 μs with a 10% overshoot. This is at the nominal operational value of 32×10^3 rad/sec/rad which is five times the maximum synchrotron frequency ($2\pi \times 10^3$ rad/sec). Because the rf phase is not derived from the accelerating gap signal (Fig. 2), no attempt is made to compensate for the cavity time constant. Since the loop response is primarily determined by the overall time delay, any reduction of this parameter will permit increased loop gain. With the addition of a correction signal proportional to $(\dot{B}/V_{rf})$ and operational use of the learn mode, it should be possible to eliminate the radial loop. Figure 7 compares the operation of the system open- loop and closed-loop (phase-loop). The learn mode was not operational at this time.

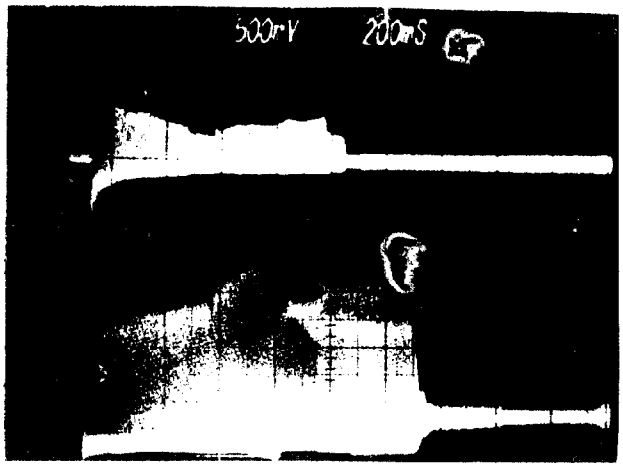

Fig. 7. Comparison of open-loop and closed-loop operation.

Comments

The system covers the complete rf frequency range and switches over from single cavity acceleration to multiple cavity acceleration with no beam loss. It also switches from the programmed drive (single cavity) to the normal bootstrap system. Detailed operational experience[2] and the high level rf power amplifier[3] are discussed in other papers of this proceedings.

Acknowledgments

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References

1. M. Livingston, J. Blewett, K. Green, and L. Haworth, Rev. Sci. Instrum. 21, 7 (1950).
2. R.K. Reece, L.A. Ahrens, D.S. Barton, D. Beavis, J. Benjamin, H. Foelsche, C. Gardner, E. Gill, S. Sidhu, P. Thieberger, "Operational Experience with Light Ions at Brookhaven National Laboratory", this proceedings.
3. R. Sanders, D. Barton, W. Frey, P. Montemurro, A. Otis, M. Plotkin, M. Pritsker, A. Soukas, J. Tuozzolo, A. Zaltsman, "A High Level, Low Frequency RF System for the Acceleration of Light Ions in the AGS", this proceedings.