POWER SUPPLY CONTROL FOR THE TRISTAN MAIN RING AND ACCUMULATION RING

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All power supplies are controlled remotely through the CAMAC interfaces which are supported by the mini-computers. The local quadrupole magnets have the individual power supply to make the experimental insertion and RF section to be dispersion-less and to allow the low betatron function operation at the colliding points. The currents of all power supplies can be remotely changed according to the input of the reference data, which are supplied from the interfacing modules in the CAMAC crates. The fine adjustment of the individual current can be also done without affecting the beam existing in the ring by the interrupting operation which transmits the reference data directly to the output port of the interfacing module from the central control room. All power supplies and magnets compose a harmonious system and are protected from the failures by the hard-wired interlocking signals.

Introduction

The electron-positron colliding accelerator, TRISTAN, is composed of the main ring (MR) with the circumference of 3018 m and the accumulation ring (AR) with that of 377 m. The electron or positron is injected into AR at 2.5 GeV from the linac, accelerated upto 7.0 GeV (8 GeV in the future) and then transferred to MR. Several cycles of AR provide MR with four bunches of electron and positron which are accelerated upto 25 GeV at present (30 GeV in the near future).

The numbers of the current circuits of the bending and quadrupole magnets are 80 for MR and 26 for AR [1]. The sextupole magnets are grouped into 6 families for MR and 4 families for AR. In addition the steering magnets and the backleg windings have the individual power supplies for the fine correction of the closed orbit distortion and the numbers of their power supplies are 520 for MR and 110 for AR. These power supplies, 606 for MR and 140 for AR, are operated synchronously through the external control modules. For synchronization the timing control system is incorporated in the control system. There are also another power supplies for the skew quadrupole and wiggler magnets which are operated asynchronously. The power supplies of the latter type have the same external control modules.

Table 1 Magnet systems of AR and MR

	AR		MR	
	No. of magnets	No. of circuits	No. of magnets	No. of circuits
Bending magnet				
Normal bend	56	1	264	1
Weak bend (4.2%)	–	–	8	1
Quadrupole magnet				
Normal cell	28	2	192	2
Local quad	58	23	200	76
Sextupole magnet				
F-type	20	2	120	3
D-type	20	2	120	3
Steering magnet				
Horizontal	10	10	56	56
Vertical	44	44	200	200
Backleg winding	56	56	264	264
Skew quadrupole	–	–	24	12
Wiggler magnet	1	1	8	4

Power supply system

Both AR and MR are the electron synchrotrons which can be operated independently. AR provides MR with a bunched beam of electron or positron which is supplied from the linac. When an accumulation of the beam in AR reaches at the pre-determined intensity, it is accelerated to the flattop energy and then transferred to MR which is waiting the beam at the same energy level. Two electron and positron bunches are injected into MR, counter-rotating each other, and then accelerated in the same ring simultaneously. When MR is running at flattop, AR is waiting at the idle state at present.

The stabilized dc power supplies have the different compositions depending on the stability requirement, rated voltage and current, etc. All power supplies are operated receiving the digital input data which is the current reference. The current stability and resolution determine the method of the current regulation and the accuracy of the reference signal. The power supplies of the main magnets, that is the bending and quadrupole magnets, adopt both current and minor voltage feedback loops and the 16 bit reference data. Whereas the power supplies of the correction magnets adopt the 12 bit data. The digital data is converted to the analogue signal with the digital-to-analogue converter (DAC) and compared with the output current for the feedback control which is measured with the dc current transformer (DCCT). The magnet systems and specifications of the power supply systems of both AR and MR are summarized in Table 1 and 2, respectively.

In MR, the power supply of the normal bending magnets is divided into four groups, each powered by the separate transformer and installed in the separate power supply house around the ring, and connected in series inserting one fourth of the bending magnets between them. One of four groups functions as a master which receives the reference data and the rest obey it. The QF (or QD) power supply has a similar constitution but two groups.

The steering magnets and backleg windings have the individual small power supplies but they are grouped together in several control units to economize the cost. Table 3 gives the summary of their power supplies.

Power supply control

The reference input data of the current wave forms to all power supplies are generated by the minicomputers and transmitted to the dual-port memory modules in

Table 2 Specifications of the power supply system

	AR			MR			
	B	QF, QD Local Q	SX	B(QF, QD)	BW	Local Q	SXD, SXF
Primary voltage (V)	3φ-6600	3φ-420	3φ-420	3φ-6600	3φ-420	3φ-420	3φ-420
Rated dc current (A)	1900	1340	100	1500(1350)	20	1500 ∿ 1700	410,440
Rated dc voltage (V)	1700	38 ∿ 170	250	4x1068(2x908)	180	47 ∿ 206	775,685
Rectification	24p-SCR	12p-SCR	12p-SCR	24p-SCR	6p-SCR	12p-SCR	12p-SCR
Current regulation	SCR pc & filter	SCR pc & trans.	SCR pc & trans.	SCR pc & filter	SCR pc & trans.	SCR pc & filter	SCR pc
Current detection	DCCT	DCCT	shunt	DCCT	DCCT	DCCT	DCCT
Current stability	$< 10^{-4}$	$< 10^{-4}$	$< 10^{-3}$	$< 10^{-4}$	$< 10^{-4}$	$< 10^{-4}$	$< 10^{-3}$
Input data (bits)	16	16	12	16	16	16	12

B = normal bend, BW = weak bend, QF, QD = normal cell quad, SX, SXD, SXF = sextupole
pc = phase control, trans. = transistor control, filter = dc filter & active filter

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Table 3 Power supplies of the steering magnets and backleg windings

	AR			MR		
	STH	STV	BLW	STH	STV	BLW
No. of circuits	10	44	56	56	200	264
Primary voltage (V)		± 200			± 210	
Rated dc current (A)		± 10		± 3	± 3	± 10
Rated dc voltage (V)		± 40		110	110	55
Rectification		diode			SCR & diode	
Current control		transistor			transistor	
Current detection		shunt			shunt	
Input signal (bits)		12			12	
Polarity		bi-polar			switched bi-polar	
No. of control units		11			8	

STH, STV = horizontal & vertical steering, BLW = backleg winding

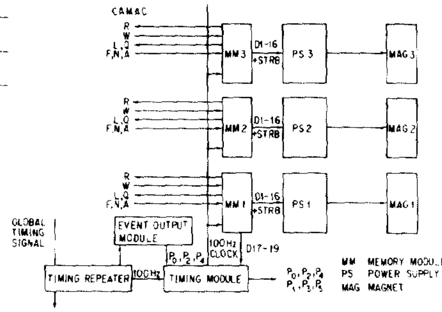

Fig. 1 Method of the power supply control.

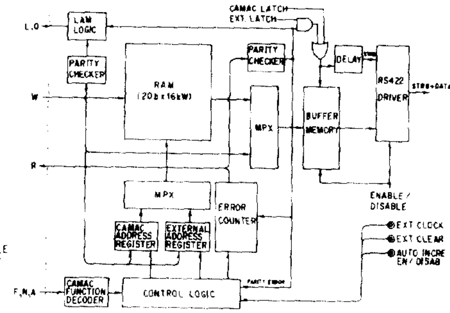

Fig. 2 Block diagram of the dual-port memory module.

the CAMAC crates in the local control rooms near the power supplies. During acceleration and deceleration, the reference current data are supplied to the power supplies from the memory modules at the timing intervals which are determined by the global accelerator timing system for AR and by the clock generator for MR and the selection of the skipping modes of the timing clock pulses. The mode selection is made in the timing module by chosing the rate multiplier of the clock pulses.

The 100 Hz clock signals of the global timing signal are extracted with a timing repeater and sent to the memory modules to transmit the reference current data to the power supplies during acceleration and deceleration (Fig. 1).

Memory module

The reference current data from the minicomputer are stored in the RAM (random access memory, 20 bits × 16 kW) of the memory module. The partition of 20 bits is 16 for the current data, 3 for the status and 1 for the parity. The parities attached to the reference data are checked when writing to and reading out from the RAM. If the parity checker finds a parity error, the LAM (look at me) signal requires the re-transfer of data when writing, while in reading the data with errors are neglected holding the last correct data in the output buffer and the error is counted with the error counter whenever the parity error is found. The block diagram of the memory module is shown in Fig. 2.

The memory module also allows the direct data transfer skipping the RAM data storage by writing the data on the output buffer from the computer terminal. This operation is useful when the fine adjustment of the current is required. It is possible to write a part of the sequential current pattern data in a vacant area of the RAM and to replace the normal pattern data with them in the midst of the operation by specifying the leading address of the sequential data in the RAM to an address counter.

The memory module has two I/O ports. One of them is used for the data I/O of the minicomputer and the other is used to send the digital data to the DAC of the power supply. In the latter case a datum is synchronously sent by the input of the external timing clock.

Timing module and clock generator

The status of the storage ring is distinguished by the 3-bit data attached to one of the current pattern data which are decoded with the timing module (Fig. 3). This module makes three event pulses giving the timing of the beginnings of injection (P1) and flattop (P3) and the end of deceleration (P5). These pulses are combined with another event pulses giving such as the initial timing for the start of an operation cycle (P0) and the beginnings of acceleration (P2) and deceleration (P4). The event pulses P0-5 form a complete cycle and some of them may appear many times in a cycle for the multi-flat-porch operation. Receiving the event pulses (P0, P2 and P4) the timing module sends out the 100 Hz timing pulses to the memory module.

The supplemental timing module of Fig. 4 is also prepared for MR to generate the clock pulses with variable frequency which enables the easy smoothing of the current at both ends of acceleration or deceleration. One clock mode of the frequency modulation can be selected from 16 modes in the read-only-memory (ROM) by executing the CAMAC function. It is operated and stopped by the execution of the CAMAC function or by the input of the external pulse. With this module it is possible to retain an arbitrary beam energy during ac-

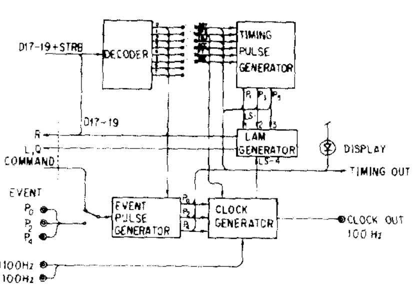

Fig. 3 Block diagram of the timing module.

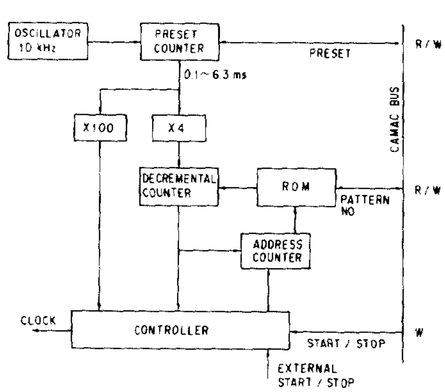

Fig. 4 Block diagram of the clock generator.

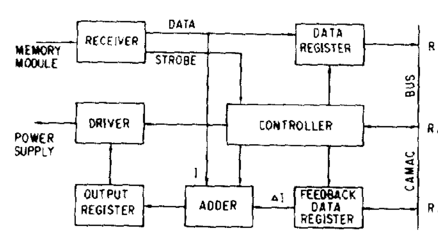

Fig. 5 Tune feedback control.

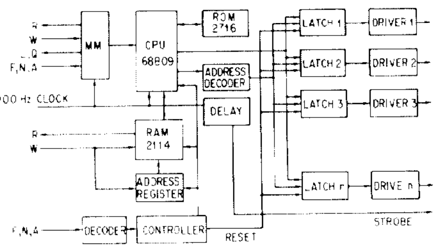

Fig. 6 Power supply control module for the steering magnets and backleg windings.

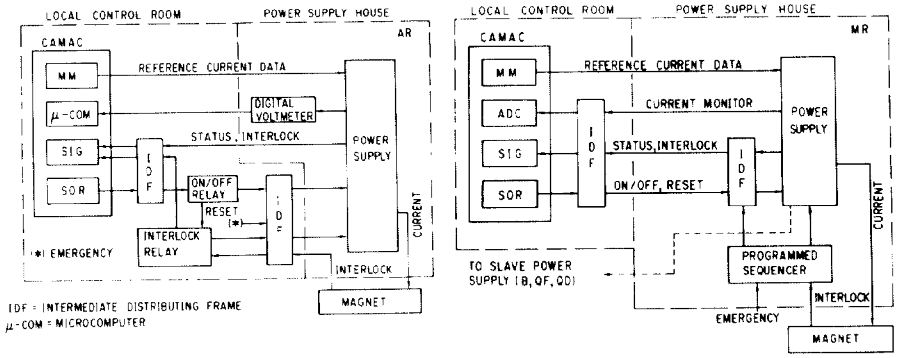

Fig. 7 Signal flows in the AR and MR power supply systems.

celeration. In the former timing module, the smoothing is given by the parabolic increase or decrease of the reference data.

The clock pulses thus extracted or generated at two places (one for AR and the other for MR) are distributed to all power supply houses with the timing pulse receiver & transmitter.

Tune feedback control module

In acceleration the electron and/or positron beams suffer the tune variation due to the tracking error of the magnet currents. The deviations of vertical and horizontal tunes can be fed back to the main quadrupole power supplies (QF, QD) through the tune feedback control modules [2]. Both the feedback data from the CAMAC bus and the reference data from the memory module are given and added in this module to generate the 16 bit digital data for the power supply (Fig. 5). The tune feedback control module is installed in the CAMAC crate and has a role of the interface between the memory module and the power supply. Its operation can be done remotely by the CAMAC command.

Power supply control module for the steering magnets and the backleg windings

By the requirement of the closed orbit control, many steering magnets and backleg windings are prepared and each has an individual small power supply. To operate them with different currents remotely, a simplified control method is developed to save the cost. A fundamental current pattern data are obtained from the memory module and a large number of reference data are calculated from it with an aid of a microprocessor. The microprocessor modifies the initial pattern multiplying coefficients and adding offsets which are gained from the measurement of the closed orbit deviation [3]. As an interval of the clock pulses is 10 msec for AR and 20 msec for MR which are long compared with the processing time, it is possible to treat many reference data with a commercially available 8-bit microprocessor. The number of current data processed with a unit is 10 for AR and 72 for MR and the total number of the control units is given in Table 3. All modified 12-bit data are latched and transferred at a time to the respective power supplies in synchronization with the clock pulse described above. The block diagram of the control module is given in Fig. 6.

Signal flow in the power supply system

Signals such as the current pattern data, interlocking signal, status signal, remote on/off and reset signals and emergency signal flow all over the accelerator area. The power supply is protected from the own failure such as the over-voltage, over-current, ground-fault, water-loss, etc., and the external interlocking signal arose from the magnet failure trips the corresponding power supply. All informations concerning to the interlock and status of the power supplies are gathered at the central control room via the signal input gates (SIG) in the CAMAC crates.

The remote on, off and reset signals are sent out from the control room via the status output registers (SOR) in the CAMAC crates as the momentary contact signals. These signals and the reference current data allow the remote operation with ease. In an emergency most power supplies are tripped with a stroke of the emergency button.

The current references are transferred from the output buffer of the memory module and latched in the input register of the power supply with the strobe signal which is supplied by each memory module with a delay of 10 μs behind the reference current data.

The output current of each power supply can be measured and gathered via the CAMAC interface to display on the screen at the control room. At AR the output currents are measured with the external multichannel digital voltmeters with the help of the intelligent CAMAC modules[4], whereas at MR the currents are measured in the CAMAC crates with the analogue-to-digital converter (ADC).

The schematic flows of the data and signals are shown in Fig. 7 for both AR and MR. These flows are controlled and surveyed under the execution of the power supply programs [5].

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