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SYNCHRONOUS TIMING OF MULTI-ENERGY FAST BEAM EXTRACTION DURING A SINGLE AGS CYCLE*

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Introduction

Synchronous triggering of fast beams is required because the field of Kicker Magnets must rise within the open space between one beam bunch and the next.

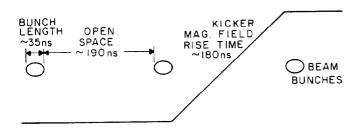


Fig. 1 - Kicker field rise time vs AGS beam bunch spacing.

Within the Brookhaven ACS, Fast Extracted Beam (FEB) triggering 2 combines nominal timing, based on beam energy with bunch-to-bunch synchronization, based on the accelerating rf waveform. During beam acceleration, a single bunch is extracted at 22 GeV/c and within the same AGS cycle, the remaining eleven bunches are extracted at 28.4 GeV/c.

When the single bunch is extracted, a "hole", which is left in the remaining circulating beam, can

appear in random locations within the second extraction during successive AGS cycles. To overcome this problem, a synchronous rf/12 counting scheme and logic circuitry are used to keep track of the bunch positions relative to each other, and to place the "hole" in any desired location within the second extraction. The rf/12 signal is used also to synchronize experimenters triggers.

System Equipment

Equipment of the Fast Extracted Beam timing system (Fig. 2) include:

- A. Computer controlled datacon autodet ³ "delays", which generate nominal timing pulses and equipment triggers;
- B. "Trigger synch" modules, which synchronize the nominal timing pulses to the beam bunch related signal;
- C. The "rf divider" module, which develop the rf/12 signals used for synchronization;
- D. "Pulse amplifier" modules, which interface the "Schottky" TTL level electronics of the previous two modules to the kickers and other equipment requiring higher level triggers.

The trigger synch, rf divider and pulse amplifier are implemented through standard "NIM" modules.

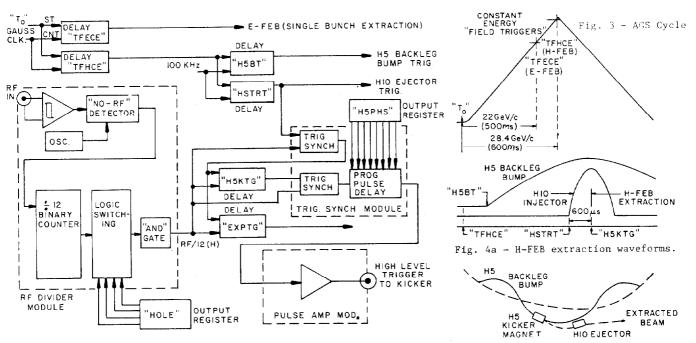


Fig. 2 - FEB timing and trigger synch. equipment.

Fig. 4b - H-FEB extraction orbit.

^{*}Work performed under the auspices of the U.S. Department of Energy.

Nominal Timing

As shown in Fig. 3, within the AGS cycle, fast extracted beam timing starts with field related constant energy triggers: "TFECE", the nominal start trigger for the E-FEB (single bunch extraction); "TFHCE", the nominal start trigger for the H-FEB (remaining beam extracted).

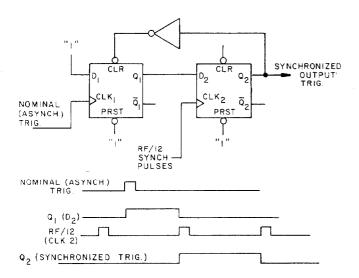


Fig. 5 - Pulse catcher synchronization.

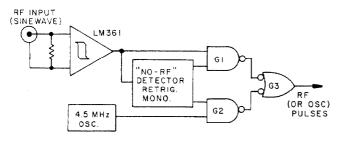


Fig. 6 - Rf input and "no-rf" detector.

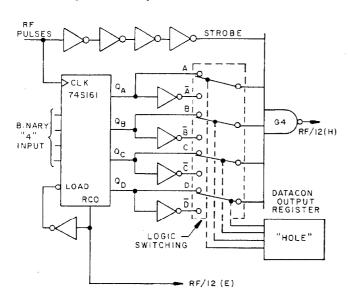


Fig. 7 - Rf/12 binary counter.

H-FEB is presented here as an example in the synchronization of kicker and other FEB related triggers.

TFHCE starts datacon autodet delays, which generate triggers for the H5 Backleg Bump, ("H5BT"), and the H10 Ejector, ("H5TRT"). (Backleg Bump and Ejector waveforms are shown in Fig. 4a; H-FEB operation on Fig. 4b.)

Trigger Synchronization

The H-10 ejector trigger, HSTRT is synchronized with an $\rm rf/12(H)$ pulse, and the synchronized output then used to start delays for experimenters in the fast beam line, as well as for the H5 kicker trigger, ("H5KTG").

During the relatively long period (~600 µsec) between HSTRT and beam extraction, the beam makes over 250 revolutions within the AGS ring, where small changes in rf phase with respect to the beam bunches may occur. To offset any problem this may cause, H5KTG is put through re-synchronization before triggering a programmable pulse delay (see Fig. 2). The pulse delay is used to align the rise in the kicker field, with the open space between bunches. Delay is controlled through an 8 bit "binary" word, adjustable in steps of I nanosecond. Computer control is through a datacon "Output Register", for H-FEB, named "H5PHS" within the Computer.

For trigger synchronization, a "pulse catcher" circuit is employed using a dual "D" (74874) flip/flop, and is shown in Fig. 5.

RF Divider

The signals used for trigger synchronization are derived within the rf divider module, where the process starts with the rf signal itself. The sinusoidal AGS low level rf drive signal was used since it was the cleanest, and most distortion-free signal available. The rf signal is sent to an LM361 wide band comparator, which converts the sinewave into TTL

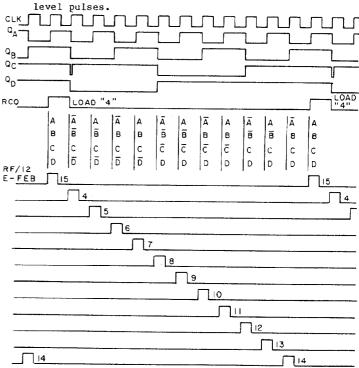


Fig. 8 - Counter operation and rf/12 outputs.

The output from the 361 comparator is sent to a gate G1, and to a retriggerable monostable multivibrator (74123) (as shown in Fig. 6). The multivibrator has a delay time of $1/2~\mu sec$, so as long as it sees rf pulses from the comparator, the "mono" will enable "GI", allowing rf pulses to pass. If the rf pulses disappear, the "mono" will change to enabling "G2", allowing pulses from the fixed oscillator to be used.

This "NO-RF" detector and oscillator scheme was necessary in order for the system to generate triggers in the absence of beam. Gate "G3" is used as an "OR", allowing either rf, or oscillator pulses through. From G3, the rf (or oscillator) pulses are sent to a binary counter (74S161) for division.

The 161 binary counter is implemented to divide the rf pulses by 12 (see Fig. 7). To do this, the "Ripple Carry Output" (RCO) is used in a synchronous mode to "load" a binary "4" from the counter's inputs, to its outputs. The 74S161 then counts from 4 to 15, where the RCO reloads the binary "4" again, and rf/12 count process continually repeats.

Figure 8 shows the logic outputs (Q_A-Q_D) of the binary counter. Through logic controlled switching (Fig. 6), the 12 allowable combinations of the "true" and "not true" outputs of the counter will yield the rf/12 signals which are used for synchronization (also on Fig. 8). Gate "G4" "ANDS" together the combinations dictated by the logic switch "positions", with a strobe derived from the rf pulses directly.

The rf/12 signal used for synchronizing E-FEB (single bunch extraction), taken from the binary counter's ripple carry output is also strobed.

For the H-FEB, a particular rf/12 signal is chosen by a 4 bit "binary" word, generated within a Datacon "Output Register". Allowable magnitudes are from binary "4" to binary "15". This device is aptly named "HOLE" within the computer, since changing its value will change the position of the missing bunch within the second extraction.

Pulse Amp

Once the trigger pulse has been developed within the trigger synch module, the TTL level pulse must be transformed into a reliable pulse for triggering the fast kicker.

Having low jitter (with respect to the synchronizing waveform) required that the trigger have fast rise time, and a long distance between the triggering equipment and one of the kickers required that be capable of maintaining fast rise time through long (~1,000 ft) coaxial cable.

As shown in Fig. 9, for the system described, an amplifier employing an MOS power FET, (VN98AK), and pulse transformer output was used. National "Clock Drivers" (0056CN) interface the TTL signal to the power FET.

Stability (Jitter)

The oscilloscope waveform shown in Fig. 10 is part of a test sinusoidal rf signal used for synchronization. External triggering used for the horizontal sweep is the H5 kicker trigger output from the trigger amplifier module. The picture shows approximately 400 traces of the "zero crossover" of the waveform, with total jitter less than 3 nanoseconds.

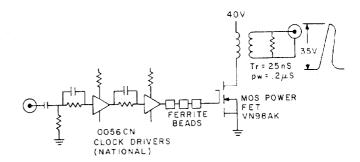


Fig. 9 - Kicker trigger pulse amplifier.

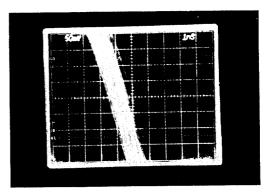


Fig. 10 - Rf (synchronizing) signal zero crossing.

Figure 11 shows the H-FEB extraction, with the single bunch of the E-FEB missing.

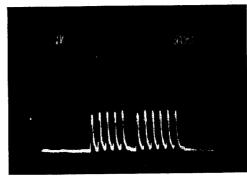


Fig. 11 - H-FEB extracted beam.

The timing system has been in use, since its design, for the past two fast beam running periods, efficiently providing timing and trigger synchronization for both single bunch and fast beam extraction.

Acknowledgment

The authors would like to thank Dr. R. Witkover for his editing expertise.

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