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PADAC MULTI-MICROCOMPUTERS
BASIC BUILDING BLOCKS FOR FUTURE CONTROL SYSTEMS

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Summary

Based on experience with the PETRA control system a concept for multi-microcomputer arrangements within the PADAC[1] standard has been developed. This setup allows the use of independent microcomputers (based on the TMS 9900) within a group of PADAC crates. Each individual microcomputer executes code from its local memory and has access to all PADAC I/O modules and a common database (256 kbytes of memory) via the shared PADAC bus. The database is assumed to contain at any time the current status of a certain control sub process. A modified version of the SEDAC[2] data acquisition hardware is be used to collect the process status at the necessary refresh rate. The communication with the outside world (operator console, etc.) is accomplished by a fast packet switching network (FPSS[3]).

Design Objectives

The PETRA control system divides accelerator control into a number of tasks: vaccum, rf, magnets and monitors, etc. Each task is handled by a dedicated minicomputer with multi-user and multi-tasking capabilities. Operational experience has shown that this setup provides sufficient sub task independence, especially during setup and maintenance periods. User demands have grown in two areas: more 'watchdog programs' for permanent equipment checks and larger numbers of constantly updated TV displays. For swift operational overviews it is desirable to have pictures in a ready-to-display form. These two demands require a vastly increased CPU bandwidth. While a multi-tasking operating system in principle allows the sharing of one CPU by a number of these programs, the updating of a small number of TV displays at desirable rates exceeds the CPU power of any mini.

To overcome this bottleneck, repetitive tasks of this nature can be off-loaded into a number of front-end microcomputers, each executing one task. To fit into the framework of the existing control system standards at DESY, the following design objectives have to be met:

- incorporation into the PADAC standard
- use of the standard PADAC microcomputer (MICRO/A) for bus arbitration, system management, host communication, and computer network (FPSS) services.
- program execution on an 'unlimited' number of sub-micro-computers (MICRO/B), which can be plugged into the system like standard PADAC modules.

Micro/B design objectives include:

- cpu chip identical to micro/A cpu chip for ease of program development
- private program memory for each micro/B
- access to all PADAC I/O modules
- access to common memory within micro/A
- indivisible multi-word transfers between common memory and private memory

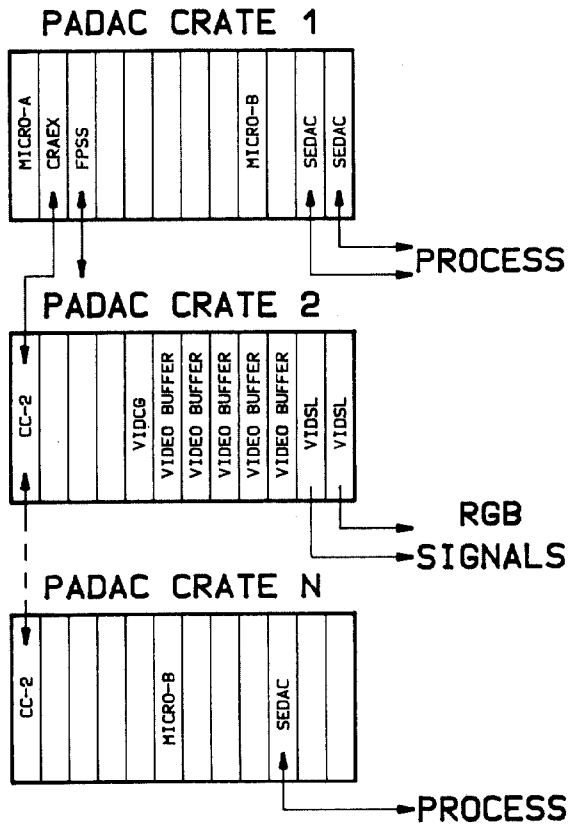

Fig. 1: Multi-Microcomputer Setup

Realization

Hardware

The crate width limitation of PADAC (12 modules per crate) has been overcome by a crate extension module which extends module addressibility to a sufficient number of crates (limited by RS-422 standards and the 11-bit module address).
Micro/B virtual memory space is divided threefold:
- local memory
- PADAC I/O addresses
- common memory mapped into micro/A memory space through a page table mechanism

Programmed access to non-local memory is executed as a PADAC DMA cycle, whose timing is controlled by the micro/A bus arbitrator. Since this is asynchronous to micro/B timing, wait cycles are introduced into micro/B memory timing.

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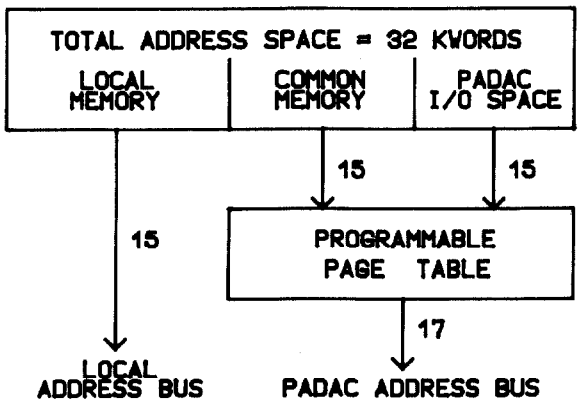

Fig. 2: Micro/B Address Space Layout

Non-divisible multi-word data transfers between common and local memory are handled by a channel-to-channel interface on micro/B. In the burst mode used, PADAC protocol permits consecutive DMA transfers without new bus arbitration.

Although all micros/B compete for PADAC bus cycles to execute their non-local memory references, bus contention is not expected unless the number of micros/B exceeds ~30, since it is virtually impossible to write a program with more than a few percent of non-local memory accesses.

Micro/A and any micro/B communicate by interrupting each other. Qualifiying information about the nature of the interrupts is exchanged via dedicated areas of common memory.

Local memory is laid out for static RAM / EPROM compatibility, which permits both PROM-resident programs and programs down-loaded from a host computer via the FPSS-network under micro/A supervision.

By use of its I/O connector micro/B can be configured as an intelligent I/O device, such as a SEDAC line controller. Extra board space for specific applications will be provided by a daughter board on micro/B.

Current PADAC micro implementation is built around the TMS-9900 CPU chip.

Software

Micro/A installations at DESY use a multi-tasking system developed in house. It provides resource allocation, interrupt handling, and process scheduling. Typical task switching time is 250 usec.

The system has been designed to permit adaption of multi-tasking to a multi-processor environment. Micro/A retains supervisor functions and global control blocks, while actual program execution can be deferred to a micro/B.

References

1) G. Hochweller, H. Frese; Tools for Man Machine Communication in the PETRA Control System, IEEE Nucl. Sci. 26 (1979), p. 3382
2) H. Frese, G. Hochweller; The Serial Data Acquisition System at PETRA, IEEE Nucl. Sci. 26 (1979), p. 3384
3) H. Frese et al., FPSS - A Fast Packet Switching System, these proceedings