

DESIGN STUDY OF LOW-LEVEL RF CONTROL SYSTEM FOR CW SUPERCONDUCTING ELECTRON LINEAR ACCELERATOR IN KAERI

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Abstract

Korea Atomic Energy Research Institute (KAERI) has been operating a 20 MeV superconducting RF linear accelerator (SRF LINAC) to conduct research on atom/nuclear reaction using neutron Time-of-Flight (nTOF). It can accelerate electron beams up to 20 MeV with 1 kW continuous wave (CW) operation mode. Unfortunately, this machine has been aged over 15 years that brings about considerably difficulty in normal operation due to the performance degradation of sub-systems. To normalize the operation condition of 20 MeV SRF LINAC, we have been carrying out an upgrade project with replacement and repair of old sub-systems from 2018. This paper describes a design study of Low-Level RF (LLRF) control system to improve the stability and acceleration efficiency of the electric field generated in the superconducting RF cavity structure of 20 MeV SRF LINAC.

INTRODUCTION

The nTOF method is generally used to measure and verify the neutron cross-section data of major actinides, minor actinides, and photo nuclear reaction library [1]. To produce neutron cross-section data from keV up to MeV range, construction of KAERI nTOF experimental building was started from early 2016. It will be mainly used to measure nuclear data [2].

To produce neutron beams in KAERI nTOF facility, we apply the photonuclear reactions in a target filled with liquid lead (Pb). An incident electron beam produces bremsstrahlung photons, and then bremsstrahlung photons bring about photonuclear chain reaction (γ, n) in the target. It can generate neutrons with a white spectrum [3]. Finally, neutrons go through nTOF experimental building with 10 m flight-path to analyze experiment results. Overview of KAERI nTOF facility is shown in Fig. 1.

To generate electron beam in the facility, SRF LINAC is used as an injector. It can accelerate electrons up to 20 MeV kinetic energy with 1 kW continuous operation mode. Two 352 MHz SRF cavities with a cryomodule were fabricated by CERN for the Large Electron-Positron Collider (LEP) facility [4]. To operate those SRF cavities, we installed a RF generator, a Helium refrigerator, a vacuum stage, a control system and a cooling system collaborating Budker Institute of Nuclear Physics (BINP), Russia in 1996.

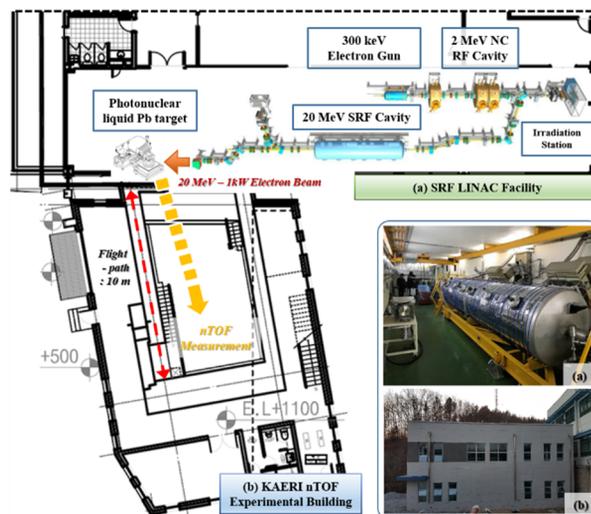


Figure 1: Overview of KAERI nTOF facility.

Unfortunately, a fire accident occurred at 2003, so sub-systems of RF generator and Helium refrigerator were broken or malfunctioned. In addition, many components of SRF LINAC outdated due to 15 years operating duration.

To solve those problems, we have been carrying out an upgrade project by replacing or repairing old RF sub-systems since 2018. In this paper, we review RF sub-systems of the SRF LINAC and design a new LLRF system based on digital signal processing to improve beam stability and accelerating efficiency.

SYSTEM OVERVIEW

The schematic of SRF LINAC for KAERI nTOF facility is shown in Fig. 2. At first, electron beams are generated from electron gun tank with 300 kV kinetic energy. They move to normal conducting (NC) RF cavities which accelerate electron beams up to 2 MeV. Continuously, SRF LINAC accelerates electron beams around 20 MeV.

SRF LINAC system is composed of two identically same RF stage. Each RF stage consists of SRF cavity, RF generator, and LLRF control system. SRF cavity has the amplitude of accelerating voltage around 9 MV per one stage with 352 MHz resonance frequency. To make high-intensity electric field (E-field) in SRF cavity, RF generator transmits 45 kW RF power signal to each stage. To raise the stability and acceleration efficiency of SRF LINAC, LLRF control system is essential. The operating parameters of SRF LINAC is summarized on Table 1.

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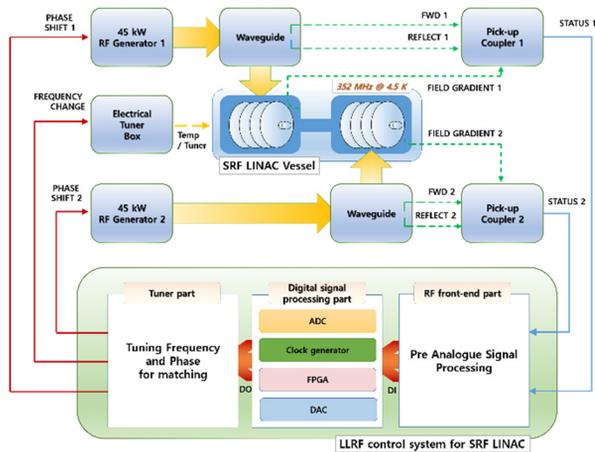


Figure 2: Schematic of SRF LINAC in KAERI nTOF.

Table 1: Operating Parameters of SRF LINAC

Parameter	Value
Resonating frequency	352 MHz
Power transmit (P_{RF})	45 kW
Maximum Accelerating Energy	20 MeV
Beam current (I_b) @ CW mode	1 mA
Operating temperature	4.5 K
Cavity type	Nb coated Cu
Number of cells	4-cell in 1 cavity
Q-factor (Q_0)	3.4×10^9 @ 6 MV/m
Characteristic Impedance (r/Q)	500Ω
Standing Wave Ratio (SWR)	< 1.1

LLRF control system has a role to prevent negative events such as beam current fluctuation, multipacting, field emission, excitation of high-order-modes (HOMs), thermal effect of frequency shifting, power distribution mismatch, microphonic, and so on [5]. If we neglect them without LLRF control system, it gives a bad influence of the beam acceleration and power generation.

Existing LLRF control system of SRF LINAC was developed by analogue system. It has advantages about intuitive implementation and low latency, but also has disadvantages about poor measurement resolution, scalability, and signal noise ratio (SNR). Moreover, existing LLRF control system consisted totally analogue components with long ages, so it was impossible to use fast data processing and big data logging. It makes worse in CW mode operation. If negative events occur simultaneously with no break time, it affects worse breakdown to RF hardware system directly than pulse mode operation. It causes problem of imprecise operation action and serious equipment damage. To overcome obstacles, we have decided to design the LLRF control system based on digital signal process.

DESIGN OF LLRF CONTROL SYSTEM

Proposed LLRF control system is classified into three parts: RF front-end part, digital signal processing part, and tuner part.

RF front-end part work for not only receiving, but also reprocessing transmit signals from RF generator to RF cavity. Input signals of RF front-end are forward power, reflect power and accelerating electric field in general. In the RF front-end part, many analogue components such as a filter, an attenuator, an amplifier, a mixer, and a combiner are necessarily used. They are applied to eliminate perturbation noise and convert RF frequency for defining output signals which flows to digital process part's input signals.

Digital signal processing part generally consists of an Analogue-Digital Converter (ADC), a clock-generation module, a Field Programmable Gate Array (FPGA) as logic board, and a Digital-Analogue Converter (DAC). ADC converts analogue signals into digital signals for implementing the sampling, and DAC works reverse versa. Clock generation module is used to implement digital sampling and synchronize timing of digital processing. Digitized sampling data go into FPGA board to compute operation frequency and power transmit level. To compare transmit signal and detecting signal, FPGA board derives output command to change operating parameters of RF system.

Finally, tuner part adjusts tuning rods to change operating frequency, or shifts phase value to match reference power level. Requirement of LLRF control system parameters is summarized in Table 2.

Table 2: Requirement Parameters

Parameter	Value	Note
Center Frequency	352 MHz	f_0
Bandwidth	~ 100 kHz	Δf_{3dB}
Phase Control Stability	≤ 0.1 deg	rms
Amplitude Control Stability	< 0.1%	rms
Phase Acceptance	$\pm 50 \sim 80^\circ$	
Dynamic range	> 20 dB	Nominal Gradient Range
Set Point Resolution	$\leq 0.1\%$, 0.1 deg	SNR Digital Resolution
Thermal Stability	± 0.05 dB	$10^\circ\text{C} < T < 40^\circ\text{C}$

METHODS AND MATERIALS

To analyze RF transmit signal in LLRF system, IQ sampling method is widely used [6]. When precise control is required, the amplitude and phase of a signal are usually detected using the IQ sampling with is written as Eq. (1).

$$\begin{aligned}
 y(t) &= A \sin(\omega t + \theta_0) \\
 &= A \cos \theta_0 \sin \omega t + A \sin \theta_0 \cos \omega t \quad (1) \\
 &= I \sin \omega t + Q \cos \omega t
 \end{aligned}$$

It is possible to calculate the amplitude and phase of the RF signal from measured IQ signal by employing a simple calculation as in the Eq. (2).

$$A = \sqrt{I^2 + Q^2}, \quad \theta_0 = \tan^{-1}\left(\frac{Q}{I}\right) \quad (2)$$

Detection signals from SRF LINAC is processed in RF front-end and ADC module by IQ sampling method. After measurement of sampling data, each terms of IQ sampling value are extracted by IQ modulation. To convert frequency to handle in FPGA, we use digital down conversion at an intermediate frequency in a traditional heterodyne scheme. Pick up signals from direction coupler or RF cavity are processed in FPGA with proportional plus integral (PI) algorithm. The PI controller consists of a proportional (P) control process, and an integral (I) process to find solutions [7]. All RF signals, once down converted and digitized, are processed in an FPGA. To generate output signal, IQ demodulation process will be run to convert analogue operation command. Flow chart of digital signal process is shown in Fig. 3.

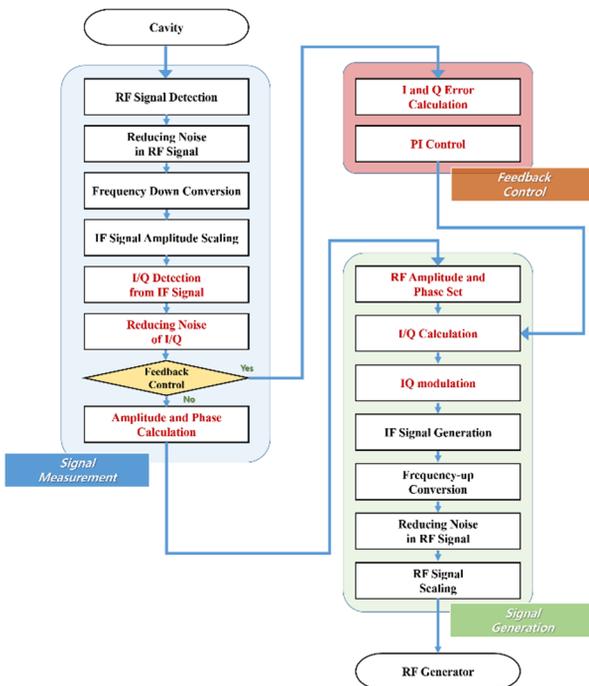


Figure 3: Flow chart of digital signal process [8].

To develop LLRF control system, we design architecture of digital LLRF board as shown in Fig. 4. It consists of two ADC modules, one FPGA module, one clock generator, one Digital Input (DI)-Digital Output (DO) module, and one DAC module with Experimental Physics and Industrial Control System (EPICS) Input/Output Controller (IOC) [9]. EPICS IOC will communicate with main server computer or embedded processor by gigabit Ethernet to satisfy low latency and fast response time.

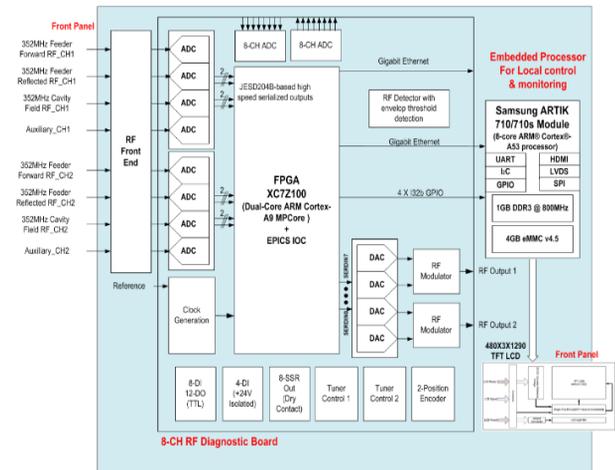


Figure 4: Design Architecture of digital LLRF board.

RESULTS AND DISCUSSION

We introduced KAERI nTOF facility and SRF LINAC system. To evaluate performance, we proposed conceptual design of LLRF control system based on digital signal processing. It has advantages to increase beam stability and acceleration efficiency for CW mode in superconducting accelerator. In the future, we will accomplish design optimization to improve performance. Finally, we will fabricate whole system and conduct performance evaluation to verify operating result data and compare to the design characteristics.

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