# TIMING SYNCHRONIZATION SYSTEM FOR BEAM INJECTION FROM THE SACLA LINAC TO THE SPring-8 STORAGE RING

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# Abstract

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title of the work, publisher, and We developed a timing synchronization system for injection from the linac of the XFEL machine, SACLA, to the lor( storage ring (SR) of SPring-8. This injection scheme is demanded by the low-emittance upgraded ring in the future. Since the RF frequencies of the linac and the SR do not have  $\overline{2}$  an integer multiples relation, we have to introduce a new on scheme to synchronize the beam ejection timing of the linac to the desired RF bucket timing of the SR. The timing is roughly adjusted by re-clocking the master trigger signal of the linac with the SR bucket timing. The residual timing difference is compensated by applying frequency modula-tion to the linac master oscillator. The amount of the timing z difference is obtained by sampling the linac reference signal  $\overline{\Xi}$  with an ADC where the SR reference signal is used as a sampling clock. We built this synchronizing system with MTCA.4 modules. The system was installed to the linac and the measured timing jitter was better than 4 ps in rms, which was enough to obtain high injection efficiency.

## **INTRODUCTION**

distribution An upgraded synchrotron radiation ring SPring-8-II [1] Frequires a low emittance beam for the injection because of its small dynamic aperture. The current injector of SPring-8 6 does not satisfy this requirement. One solution is to utilize 20 the linac of the Xray Free Electron Laser (XFEL) facility, SACLA [2], which has very low emittance electron beam. licence The new ring has a short bunch length of 6 ps in rms. which also requires a precise timing synchronization is required at 3.0 the injection.

There are several methods to synchronize the beam ejec-M tion timing of the linac with the bucket timing of the storage ring (SR). The first method is waiting for an accidental coincidence between the two timing signals. The second method is to use an arbitrary waveform generator (AWG) synchroterms ( nized to the SR, and to make the AWG output a pulsed rf  $\underline{\underline{g}}$  reference signal for the linac [3]. The third method is to use a common divisor frequency to generate the rf reference ы pui frequencies of the linac and the ring [4]. The first method is not applicable because the timing acceptance of the ring is too small to wait in actual operation. The second method has  $\frac{2}{2}$  difficulty in reducing the phase noise of the linac reference  $\hat{\Xi}$  signal. As for the third method, the linac frequency is affected by the SR frequency change. The circumference of the ring changes of the order of  $10^{-6}$  due to tidal effect and so on, and the reference frequency of the SR also changes the same from amount to keep the beam energy of the ring constant. This situation is not preferable for the high-power ultrashort-pulse

lasers used at the XFEL experiment, where stable reference is required for precise timing synchronization between the XFEL pulse and the laser pulse.

We adopt a new scheme to synchronize the linac ejection timing with the SR bucket timing. We apply two steps for synchronization. The first step is adjusting the master trigger timing of the linac to the SR bucket timing. The second is applying Frequency Modulation (FM) to the master oscillator of the linac. These timing modifications are applied only at the SR beam injection shot to minimize the perturbation to the XFEL shots. The detail of the synchronization method, implementation of the system to MTCA.4 standard modules and achieved performance are described in this paper.

# SYNCHRONIZATION BETWEEN LINAC AND STORAGE RING

## Master Trigger Timing

At the linac of SACLA, the frequency of the timing clock is 238 MHz, which is the frequency of the sub-harmonic cavity,  $f_{Li}$ , and its interval is 4.2 ns. The master trigger is synchronized to the 238 MHz clock and the AC power line signal (60 Hz). The time interval between this master trigger timing and the beam ejection timing is 15.5 ms, which corresponds to a fixed delay count of the linac clock. This clock and the master trigger are delivered to the subunits through the optical links. The reference frequency of the storage ring,  $f_{SR}$ , is 508.58 MHz, and a bucket interval is 2.0 ns. The number of the stored buckets in the storage ring (the harmonic number, h) is 2436 and the revolution interval is 4.8 µs.

If a logical AND of the AC 60 Hz and the SR revolution signal is used as the input data to the D-F/F whose clock is  $f_{Li}$ , the maximum timing difference between the master trigger and the revolution signal is 4.2 ns.

#### with Measurement and Adjustment of the Timing Difference

published The next task is to measure the residual timing difference between the master trigger and the revolution signals. We usually use an oscilloscope or a time interval counter for timing measurement. These devices need averaging to obtain high resolution and are not suitable for the single shot measurement with high precision. We measure the phase final of the clock signals which the timing signals are based on. In our case, the master trigger timing is based on the linac reference and the revolution timing is based on the SR reference. Those reference clocks have different frequencies preprint and treating the phase is a complex thing. Therefore, we prepare a Numerically Controlled Oscillator (NCO) whose

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Precise Adjustment of Ejection Trigger Timing

For stable XFEL operation, the FM amplitude should be

reduced as small as possible. It is required not only from

the amplitude and phase stabilities of the rf accelerating

structures of the linac, but also from the ultrashort-pulse

lasers used at the pump and probe experiments. The lasers

have the resonators with about 3 m path length and the piezo

path length compensators are used to lock the laser timing

to the linac timing. The timing change of 4.2 ns within 15.5 ms during the SR injection corresponds to the frequency

deviation of  $2.7 \times 10^{-7}$ . The path length change of the laser becomes about 1 µm, which is over the stroke of the

piezo compensator. From the point of view of the SR, the ejection timing can be delayed by the integer multiple of the revolution time. The change of the timing difference after

 $dt_0 = \frac{h}{f_{SR}} - \frac{\operatorname{int}\left(\frac{f_{Li} \cdot h}{f_{SR}}\right)}{f_{Li}}$ 

Utilizing this relation and the phase  $\phi_0$  measured at the pretrigger (which is synchronized to the AC 60 Hz and the

bucket timing), the wait revolution number *n* is calculated

to be  $n = \phi_0 / \Delta \phi$ , where  $\Delta \phi = dt_0 \cdot 2\pi f_{Li}$ . Then the actual

master trigger is delivered to the linac subunits after the n revolution time from the pre-trigger. The maximum time

difference is reduced from 4.2 ns to 0.1 ns, and the range of FM is reduced to 1/42. This value is small enough compared

to the full stroke of the piezo compensator. Maximum delay time from the pre-trigger is  $42 \cdot 4.8 \,\mu\text{s} = 197 \,\mu\text{s}$ , which is

one SR revolution time  $dt_0$  is as follows,

frequency corresponds to the difference between the two clocks,  $\Delta f = f_{Li} - f_{SR}$ . The phase of the NCO signal is set to zero at the master trigger timing. The linac reference clock signal is input to an ADC with a sampling clock of the SR reference signal. The obtained data from the ADC have the same frequency to that of the NCO, and here we can define the phase, i.e. the timing difference. The *k*-th data sampled by the ADC, a(k), at the time  $t(k) = k/f_{SR}$  is expressed as follows,

$$\begin{aligned} u(k) &= \cos[2\pi f_{Li} \cdot t(k) + \phi] \\ &= \cos\left[2\pi k \frac{f_{Li}}{f_{SR}} + \phi\right] \\ &= \cos\left[2\pi k \frac{f_{Li} - f_{SR}}{f_{SR}} + 2\pi k + \phi\right] \\ &= \cos[2\pi\Delta f \cdot t(k) + \phi], \end{aligned}$$

where  $\phi$  is a phase offset at time zero, i.e. k = 0. We prepare two NCOs which correspond to the cosine component,  $a_{N \cos}(k)$ , and sine component,  $a_{N \sin}(k)$ ,

$$a_{N\cos}(k) = \cos[2\pi\Delta f \cdot t(k)]$$
  
$$a_{N\sin}(k) = \sin[2\pi\Delta f \cdot t(k)].$$

By multiplying the sampled data with NCO signals, we obtain two values, I(k) and Q(k), which have information on  $\phi$  and a fast oscillating term,

$$I(k) = a(k) \cdot a_{N\cos}(k)$$
  
=  $\cos[2\pi\Delta f \cdot t(k) + \phi] \cos[2\pi\Delta f \cdot t(k)]$   
=  $\frac{1}{2} \{\cos[4\pi\Delta f \cdot t(k) + \phi] + \cos\phi\}$   
 $Q(k) = a(k) \cdot a_{N\sin}(k)$   
=  $\frac{1}{2} \{\sin[4\pi\Delta f \cdot t(k) + \phi] - \sin\phi\}.$ 

The initial phase  $\phi$  can be extracted by applying a low pass filter (LPF) to the values I(k) and Q(k),

$$\phi = -\arctan\left\{\frac{\text{LPF}[Q(k)]}{\text{LPF}[I(k)]}\right\}.$$
(1)

For a high-resolution phase measurement, the frequency  $\Delta f$  should be carefully selected because of the limitation of the ADC's sampling speed and its resolution. We use frequency dividers of 1/3 and 1/6 for the linac clock and the SR clock, respectively. The 1/3 divider is reset by the master trigger of the linac. The 1/6 divider is also reset for synchronizing to the aimed bucket timing. The value of  $\Delta f$  is as follows,

$$\Delta f = 238 \text{MHz}/3 - 508.58 \text{MHz}/6 = 5.43 \text{MHz}.$$
 (2)

The residual timing difference within 4.2 ns can be corrected by applying an FM control to the Master Oscillator (M.O.) of the linac. A Proportional and Integral (PI) feedback control is implemented to stabilize the phase to the set value.

small compared to the AC line interval of 16.6 ms.

# IMPLEMENTATION OF THE SYSTEM TO MTCA.4 STANDARD MODULES

This synchronization logic was implemented in MTCA.4 modules [5]. We used a commercially available digitizer Advanced Mezzanine Card (AMC) made by Struck Innovative System GmbH, SIS8300L2 [6], and a custom made Rear Transition Module (RTM) made by Candox system Inc. [7]. The AMC has a maximum sampling rate of 125 MHz and 16 bits resolution. A firmware running on the Field Programmable Gate Array (FPGA) of the AMC was coded by Mitsubishi Electric TOKKI Co. [8]. A block diagram of the system is shown in Fig. 1. The  $f_{SR}/6$  signal is used for the clock of the FPGA and the ADC. The AC 60 Hz signal is input to the AMC, and the pre-trigger is generated inside the FPGA. The wait turn number *n* is calculated using the measured phase at the pre-trigger timing. Then, the actual master trigger is generated after the *n* revolution time and is delivered to the linac subunits. The residual phase difference is compensated by feeding a FM control signal to the M.O. of the linac.

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maintain attribution to the author(s), title of the work, publisher, and DOI Figure 1: Block diagram of the system. The timing difference is measured at the phase detection section. The precise adjustment of the master trigger is made and the residual difference is compensated at the FM feedback section.

#### RESULTS

The performance of the system was tested using actual ac-celerators. The SR reference signal was transferred through The performance of the system was tested using actual acan optical link. The master trigger signal was distributed to the linac subunits, the monitor modules and the pulse  $\stackrel{\text{g}}{=}$  magnets of the storage ring through the optical links. We of measured the time jitter between the SR reference signal and and the ejection trigger signal using an oscilloscope. Figure 2 shows waveforms triggered by the master trigger. A and and the ejection trigger signal using an oscilloscope. histogram of the 508.58 MHz signal projected to the timing axis is also shown in the figure. The peak-to-peak timing  $\overline{<}$  jitter of the 508.58 MHz clock signal was about 100 ps. This S value agrees to the expected one from the method described  $\Re$  in the previous section. Figure 3 shows waveforms triggered O by the ejection trigger signal. The timing jitter was 3.8 ps in <sup>2</sup>/<sub>2</sub> rms which showed successful suppression of timing differ-sence between the ejection timing and the bucket timing by  $\overline{\circ}$  the FM feedback. Using this system we successfully injected terms of the CC BY 3 a beam from the SACLA linac to the storage ring with an injection efficiency of better than 90 %.

### SUMMARY

We built a timing synchronizing system between the ejecthe 1 tion timing of the SACLA's linac and the SR's revolution timing. To build the system, we introduce two steps; the mas-ter trigger timing adjustment to a SR bucket timing within ter trigger timing adjustment to a SR bucket timing within 0.1 ns by waiting for up to 42 turns, and the FM feedback control to the master oscillator of the linac. The measured é atiming jitter was better than 4 ps in rms including the jit-Ξ ter of the oscilloscope. The beam injection test from the work linac to the storage ring was successfully carried out with an injection efficiency of better than 90 %. In addition to the synchronization system, we are developing a new control rom framework and a beam route control system for the beam injection from SACLA [9, 10]. User operation with this Content system is scheduled to start in 2020.



Figure 2: Measured timing jitter between the master trigger (green line) and the 508.58 MHz clock (red line). The horizontal axis shows the time with 500 ps per division. The vertical axis shows the voltage of the signal. The master trigger signal timing is 15.5 ms prior to the ejection timing. The jitter is about 100 ps peak to peak as expected.



Figure 3: Measured timing jitter between the ejection trigger (green line) and the 508.58 MHz clock (red line). The jitter is reduced to 3.8 ps in rms with the FM feedback.

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