ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-THPRB021

AUTOMATIC LOOP FOR CARRIER SUPPRESSION IN ATTOSECOND RF RECEIVERS

U. Mavric†, M. Hoffmann, F. Ludwig, H. Schlarb, L. Springer, Deutsches Elektronen-Synchrotron, DESY, Hamburg, Germany

Abstract

The carrier suppression interferometer method can be used as a radio receiver architecture which allows for detection of RF signals in the attosecond range. The carrier suppression scheme requires an automatic carrier suppression circuit which provides stable operation of the RF receiver in the best operating point. In the poster we investigate the requirements for such an algorithm, evaluate the achievable closed loop bandwidth and the side effects on the overall-performance. In addition we apply the carrier tracking to simplify and automate the characterization of various electronic phase shifters and attenuators in the as-range.

PROBLEM DEFINITION

The carrier suppression interferometer [1] used for attosecond receivers [2] requires a large suppression of the carrier before the residual of the carrier along with the signal is amplified by the high-gain, low-noise RF amplifier.

In this paper we investigate some of the limitations and requirements for an automatic procedure which will keep two RF vectors of a given frequency at the optimal amplitudes and phases relative to each other so that the combined result includes the lowest (in amplitude) possible vector of a given frequency. The automatic process should take into account influences coming from the environment (e.g. temperature, humidity, vibrations) and should consider that the phases and amplitudes of the two vectors can be in an unknown state at the process start-up.

Considering the block-diagram of the setup shown in Figure 1 the following system related questions are of concern:

1. The resolution of the DACs driving the phase shifters, variable attenuators or other microwave structures.
2. How fast can we follow the carrier changes and compensate for them?
3. Does the system need actuators of various sensitivities at given standard DACs?
4. What type of control algorithm to use?

SYSTEM OVERVIEW

Figure 1 represents the setup that was used to develop, test and study the automatic carrier suppression procedures. The main RF signal is generated by a common RF source operating at 1.3 GHz. The source is split and passed through various branches which are then recombined. The automatic procedure controls the variable phase shifter and variable attenuator which are located in one of the branches (see Figure 1). The same 1.3 GHz source is used to generate all the required signals to down-convert and sample the RF signal. The sampled signal is processed in an FPGA and transmitted over PCIe to a CPU. In parallel a second FPGA controls the DACs which drive the actuators (phase shifter and attenuator). The actuators are controlled by the same CPU over Ethernet.

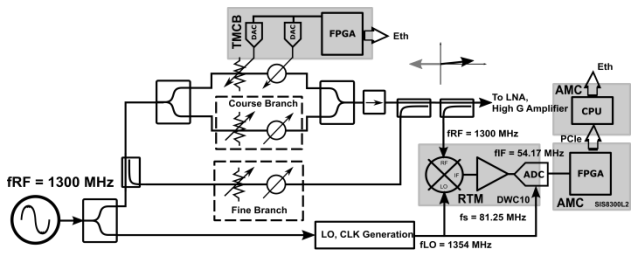

Figure 1: Block diagram of the measurements setup. The carrier suppression interferometer is implemented with connectorized components. The down-conversion, digitalization and CPU are centralized in a MicroTCA.4 crate. All the algorithms are running on the CPU.A one line figure caption is centred.

ALGORITHM IMPLEMENTATION

The proposed automatic process consists of two steps. The first step is slow and it addresses the problem of the unknown initial state. The second step is faster and it addresses the problem of a long-term tracking of the suppression, which is independent of the environmental changes. We have investigated two types of possibly faster algorithms. Feedback on the detected amplitude/phase and the method where we determine the correction based on 3 measured points of the suppression.

Slow Algorithm

In the first step both actuators are swept over their full range and the optimum control voltage is registered. The amplitude and phase control is done alternately. At each pass the range of voltage sweeps and the granularity of the driving voltages are decreased. The speed at which these two parameters fall with each pass defines the speed of convergence and quality of convergence (what suppression level are we able to achieve). The current settings use 2^{-n} for voltage step and 3^{-n} for sweep ranges and experiments show they are robust. The algorithm has always been able to find a suppression value in the range of -80dB within 20 iteration steps.

The algorithm can be implemented on a server level as the first step in the carrier suppression process. The slow

† uros.mavric@desy.de

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algorithm can be used in cases when the system has experienced a large change (phase or/and amplitude) in the loop (e.g. after power cycle, longer shutdown etc.) and we have no information where the optimal position is.

Fast Algorithm - Feedback on Amp/Pha

This algorithm uses the error values of the amplitude and phase of the suppressed carrier to calculate the correction voltage which is applied to the DACs. The main assumption is that at high suppression levels the amplitude and phase corrections can be decoupled and controlled separately. The positive feature of this method is that there is no perturbation of the system needed. The next calculated sample is already the correct one. The main disadvantages of this approach is that as the carrier gets smaller the phase and amplitude are less defined, thus the SNR is lower, resulting in a higher error of calculated correction sample. The next problem is the wrapping of the phase where at low carrier levels (<-75dB suppression) the signal experiences 180 deg phase jumps within the acquired buffer which makes the detection of the phase more complex. Furthermore, for this method the drifts of phase and amplitude in the receiver electronics cannot be distinguished from the drifts of the setup itself therefore this method requires additional drift compensation methods for the electronics. All the above mentioned problems lead to a more complex algorithm which finally results in a non-robust system. This is also what was observed during measurements. Therefore, it was decided that an alternative method will be investigated.

Fast Algorithm – 3 Point Method

The second approach uses the absolute value of the suppressed carrier as the input into the calculation of the next correction value. This makes the algorithm insensitive to detection electronics drifts (e.g. RMS detectors and amplitude transmission is less sensitive to drifts). The method uses 3 measured points of the suppression to predict the correction to be applied. The first measurement is non-perturbing, meaning that the control voltage equals to the currently set control voltage. The other two suppression values are obtained by slightly changing the control voltage in both directions from the current control voltage. The size of the delta voltage can be defined experimentally. For the measurements presented in this paper a delta voltage which causes a loss in suppression by 3dB was applied.

The algorithm relies on the fact that the suppression follows a typical "V" like shape shown in Figure 2. Based on this knowledge the algorithm expects some typical positions of the suppression values S_{-1}, S_0 and S_{+1}. For example, if the second suppression S_0 is lower than S_{-1} and S_{+1} it means the optimal suppression S_{opt} is located somewhere between S_{-1} and S_{+1}. Depending whether $S_{-1}>S_{+1}$ or $S_{-1}<S_{+1}$ the algorithm predicts whether the S_{opt} lays between S_{-1} and S_0 or S_0 and S_{+1}. The algorithm would under such conditions take the current delta voltage divided by 2 as the next delta voltage from the suppression voltage. Following this procedure the algorithm converges to lower suppression values. The main disadvantage of the algorithm is that it requires a constant perturbation of the loop in order to achieve a desirable suppression. If the required suppression is low the perturbations happen very often. The algorithm has proven to be robust over several hours (~ 24 h). The algorithm can be implemented on an FPGA.

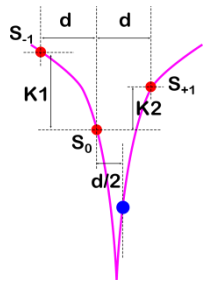

Figure 2: The geometrical representation of the fast algorithm (3 points). The suppression values follow a "V"-like shape around the optimal suppression value.

RESULTS

We have investigated how the suppression value affects the detected amplitude and phase noise of the suppressed carrier before the amplifier. Furthermore, we measured how much one has to change the phase and the amplitude in order to loose 3dB in suppression depending on what the nominal suppression is. Table 1 summarizes the results.

Table 1: Suppressed Carrier Amplitude And Phase Noise As A Function Of Suppression. Required Voltage Change On The Amplitude Or Phase DACs For A -3dB Change In Suppression Is Shown In The Last Two Columns

Suppression	Amp. Noise [rel. to 1 pp]	Pha. Noise [deg pp]	-3dB Change Phase [mV]	-3dB Change Amp [mV]
-40	3e-4	3	30	15
-50	3e-4	10	10	5
-60	3e-4	30	4	2
-70	3e-4	300	1	0.3
-80	3e-4	360*N	0.3	<0.1

The resolution of the used DACs equals1 $CNT = 40\ \mu V$. It is therefore not possible to control the given setup below app. -80 dB of suppression. For a higher suppression it is necessary to have more sensitive actuators. This can be normally achieved with a reduced range variable phase shifter or attenuator. This suggests that having two loops would help decreasing the suppression value: a high-sensitivity, reduced-range and a low-sensitivity, large-range loop.

Slow Algorithm

Figure 3 shows the operation of the slow algorithm. The graph above shows the suppression value as a function of DACs control voltages for amplitude and phase. The multiple plots of various colours represent each iteration. One can see that the range of sweep is getting smaller, the sweep is finer and the suppression is higher. The

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amplitude and phase iterations are interleaved. The plot below in Figure 3 shows individual minimum suppression values as a function of iteration number. The graph shows that it was possible to achieve -80 dB of suppression, which is close to the limit of the setup. The algorithm proved to converge within 25 steps under all conditions we used it in (e.g. large changes of amplitude and phase transfer functions).

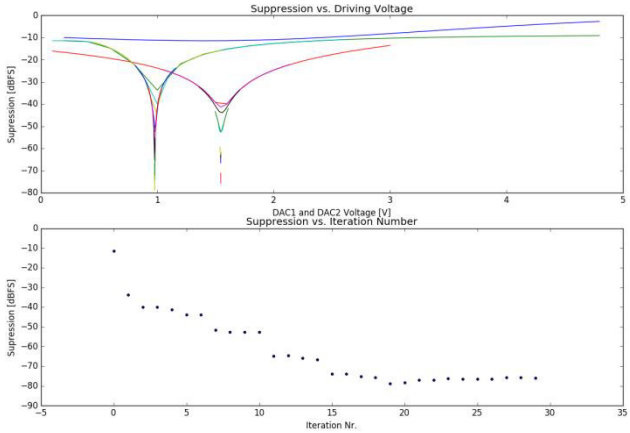

Figure 3: Suppression value as a function of DAC voltages. A full range sweep is done first. The setup has one optimal point. The graph below shows the speed of convergence (maximum suppression for each iteration).

Fast Algorithm

Both fast algorithms (amplitude/phase, 3 points) were tested by inducing large perturbations in the loop. Large perturbations of phase (> 40 deg) and amplitude (>0.1 dB) were corrected.

The initial implementation of the amplitude/phase method proved to be very unstable under these conditions because of the large fluctuations of phase noise (> 360 deg). The fluctuations caused phase wrapping which added additional static phase offsets. This method also assumed that amplitude and phase can be decoupled, if we work at high suppression values. Investigations showed that this assumption was correct but this condition was easily voided with large external perturbations. Under large perturbations correcting the amplitude based on amplitude change information and correcting phase based on phase error information can lead to loop instabilities. With more exception handling, a more frequent switching between fast and slow algorithm the amplitude/phase algorithm can still be an interesting approach. However, the disadvantage of a non-perfect receiver (non drift-free electronics) still remains and can be solved by adding more complexity to the system.

The 3 points method was also tested by inducing large perturbations (amplitude and phase) in the loop during operation. The system always recovered and brought the suppression value to the expected limits. The algorithm is only active if the suppression is worse than a certain value and it does not act if the suppression is better than a set-point value. Figure 4 shows the operation of the algorithm over a longer time period (10 h).

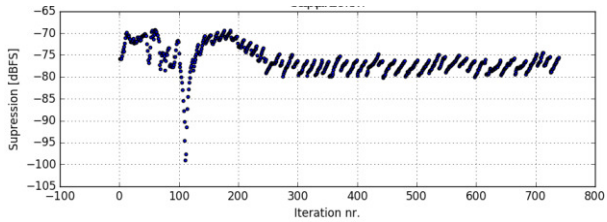

Figure 4: Suppression value over 10 h of loop operation under normal operating conditions (no ext. perturbation). The initial transients represent the system warm-up.

The 3 points algorithm can be implemented on an FPGA. The estimated delay is 100 clk cycles per iteration. With a 1MHz processing rate we need 100us per iteration. Measurements show that the fast algorithm can converge within 200 iterations for large (extraordinary) loop perturbations and needs <10 iterations during normal operation. This gives 1ms-20ms of delay at 1MHz processing. Steps in the future should go into algorithm optimization towards less delay, higher processing speed and loop parameters optimization.

CONCLUSION

In this paper we have built and tested a possible automatic carrier suppression setup. The automation comprises of a slow and fast algorithms. Two variants of the fast algorithm were investigated where the second method (3 points) proved to be more robust and less complex. It can also be concluded that a two-loop system can achieve higher suppression values also with standard DACs (18 bit). The speed of the fast algorithm is estimated to 1ms with possibilities for improvements (factor of 50 is realistic).

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