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DEMONSTRATION OF FEASIBILITY OF THE CLIC DAMPING RING EXTRACTION KICKER MODULATORS

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Abstract

The CLIC study is investigating the technical feasibility of an electron-positron collider with high luminosity and a nominal centre-of-mass energy of 3 TeV. Pre-damping rings and damping rings (DRs) will produce ultra-low emittance beam with high bunch charge. The DR kicker systems must provide extremely stable field pulses to avoid beam emittance increase. The DR extraction kicker system consists of a stripline kicker and two pulse modulators. Specifications for the electromagnetic field pulses require that the modulator produce pulses of 160 or 900 ns flattop duration, +/-12.5 kV and 305 A, with ripple and droop of not more than +/-0.02 % (+/-2.5 V) with respect to an ideal waveform. Inductive adder topology has been chosen for the pulse modulators where the output waveform can be adjusted by applying analogue modulation methods. Two full-scale, 20-layer, 12.5 kV prototype inductive adders have been designed and built, and they are being tested at CERN. These modulators will be tested with a prototype stripline kicker, installed in a beamline at ALBA Synchrotron Light Source in Spain. The results of the laboratory tests and measurements are presented.

INTRODUCTION

The Compact Linear Collider (CLIC) would be a high-energy electron-positron collider [1]. It could provide very clean experimental environments and steady production of all particles within the accessible TeV energy range. To achieve high luminosity at the interaction point, it is essential that the beams have very low transverse emittance: the Pre-Damping Ring (PDR) and Damping Ring (DR) damp the beam emittance to extremely low values in all three planes.

Stripline kickers are required to inject beam into and extract beam from the PDRs and DRs [2]. Jitter in the magnitude of the kick waveform causes beam jitter at the interaction point [3]. Hence, in particular, the DR extraction kicker must have a very small magnitude of jitter: the 2 GHz specifications call for a 12.5 kV pulse of 160 ns duration flat-top, with a combined ripple and droop of not more than ±0.02 % [1]. The 1 GHz specifications call for a burst of two 160 ns duration pulses with 580 ns between the end of the flat-top of the first pulse and the beginning of the flat-top of the second pulse. This can also be fulfilled with a single 900 ns, continuous, flat-top pulse. The requirements for the voltage and stability during two 160 ns flat-top sections are the same as for 2 GHz design, i.e. ±0.02 % [1]. The flat-top repeatability requirements are also extremely tight, ±0.01 %, for both RF system designs [1].

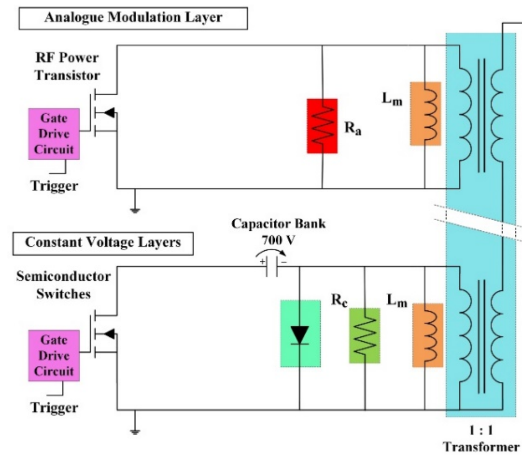

Figure 1: Schematic of an inductive adder with a single constant voltage layer with core loss resistance Rc and magnetizing inductance Lm, and with an analogue modulation layer with modulation resistance Ra, magnetizing inductance Lm and an RF power transistor.

THE INDUCTIVE ADDER

A review of literature of existing pulse generators has been carried out and an inductive adder (Fig. 1) has been selected as the most promising means of achieving the specifications for the DR kickers [4]. The inductive adder is a solid-state modulator, which can provide relatively short and precise pulses. An early reference about design principles of an inductive adder is given in [5] and an extensive summary of previous developments of inductive adders at Lawrence Livermore National Laboratory is given in [6], with examples of using modulation techniques for adjusting output waveforms. More recent research on inductive adders, also called inductive voltage adders or linear transformer drivers in the literature, have been carried out for Pockels Cells divers for the National Ignition Facility [7], fast kicker systems at Lawrence Berkeley National Laboratory [8] and industrial applications of pulsed power [9].

In total five prototype inductive adders for the CLIC DR kicker systems have been designed and built at CERN. The reasoning for choosing the main components of the inductive adder has been given in [10]. With a careful design of the adder, it may be possible to directly meet the ripple and droop requirements of the PDR kicker and analogue modulation may provide a means to meet the demanding specifications for the DR kicker [10, 11]. The design parameters and the initial results for the first two prototype inductive adders were presented in [12] and [13]. These devices have been equipped with an analogue modulation layer, which can be used to compensate the

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droop and ripple of the output waveform. Operation of the passive and active modulation layers has been verified with measurements and the results were presented in detail in [14-16]. Evaluation of magnetic cores for the full-scale, 12.5 kV, 250 A, prototype inductive adder was presented in [17]. Three papers [17-19] presented initial measurements on the first five layers of the full-scale prototype inductive adder. The detailed electrical design of the full-scale prototype inductive adder was presented in [18]. Two recent papers [20, 21] presented initial measurements on the first 20-layer, full-scale, prototype inductive adder with 10 or 17 constant voltage layers installed and one analogue modulation layer in operation, up to 6.4 kV of operation voltage. This paper is a continuation of these studies.

SPECIFICATIONS FOR THE 12.5 kV PROTOTYPE INDUCTIVE ADDER

Table 1 shows the specifications for the 12.5 kV prototype inductive adder for the CLIC DR. In the CLIC DR kicker system, the inductive adder generates pulses for a stripline kicker, which has an average odd-mode impedance of 40.5 Ω during a pulse [2]. The striplines may be terminated with their odd-mode characteristic impedance and therefore the nominal output current of the inductive adder, at 12.5 kV, would be 309 A. The full-scale prototype inductive adder has been designed to supply pulses with up to 900 ns flat-top duration. The specification for the maximum allowed total pulse duration, including rise and fall time and flat-top, is 2.2 μs [1]. However, to limit stress on the kicker system, the desired rise and fall times are in the range of 100 ns.

Simulation studies of the CLIC DR extraction kicker striplines have shown that, in order to achieve the required stability for the total of the deflecting magnetic and electric fields, the waveform for the kicker should be a “controlled decay waveform”, as shown in [22], instead of a perfect “flat-top” pulse. The flat-top stability and repeatability requirements for the output pulse of an inductive adder remain unchanged, however the shape of the output waveform must be compared to a simulated, optimum, pulse waveform instead of a flat-top pulse. The required pulse flat-top stability of ±0.02 %, i.e. ±2.5 V in absolute numbers for ±12.5 kV operation, defines the allowance for any variation for a single pulse with respect to the simulated reference waveform. The pulse flat-top repeatability defines the allowed difference of any consecutive pulses and it is specified to be ±0.01%, which corresponds to ±1.25 V, for ±12.5 kV operation.

MEASUREMENTS ON THE FULL-SCALE PROTOTYPE WITH 18+1 LAYERS

Measurement Set-up

Measurements shown in this paper were carried out with a prototype inductive adder with 18 constant voltage layers and a single analogue modulation layer installed, and one spare constant voltage layer (Fig. 2). The primary circuit of each constant voltage layer consisted of a single printed circuit board (PCB) with four current branches powered. Each current branch consisted of either a single NWL T00216, 12 μF, [23] or a Leclanché PPM-4 170-23.0, 12 μF [24], pulse capacitor, and an APT12057LFLL [25] MOSFET. Each cell of the inductive adder was equipped with two Finemet FT-3L type magnetic cores [17, 26]. The nominal maximum output voltage of the set-up was 12.5 kV, corresponding to approximately 700 V per layer with 18 constant voltage layers. The output waveform was recorded with a Rohde & Schwarz RTO1004 oscilloscope [27], which has a specified resolution of 14 effective bits in the required bandwidth, 100 MHz. The primary circuit of the analogue modulation layer consisted of a 2.4 Ω resistor in parallel with a radio-frequency power MOSFET, type ARF463AP1G [25].

Table 1: Specifications for the 12.5 kV Inductive Adder for CLIC DR Extraction Kicker Inductive Adder

Output Voltage	12.5 kV
Nominal output impedance	50 Ω
Output current	309 A
Flat-top duration	160 | 900 ns
Desired pulse rise/fall times	100 ns
Flat-top stability	±0.02 %
Flat-top repeatability	±0.01 %

Figure 2: Prototype inductive adder with 19 constant voltage layers and 1 analogue modulation layer (the topmost PCB).

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Measurements on a Flat-top Pulse

The goal of the measurements shown in this paper was to verify that the controlled decay waveform, required for the CLIC DR extraction kickers, can be generated by the prototype inductive adder at close to nominal operation voltage. However, the starting point was a flat-top pulse (Fig. 3), generated by applying active analogue modulation. For comparison, the waveform without applied modulation is also shown in Fig. 3 (black). The measured flat-top stability achieved by applying modulation (blue) was ±0.025 % (±2.5 V) for the best 160 ns section during the pulse. This fulfils the absolute stability requirement for the 1 GHz specifications for the CLIC DR extraction kicker system, i.e. ±2.5 V [1], at 80 % of the nominal voltage of the inductive adder. The relative stability requirement of ±0.02 % is slightly violated.

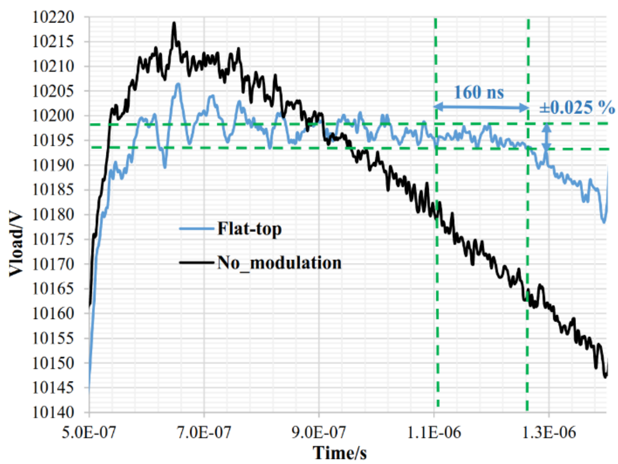

Figure 3: Measured waveform of the prototype inductive adder without modulation (black) and with active analogue modulation (blue).

The blue waveform in Fig. 3 is an average of 100 measured pulses, in order to improve the resolution of the measurement. In earlier measurements, presented in [21], ±0.01 % flat-top stability was achieved for 160 ns and ±0.02 % for 900 ns flat-top duration at 6.4 kV: hence the measured flat-top stability was better at lower output voltage. However in the measurement shown in Fig. 3, the compensation waveform applied for the analogue modulation layer was tuned manually. Compensation could be improved further by iterations in the time domain or analytically in the frequency domain, by comparing Fast Fourier Transforms of the required waveform and the measured waveform. The steps for the frequency domain corrections have been described in detail in [16].

Measurements on a Controlled Decay Waveform

Figure 4 shows a simulated optimum controlled decay waveform (green) with error margins for stability, i.e. ±0.02 % (black) and a measured waveform (blue). The measured load voltage in Fig. 4 is an average of 100 pulses. The simulated, optimum, waveform was normalised to have a maximum amplitude of 10.2 kV, which is approximately 80% of the required nominal output voltage. In Fig. 4, the simulated reference waveform is delayed in order to compare the relatively linear section of the reference waveform to the measured waveform. From time point 1.04 µs onwards, the measured waveform is within ±0.02 % over 160 ns with respect to the simulated reference waveform and this fulfils the 1 GHz specifications for the CLIC DR extraction kicker system. It is expected that the matching can be improved with the same hardware, also for a longer section than the 300 ns shown in Fig. 4. Also in this measurement, the control signal for the analogue modulation layer was adjusted manually. Matching can be improved further, with the same means as described in the case of a flat-top pulse in the previous section.

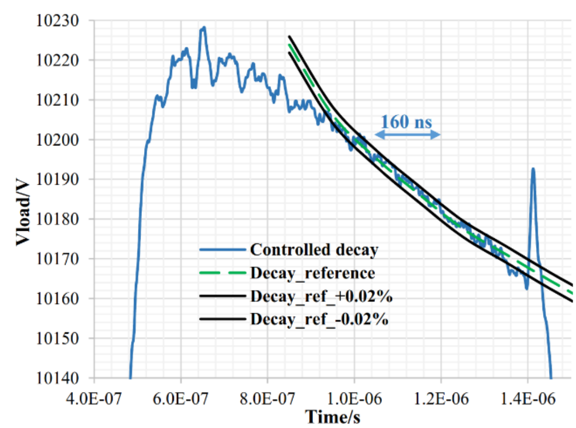

Figure 4: Simulated optimum waveform for the CLIC DR extraction kicker (green) with ±0.02 % stability margins (black), and an average of 100 measured pulses (blue) of the prototype inductive adder.

CONCLUSION AND FUTURE WORK

This paper presents measurements on the 20-layer CLIC DR extraction kicker prototype inductive adder at close to nominal operation voltage. Active analogue modulation was applied to the output pulses to generate either a flat-top pulse or a controlled decay waveform required for the CLIC DR stripline kicker [22]. In the measurements shown in this paper, the measured waveform was within +0.02 % with respect to the simulated reference waveform for 160 ns duration at 10.2 kV. However, the matching can be improved for a longer duration with the same hardware.

In the near future, the two 20-layer prototype inductive adders will be tested together with the CLIC DR prototype extraction stripline kicker [2, 28] at ALBA Synchrotron Light Source in Spain. Characterisation of both the striplines and the modulators can be carried out by changing the relative timing of the kicker pulse with respect to the passing particle bunch and by sweeping the kicking time point over the full duration of the pulse flat-top [29].

The inductive adder technology is also seen as a promising technology for use in both existing CERN

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kicker systems [30] and possible future kicker systems at CERN, e.g. for a Future Circular Collider [31, 32].

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