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HIGH EFFICIENCY, HIGH POWER, RESONANT CAVITY AMPLIFIER FOR PIP-II*

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Abstract

Diversified Technologies, Inc. (DTI) is developing an integrated resonant-cavity combined solid-state amplifier for the Proton Improvement Plan-II (PIP-II) at Fermilab. The prototype has demonstrated multiple-transistor combining at approximately 70% efficiency, at 675 watts per transistor at 650 MHz, with virtually no combining losses. The design simplifies solid-state transmitters to create straightforward scaling to high power levels. A crucial innovation is the reliable "soft-failure" mode of operation; a failure in one or more of these myriad combined transistors has negligible performance impact. The design couples the transistor drains directly to the cavity without first transforming to 50 ohms, avoiding the otherwise-necessary multitude of circulators, cables, and connectors. DTI's design increases the power level at which it is cost-effective to employ a solid-state transmitter.

The cavity-coupled amplifier built by DTI under Phase I of this Small Business Innovation Research (SBIR) effort demonstrated the following key attributes which differentiate it from other amplifiers:

- Graceful Degradation
- Simplicity of FET direct-coupling to cavity
- High efficiency through Class-E Type Operation
- Substantially reduced number of RF, electrical, and cooling connectors.

DTI is upgrading the system to accommodate more transistors in each cavity module, in order to build a complete 100 kW-class transmitter in Phase II of this SBIR, which will consist of up to four cavity modules and a central combiner.

OVERVIEW

Achieving high power from solid-state amplifiers is only possible by combining the outputs of multiple transistors. Each transistor is limited to relatively modest power levels (less than 1000 watts), so hundreds to thousands of devices must be combined to compete with large conventional Vacuum Electron Devices, such as klystrons. In contrast to phased array radars, where space combining enables the contribution of thousands of individual, low power amplifiers to create a high power beam, the RF power for accelerators must be available at a single coupler to drive the accelerator cavity. Efficiently combining multiple transistors, while delivering high reliability at an affordable cost, are the main challenges for high power solid-state amplifiers (SSAs).

Binary combining (2^N) is common at lower power, but high total insertion losses rule it out for most accelerator applications. DTI's cavity combiner is a unique form of the so-called N:1 combiner. The amplifier module combines the power of more than 64 transistors in one step. While there are other types of N:1 combiners, they typically require high power RF connectors and water cooling lines for each individual amplifier stage, leading to a level of complexity which scales with output power and total number of transistors. DTI's approach avoids most of this complexity, while the demonstrated graceful degradation feature ensures high reliability.

In this approach, the cavity serves as both a power combiner and also as an integral part of the transistor output matching network. The low output impedance transistors are not matched to an arbitrary 50 ohm impedance level; rather the coupling loop and associated transmission line (when operated in the cavity) operates at a lower impedance level, presenting the optimum load impedance at the drain of the devices. This configuration is simple, has low losses and is responsible for the graceful degradation property.

DTI's design is a radical simplification of high-power, narrow band transistor-based amplifiers, and allows for straightforward scaling to increased power levels (hundreds of kilowatts) at most accelerator frequencies.

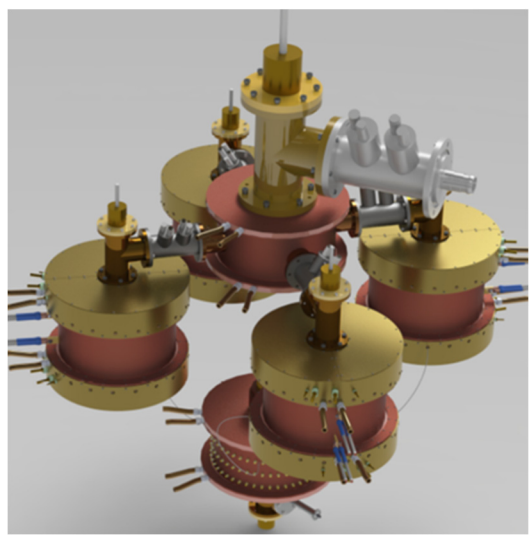

Figure 1: Conceptual layout of a high power solid-state transmitter based on four DTI cavity amplifier modules combined in a passive 4:1 cavity combiner. Power level of this concept scales to at least 500 Kw.

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In Phase II of this Small Business Innovation Research (SBIR) grant, DTI is building and testing a 100 kilowatt-class amplifier by combining up to four of the amplifier modules with associated power supplies [e.g., Fig. 1]. Under our ongoing Phase II effort, DTI is upgrading the system to accommodate over sixty four 500 W transistors in each cavity module to achieve about 40 kW each.

In a related effort, DTI has extended this design from 650 MHz to 1.3 GHz with similar results and hardware performance.

CAVITY COMBINING OVERVIEW

The resonant cavity is a well-known means of combining or dividing power. Typically, a cavity has a high *unloaded* Q, so that intrinsic losses can be very low. With heavy input and output loading, the *loaded* Q is much lower, giving good (wide) bandwidth while retaining the intrinsic low conduction losses of the cavity. The specified cavity mode offers a large, well-defined electromagnetic field structure which can be driven simultaneously by many transistors. In principle, various cavity geometry and mode combinations could be used with the cavity-combined amplifier concept. For simplicity, and many practical reasons, a cylindrical design (TM_{010} mode) was chosen for the prototypes, though a more complex coaxial or other structure may ultimately be used for a specific market-ready product.

The resonant cavity's ability to accommodate additional transistors without significantly changing the interior magnetic or electric fields by increasing the output coupling allows nearly linear increases in power per transistor and greatly simplifies each power output stage. The combination of many isolated inputs into a single cavity naturally gives a high degree of redundancy and a graceful degradation characteristic. With this design, a failure of one or several of these combined transistors has negligible performance impact. The amplifier module can continue operating stably with no interruption, and the low-level RF control system can simply adjust the drive to keep the accelerator field constant.

This behaviour is important in an amplifier with a large number of transistors integrated into one module. An adequate (excess) number of devices are designed into the amplifier to provide a performance margin for one or more failures.

High Efficiency Operation

The power amplifier contains the Class-E output circuitry implemented for the transistor. The output cavity coupling circuit incorporates the harmonically-tuned output matching network for the transistor and interfaces directly to the cavity coupling loop. The ideal Class-E waveform allows a large current conduction angle for the transistor while simultaneously minimizing V x I losses in the device. This allows high efficiency and high power to be achieved in the same circuit. Thus Class-E (and related topologies) is superior to Class-AB which achieves high linearity at the cost of efficiency and Class-C which achieves high efficiency by employing a narrow current (conduction angle) waveform.

The DTI coupling loop topology is ideally suited for push-pull transistors. The output matching network was implemented with transmission-line matching elements via the stripline, stubs and the loop itself.

SIMULATION AND DESIGN

The performance of the cavity amplifier was computed analytically and simulated in electromagnetic finite element analyses (FEA) and electronic design automation (EDA) software. The analytic results were useful for initial sizing and performance calculations, and the FEA and EDA results were useful for determining precise operating characteristics. Analytic solutions are used to identify the fields and generate the mode spectrum for the basic cavity, but FEA is used to investigate more complex structures incorporating the input and output couplers.

Modelling was been done initially with Maxwell by Ansoft (ANSYS) and is now done in EMPro and ADS by Keysight.

CLASS-E CIRCUIT DESIGN

A Class-E type tuning network was selected due to the large parasitic inductance of the drain connection to the transmission line (~2 nH per side) and the large output capacitance (~200 pF per side) intrinsic to high power RF LDMOS transistors. The effects of the large output capacitance and parasitic inductance can be resonantly tuned-out by presenting a capacitive load at the transformed end of the transmission line such that the transistor output capacitance, parasitic inductance, and capacitive transmission line load are able to efficiency resonate power out of the transistor.

Class-E circuitry approximates a square voltage waveform at the transistor drain by adding 3rd harmonic resonant tuning in the output circuitry. A classic Class-E circuit presents a partially inductive impedance to the drain at the fundamental, creating a phase shift of about 50 degrees between the total drain current and voltage. This phase shift determines the point at which the load current is diverted from the transistor conduction channel to the transistor output capacitance. The phase shift along with the real loading resistance is chosen such that the capacitor voltage drops to zero before the switch turns on and such that the capacitor voltage rises slowly when the switch turns off, thereby minimizing switching losses. Ideally a resonant tank at the load presents a short circuit at the load to all the harmonics, and the quarter-wave transmission line transforms these shorted harmonic impedances to a short circuit at the drain for the even harmonics and an open circuit to the drain for the odd harmonics.

In the cavity-coupled circuit, the impedance at the coupling loop is initially an inductance L_{loop} with an equivalent cavity loading resistance RL in parallel. A capacitance stub was then added at the coupling loop to properly tune the impedance at the loop such that the transformed

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impedance at the drains can efficiently resonate power out of the transistor.

Based on the range of impedance values presented by the loaded cavity at the coupling loop, it was determined that a coupling loop impedance of RL = 40, L = 2 nH was an efficient and realizable operating point. Given the quarter wave transmission line, it was found that a capacitive stub with capacitance ~8 pF was near optimal for presenting a Class–E type inductance load.

EXPERIMENTAL RESULTS

We extensively measured the transistors' performance outside of the cavity, with a cavity equivalent load to better model the parasitic components, and design the tuning technique for efficient operation in the cavity. The input matching network was designed for a good match across a broad frequency range.

The tuning stubs were then tested and found to conform to the simulations. Once the transistor was properly characterized outside of the cavity it was placed back into the cavity. Figure 2 shows the progression of power and efficiency for 1 to 4 coupled transistors, which achieved over 650 W per transistor at approximately 70% efficiency.

100 KW SSA CONSTRUCTION

The next step is to build a complete 100 kW-class transmitter utilizing multiple cavity amplifier modules. The medium power outputs will be combined using a passive cavity combiner [e.g., Fig. 3]. This SSA will operate at 650 MHz as required for PIP-II and other advanced linear accelerators, though the concept is readily scalable to other frequencies (as we recently demonstrated at 1.3 GHz).

The modules consist of two "bolt-circle" diameters of transistors on each endwall. A set of eight or more slots in each bolt circle allows sixteen or more total coupling loops, each driven by one or more transistors. Our effort at 1.3 GHz successfully demonstrated driving each coupling loop with four transistors. Assuming a saturated power output of 600 watts per transistor, four transistors per loop, and at least 32 loops, this exceeds the desired goal of 25 kilowatts per module with at least one redundant device, allowing N+1 redundancy and graceful degradation of output power in the event of a random transistor failure. The cavity amplifier module mechanical details will also be upgraded for high average power operation with improved RF joints and cooling.

The outputs of the 40 kW class modules will be combined in a passive cavity combiner. We plan to combine approximately four amplifier modules in a simple pillbox cavity with four $3\frac{1}{8}$" coaxial inputs and one larger coaxial output.

FEA modeling will be performed to estimate the voltages and currents in the passive cavity combiner and on the high power coupling loops. It is expected that the passive cavity may require purging or pressurization with dry air to prevent breakdown.

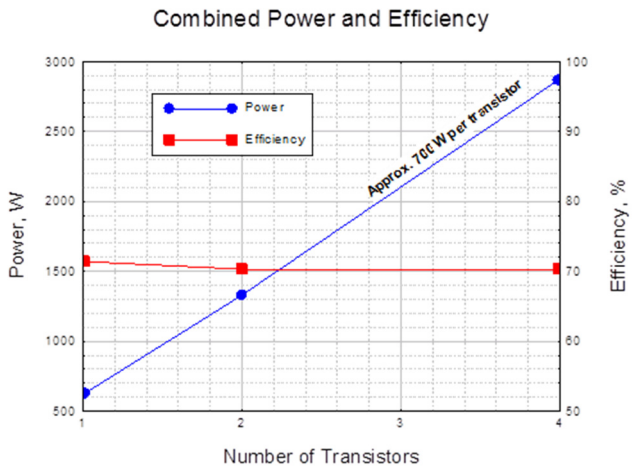

Figure 2: Improved Phase I Class-E cavity output vs. Number of Transistor Inputs.

CONCLUSION

DTI has demonstrated the efficiency and scalability of this cavity combiner design, and is working to optimize its performance under Phase II of our SBIR grant from the Department of Energy. Moving forward, we believe that this technology will provide significant life cycle cost savings for existing and planned accelerator systems, in three areas : high reliability (much greater than klystrons); improved efficiency (lower electrical power costs); simplified drive electronics (no need for high voltage power supplies or modulators); and minimized RF and thermal connections. Our plan is to demonstrate a 100 kW RF combiner in 2019.

This work is funded in part by a Department of Energy Phase II SBIR Grant (DE-SC0015780), and the cavity combiner design is patent pending.

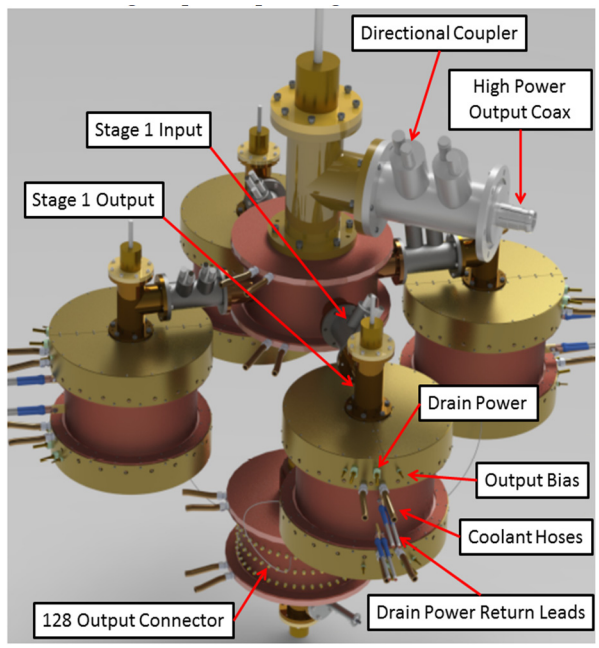

Figure 3: Arrangement of 100 kW-class transmitter based on four cavity amplifier/combiner modules.