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DYNAMIC SIGNAL ANALYSIS BASED ON FPGA FOR NSRRC DLLRF

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Abstract

As DLLRF control system designs for SRF cavities have greatly matured and the FPGA technology has improved as well, it is possible now to think about incorporating dynamic signal analysis (DSA). Implementation of a DSA in the FPGA is desired to study the frequency response of the open/closed loop gain in a SRF system. Open loop gain is useful to observe the stability of a SRF system while closed loop gain can be applied to investigate the operational bandwidth of the system feedback and also to configure the performance of a PID controller. The DSA function was confirmed by analyzing the frequency response of a digital filter and the results of the analysis will be compared with MATLAB simulations.

INTRODUCTION

Since noise suppression capabilities of the LLRF system play an important role to improve the stability of the SRF, many particle accelerator facilities use now a DLLRF system for cavity control. The advantages of a DLLRF system include anti-noise capability, flexibility, reproducibility, and extensibility [1-3]. Anti-noise capability: a digital PID feedback system can suppress cross-talk. Flexibility: the digital circuit is easy to be modified, be it for upgrade, optimization or debugging. Reproducibility: little time is needed to download a program into the FPGA core. Extensibility: many functions can be incorporated into the FPGA, such as a post-mortem circular buffer, amplitude modulation, step-response and dynamic signal analysis (DSA). A DLLRF system was developed for the NSRRC TPS and its performance was presented in published studies [4, 5]. For the current DLLRF system, this study expands the application and provides a method to incorporate the DSA function in the FPGA. Results are compared with MATLAB simulations of the FIR filter and bandwidth measurements on the TPS booster cavity.

DSA ARCHITECTURE

The DSA architecture includes two parts. One is a dynamic signal generator (DSG) and the other is a signal analysis function. The function diagram of the DSG in the FPGA is shown in Fig. 1. In this study, amplitude modulation, Fig. 1(a), is used to add a dynamic signal into the output signal of the DLLRF. In Fig. 1(a), CW is the continuous RF wave, DW is the dynamic signal, and MW the output signal of the DLLRF modulated by the product of (1+CW) and DW. The signal MW' is MW after passing through the cavity ready for analysis. A simplified DLLRF function blocks in the FPGA are shown as blue blocks in Fig. 1(b) and DSG function block the DSG function as yellow blocks. The DSG is inserted ahead of the DAC and the frequency of the dynamic signal can be presented by Eq. (1).

$$f_{DW} = \frac{f_s}{(div + 1) \times 360} \quad (1)$$

where f_{DW} is the frequency of the dynamic signal, f_s is the sampling frequency, and *div* is a component of the frequency division. The FPGA includes a counter and a cosine table with 360 points corresponding to 360 degrees. If the counter equals to *div* then the address of in the cosine table steps to the next degree, otherwise the counter increases by one step every clock cycle. The product of the cosine table output is multiplied with the gain (g) and added to unity. Finally, the output of the DSG (DW) multiplied with the DLLRF output (CW) becomes the MW signal. The relationship of MW, CW, and DW in the time domain is illustrated in Fig. 1(c) when the phase is zero.

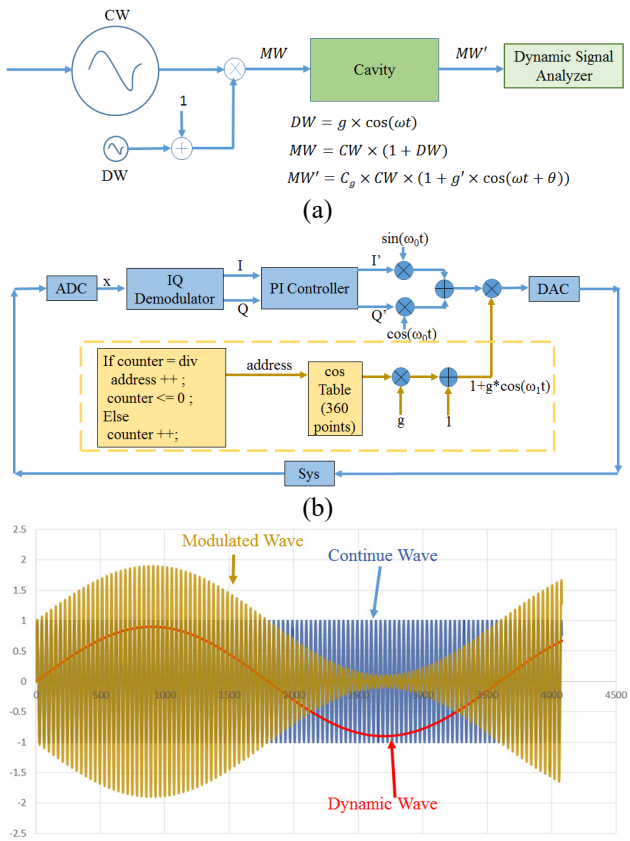

Figure 1: Dynamic signal generator. (a) Amplitude Modulation. (b) Architecture of the DSG in the FPGA. (c) Simulated Modulated, Continuous, and Dynamic waves in time domain.

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GAIN AND PHASE ANALYSIS

An important point of a DSA is its analysis method, for which an easy idea is presented to realize gain and phase evaluation. The gain is the power ratio of the dynamic signal before and after it passes through the test system. As the Fig. 2 shows, $P_{feedback}$ is the measured power in the cavity system and P_{input} is the input power to the cavity system. The electric field power of the cavity cloud is shown as the gap voltage. The dynamic signals in Fig. 2 include three different frequencies (f_{DY1}, f_{DY2}, and f_{DY3}). A_i and A_f are the voltages of the dynamic signals with f_{DY2} the frequency as observed from $P_{feedback}$ and P_{input}. The gain at frequency f_{DY2} can be calculated as Gain = $20 \cdot \log(A_f/A_i)$. The upper and lower half waves of the dynamic signal are not equal because of the nonlinear relation between the power and the cavity gap voltage. However, this does not affect the gain analysis.

Cosine wave was chosen as the dynamic signal because it was convenient for the phase analysis. The maximum amplitude of the cosine signal occurs at 0º, so it was easy to find the 0º point. In Fig. 2, the peak of the upper half wave was at zero degree. The phase in the dynamic signal analysis define the phase change between $P_{feedback}$ and P_{input}. In other words, the phase of the DSA represents the phase change before and after the dynamic signal passes through the test system. For example, at f_{DY3}, the 0º point of $P_{feedback}$ occurred while the P_{input} was 300º. Then the phase at f_{DY3} frequency was 60º (or - 300º).

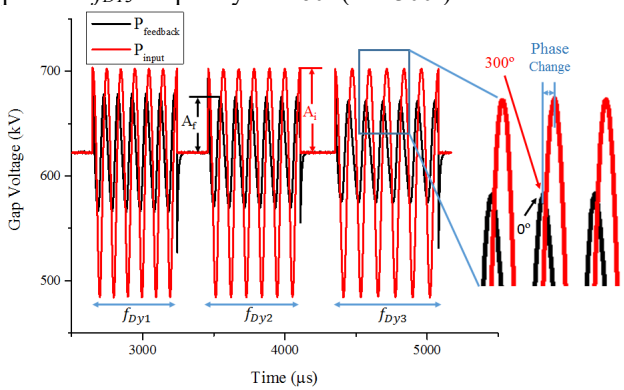
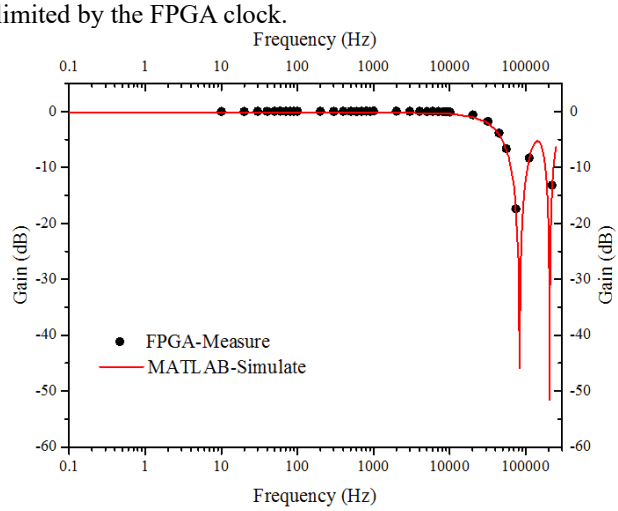


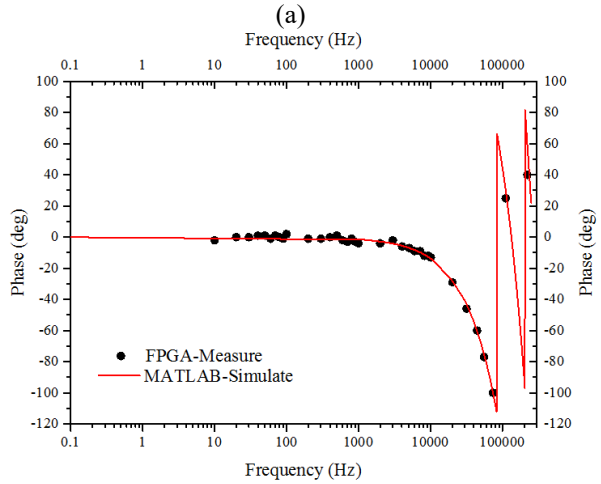
Figure 2: Example for the gain and phase analysis.

TESTING A DIGITAL FILTER

The accuracy of the DSA function was tested with a digital FIR low pass filter and the coefficients for the FIR filter were generated by MATLAB. The pass frequency was set to 100 Hz and the stop frequency was 50 kHz, while the specified value was 150. According to the coefficient, the lowpass filter was implemented in the DLLRF by the FPGA. The signal received from the ADC is processed by the lowpass filter, then analyzed by the DSA function. The results are shown in Fig. 3 and they also are compared with MATLAB simulations. In Fig. 3(a), the gain of the MATLAB-Simulation approaches 0dB when the frequency is smaller than 20 kHz, then decreases until 70 kHz, followed by oscillations beyond 70 kHz. The gain in the FPGA-Measurement matched the results of MATLAB-simulations at all frequencies. In Fig. 3(b), the phases in the MATLAB-Simulations and FPGA-Measurements were both close to zero at low frequencies, (< 10 kHz), decreasing to -110º up to 70 kHz, and then reversed toward positive degrees. However, the gain and phase of the FPGA-Measurement could not completely present the gain oscillations and phase reversals at high frequencies (> 70 kHz). According to Eq. (1), the highest frequency of the DSA is 222.22 kHz and the second highest frequency is 111.11 kHz while the clock of the FPGA is 80 MHz. The resolution of the FPGA-Measurement is limited by the FPGA clock.



(a)



(b)

Figure 3: DSA analysis results of the digital filter. (a) Gain and (b) Phase comparison of the MATLAB simulation and FPGA measurement.

BANDWIDTH OF THE TPS BOOSTER CAVITY

The TPS Booster cavity loop was analyzed by the DSA function and the result is shown in Fig. 4. During operation, the transmitter output is a continuous wave controlled by the PID feedback. The cavity loop gain includes a good noise suppression of about -30 dB at low frequencies (< 300 Hz) which becomes weaker reaching -2.5 dB as the frequencies increase from 300 Hz to 20 kHz and getting stronger again above 30 kHz. This gain curve can be separated into three parts. One is for frequencies lower

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than 500 Hz, another is a mixed area including PID and cavity effects at frequencies from 500 Hz to 11 kHz, and the last is for frequencies higher than 20 Hz. The gain at frequencies lower than 500 Hz is dominated by the characteristics of the PID controller. At frequencies higher than 500 Hz, the anti-noise capacity of the PID decreases with increasing frequency. At frequencies higher than 20 kHz, the PID had almost no effect and the gain curve presented the feature of the Petra cavity. Because the gain began to decrease above 30 kHz, we conclude that the bandwidth of the Petra cavity is about 60 kHz.

As shown in Fig. 4, the phase measurements at low frequencies (< 1 kHz) include significant uncertainties. Because the anti-noise capacity of the PID controller is working well at low frequencies, the A_M is almost constant. It is easy to be affected by errors from the ADC sampling. Comparing the phase results in Fig. 3(b) and Fig. 4, the error bar in Fig. 3(b) is almost zero because the error of the ADC sampling is suppressed by the digital filter. In the future, a digital filter will be incorporated to improve the stability of the phase at low frequencies.

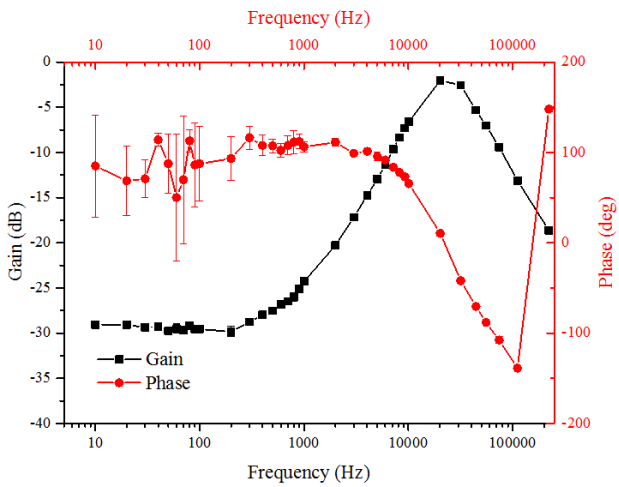

Figure 4: DSA analysis results for the TPS Booster cavity.

CONCLUSION

In this study, the DSA tool to analyse the frequency response based on a FPGA is presented. It is composed by a DSG and a signal analysis function. The feasibility of the proposed DSA is identified by the digital filter test where the gain and phase results of both the FPGA-Measurement and MATLAB-Simulations agree. Furthermore, the TPS booster cavity loop was tested with the DSA. The result of the gain curve shows the feature of the PID controller at low frequencies (< 500 Hz) and the characteristics of the Petra cavity at high frequency (> 20 kHz). Simultaneously, the Petra cavity bandwidth of about 60 kHz, could be determined from the gain curve. Although the phase measurements suffered from the interference of ADC sampling errors at low frequencies, it will be improved by incorporating a low pass filter into the measuring loop.

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